A circuit topology useful for such RIAA phono applications is shown in Figure 6-17. This circuit consists of two high-quality wide bandwidth gain blocks, U1 and U2, as discussed above. Selection of these amplifiers and their operating conditions optimizes the preamp for gain, noise, and overload characteristics. The circuit can be set up for either MM or MC operation by simple value changes and op amp selection.

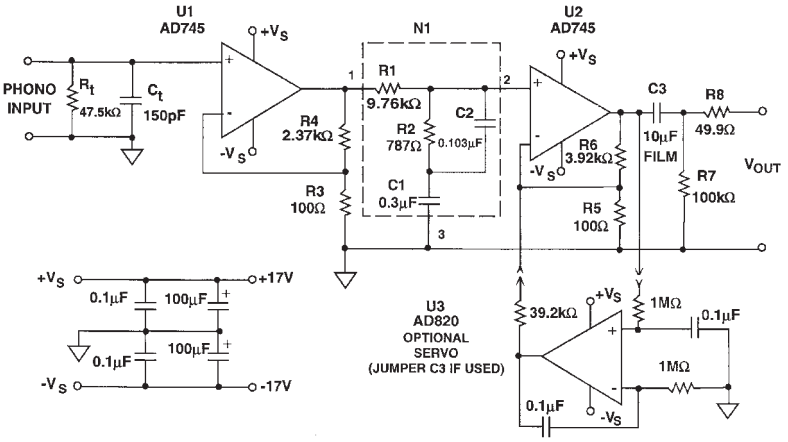

Figure 6-17: A passively equalized RIAA preamp with 40 dB gain

The gain stages are set up for the required total gain, via R_4-R_3 and R_6-R_5. In general, the total 1 kHz gain of this circuit G is:

$$G = 0.101 \bullet \left[1 + \left(R_4 / R_3\right)\right] \bullet \left[1 + \left(R_6 / R_5\right)\right] \qquad \text{Eq. 6-11}$$

The op amp gain blocks could be made identical for purposes of simplicity but are not necessarily so for the following reasons. A preamplifier topology such as this must be carefully optimized for signal-handling capability, both from an overload standpoint and from a low-noise viewpoint. Stage U1 is chosen for a gain sufficiently high that the input-referred noise will be predominantly due to this stage and the cartridge, but not so high that it will readily clip at high level high frequency inputs. Amplifiers with a ≈10 V rms output capability allow U1 to accept ≈400 mV rms at high frequencies using ±18 V supplies, while still operating with useful gain (about 25 times).

The gain of the two blocks are set by R_4-R_3 and R_6-R_5, as defined by Eq. 6-11. The gain values shown yield a 1 kHz gain that is the product of the U1-U2 stage gains (24.7 times 40.2), times that of the interstage network N (0.101). This yields an overall 40 dB 1 kHz gain. Other gains are realized most simply by changes to R_5 or R_3.

As previously noted, a passively equalized preamplifier such as this must be carefully optimized both from an overload standpoint and from a low noise viewpoint. Stage U1 is chosen for a gain sufficiently high that the input-referred noise will be predominantly due to this stage (and the cartridge, when connected), but not so high that it will readily clip at high level high frequency inputs. To aid this objective, maximum supply voltage and a high output capability amplifier should be used for U1.

Note that U1 operates at relatively high gain, but it needn't be unity gain stable. Decompensated low noise op amps such as the OP37 and the FET input AD745 will provide best signal/noise ratio here. For other FET-input types, the AD845, as well as the OP17 family types, will also yield good performance, but with higher noise levels.

In general, the preceding factors dictate that gain distribution between U1 and U2 be LOW/HIGH from an overload standpoint, but HIGH/LOW from a noise standpoint. Practically, these conflicting requirements can be mitigated by choosing the highest allowable supply voltage for U1, as well as a low noise device. Because of nearly 40 dB loss in the network N at 20 kHz, the output overload of the circuit will be noted at high frequencies first. With the gain distribution shown, the circuit allows a 3 V rms undistorted output to 20 kHz with ±15 V supplies, or more with higher supply voltages.

The equalization network N following U1 should use the lowest impedance values practical from the standpoint of low noise, as the noise output at Pin 2 of the network is equivalent to the input referred noise of A2. The network of Figure 6-17 uses the "N1" RC values of R_1-R_2-C_1-C_2 of Figure 6-9a. As noted, scaling can be applied to either network of Figure 6-9 for component selection, as long as the same ratios are maintained.

Noise in amplifier U2 is less critical than U1 at low frequencies, but is still not negligible. A low voltage noise device is very valuable to the U1 and U2 positions, as is a relatively low input current noise. If extremely low noise performance is sought, such as for a moving coil preamp, the N1 values can be reduced further, and R3 be lowered for lower noise and additional gain. For example, a 45 dB gain preamp could be realized by just dropping R3 to 56.2 Ω, and using an OP37 for U1.

As mentioned before, a low bias current device is appropriate to U1 using bipolar amplifiers. With a 100nA or less bias current device, direct coupling to a moving magnet phono cartridge is practical. For example, the 80 nA (maximum) bias current of the OP37 will induce only an additional 80 μV–160 μV input voltage offset at U1 for a typical 1 kΩ–2 kΩ cartridge resistance. For lower dc resistance MC cartridges, this will be much less of course. Similarly, the bias current induced offset voltage of U2, from the 10 kΩ dc resistance of R_1 will also be low relative to the amplified offset of U1. As a result, the worst-case overall output dc offset using two AD745s can be held to under 2 V for a 40 dB gain, allowing a single C_3 coupling capacitor for dc blocking purposes.

Frequency response of this passively equalized preamp tends to be better than that of the active versions, because of less interaction with the amplifier(s) as compared to the active preamps. It can approach the inherent accuracy of the network components in the audio range, with potentially greater errors at higher frequencies.

Figure 6-18 illustrates this point, in a simulation of the Figure 6-17 circuit using the OP37 models. The midband error is on the order of ±0.02 dB with the N1 network composite values. For practical purposes

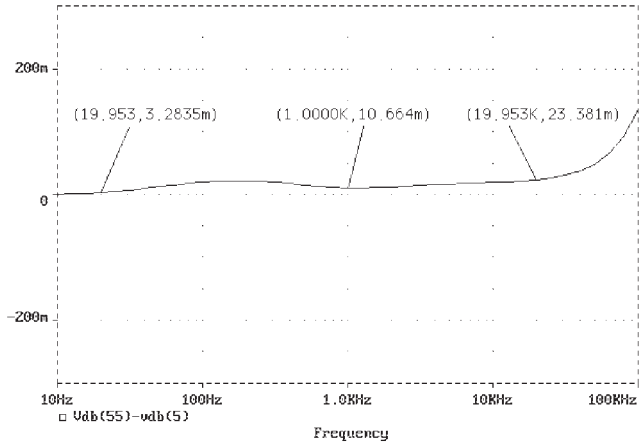

Figure 6-18: Relative error (B) versus frequency for passively equalized RIAA preamp, gain of 40 dB (simulation)

then, the frequency response errors of this circuit will be governed by the tolerances of the network components used within it.

This circuit also can be optionally adapted to servo control of the output offset. This is accomplished by deleting coupling capacitor C_3, substituting a jumper in its place, and using the noninverting servo integrator U3 around stage U2. This is shown as an option within Figure 6-17. A general-purpose noninverting servo can be used for U3, along with a low-offset op amp, such as the AD820, or the OP97.

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Audio Line Level Stages

Audio line level stages represent an intermediate level in dynamic range for practical audio circuits using modern IC devices. Line level amplifying stages generally work with single-ended or balanced input/output signal levels of 1 V–10 V, and at medium levels of power. This section discusses some basic types of audio line stages which are:

Line receivers—including line receiver stages that accept single-ended or balanced line level signals with maximum noise immunity, and provide scaled outputs for further processing.

Line amplifiers—including amplifiers that scale a received signal in single-ended form and feature low distortion designs.

Line drivers—including single-ended and balanced drivers capable of driving appreciable output levels in terms of voltage, swing, current levels, and/or difficult loads, such as capacitive lines.

Some general concepts of line driving and buffer amplifier design have been covered previously, with emphasis on video applications (see References 1–3). Some of the material in this section continues and expands on those themes with audio line-receiver and line-driver discussions in a wide variety of applications. Video applications for line driving and receiving is discussed in detail within Section 6-2.

Audio transmission systems, unlike their video counterparts, do *not* use terminated transmission lines as a rule, so long transmission lines usually appear capacitive. Therefore, the concepts of capacitive load isolation are also important to audio drivers. In general, when building practical audio circuits of any type, "housekeeping" rules of layout and bypassing are strongly recommended, particularly so for audio buffer and line driver circuits. They are discussed in further detail in that section.

The function of sending/receiving audio signals between various system components has traditionally involved trade-offs of one form or another. Fully differential or *balanced* transmission systems are best at rejecting low frequency and RF noise, so they are used for highest performance, and are discussed in some detail following.

A typical audio system block diagram using differential or balanced transmission is shown in Figure 6-19. In concept, a balanced transmission system like this could use several input/output coupling schemes within the driver and receiver. Some major points distinguishing coupling method details are discussed briefly, before addressing actual circuits.

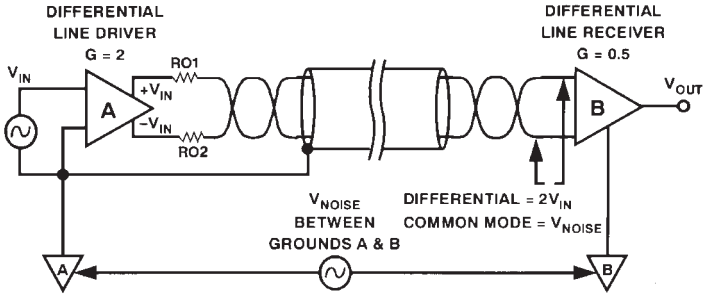

Figure 6-19: An audio balanced transmission system

Transformers (see References 4–7) have been a traditional audio line coupling element. They can be used at either input or output stage. They also have well-known problems with noise pickup, frequency response, distortion, and operating level. While these problems are soluble to some degree, answers are usually costly. Nevertheless, transformers are unexcelled in notable areas.

The single most outstanding virtue of transformer operation lies in the ability to isolate while transmitting the signal, which shows up in two regards. The first of these is that transformers, which transmit an audio signal between the end terminals of an isolated winding, thus *galvanically isolate* driver and receiver stages. This is accomplished at common-mode voltage (ground difference) levels up to the breakdown potential of the windings, allowing signals to be transmitted across very high ground potential differences (tens or hundreds of volts). This feature is very difficult to achieve with solid-state circuitry. Secondly, suitably designed transformers can have very high common-mode rejection (CMR) over the audio range, ≥100 dB in some cases, a factor basically intrinsic to their nature. Some transformer-isolated stages are described in this section.

In practice the general system of Figure 6-19 can use either transformer-based or active stage coupling to the line, at either end. The goal for either approach is to reproduce a final signal V_{OUT} equal to V_{IN}, while rejecting noise between grounds A and B by a factor of 80 dB–100 dB. Typically, a unity gain (overall) design uses a balanced line drive of $\pm V_{IN}$, followed by a receiver gain "G" of ½, which maximizes the receiver CM range.

A point worth noting that the ± voltage drive to the line need *not* be exactly balanced to reap the benefits of balanced transmission. In fact the drive can be asymmetrical to some degree, and the signal will still be received at V_{OUT} with correct amplitude, and with good noise rejection. What *does* need to be provided is two well-balanced line-driving impedances, R_{O1} and R_{O2}. Also, in conjunction with these balanced drive impedances, the associated (+) and (–) receiver input impedances should also be equal. The technical reasons for this will be apparent shortly.

Audio Line Receivers

A brief review of the topologies and application points of audio line receivers helps in understanding their evolution, and more importantly, how their audio performance differs with topological changes. Figure 6-20 is a diagram of a classic 4-resistor differential amplifier. This general circuit is also known as the most simple instrumentation amplifier form, even though its performance as an in amp has severe limitations. Within audio applications, this and related circuits are called "line receivers" for the sake of brevity. Various in amp type topologies have developmental histories dating from the late sixties up to and including today's modern in amp ICs (see References 8–12 and Chapter 2).

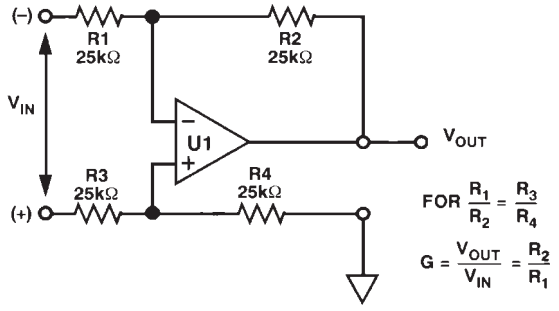

Figure 6-20: A simple line receiver using a 4-resistor differential amplifier

In today's professional audio world, signals by and large get transmitted in balanced mode (Figure 6-19). This fact is simply due to the much greater noise immunity of this method, vis-à-vis the more simple, but highly noise-susceptible single ended method.

Yet, even within the professional audio world there is no real unanimity on signal driver and receiver circuits for use within balanced circuits—they take on many forms and have differing performance, and a wide variety of circuits find use. Before getting into actual receiver circuitry, it is helpful to take a brief look at some problems impacting circuit performance in terms of common mode (CM) noise susceptibility. This will illustrate how careful hardware choices lowers system cost/size, and maintains excellent performance. Conversely, simple receivers can also be used, for modest performance.

Source-Load Interactions within Balanced Systems

Some recent attention has focused on the general problem of noise susceptibility in audio system interfacing (see References 13 and 14). The discussions below are concerned with how balanced system drivers and receivers interact fundamentally to produce undesired side effects of noise susceptibility. Suggestions for practical solutions are then offered.

In most simple form, a balanced audio transmission system consists of a differential output driver, an interconnecting cable, and a differential input receiver, such as shown in Figure 6-19 (again). The driver produces nominally equal and out-of-phase output signals, with some characteristic (and matched) source impedances, R_{OUT1} and R_{OUT2}. As will be seen, from a noise susceptibility standpoint, it is highly desirable that these two impedances be well balanced, i.e., matched. The driver is connected to the input end of a balanced transmission line, typically a shielded twisted pair. At the opposite end of this line, a differential input receiver receives the balanced signal, and (ideally) rejects the CM noise voltage V_{NOISE}.

The design of both the driver and the receiver has great influence upon how well the overall scheme works in transmitting a noise-free audio signal from driver to receiver. References 14 and 15 discuss different driver and receiver types, active and passive. These papers bring out the inherent degradation in noise sensitivity active receivers can trigger, if they do not have input characteristics which are an appropriate complement to the system driving impedances.

From a noise introduction point of view, the balanced transmission system under discussion can be analyzed as a bridge circuit, as shown in Figure 6-21. Here the two source resistances R_{OUT1} and R_{OUT2} correspond to the output resistances of the differential driver voltage sources. Similarly, input resistances R_{IN1}

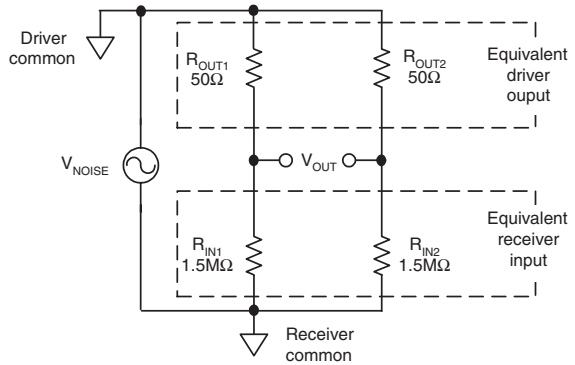

Figure 6-21: A conceptual driver/receiver diagram of a balanced line audio system with key impedances and CM noise

and R_{IN2} correspond to the input resistances of the differential receiver. V_{OUT} represents the output of this bridge, which is due solely to the bridge mismatching and CM noise V_{NOISE}.

Such a bridge as Figure 6-21, when *maximized* for output sensitivity, will produce a differential output V_{OUT} which is highest as a function of element unbalance when all four resistances are of the same order.

The following general expression illustrates the intrinsic common-mode rejection (CMR) of this bridge as a function of the resistance values and their deviation, K_R:

$$CMR\,(dB) = 20 \bullet \log_{10}\left[\left(1 + \left(R_{IN}/R_{OUT}\right)\right)/K_R\right] \qquad \text{Eq. 6-12}$$

Some sample calculations with this relationship show that *CMR* is a *minimum* for a given change in K_R (the total resistor deviation expressed in fractional form) when $R_{IN} \approx R_{OUT}$. A CMR minimum is simply another way of saying that the bridge is most sensitive to the excitation voltage V_{NOISE} when $R_{IN} \approx R_{OUT}$. To place this in perspective, a conventional instrumentation bridge operates thusly, with all four arms nominally equal. This yields the highest sensitivity to the applied voltage (see Chapter 4).

On the other hand, CMR is maximum and bridge sensitivity is *minimized,* when the upper and lower arm resistances differ widely. This improves substantially as R_{IN} becomes >> R_{OUT}. Or, within an audio system, as the driver R_{OUT} is by design made much less than the receiver R_{IN}. With the example values above, there is a 1/30,000 ratio between the R_{OUT}/R_{IN} upper/lower elements. This factor makes relatively high percentage changes in either the upper (or the lower) arm resistances a somewhat harmless phenomenon. In other words, small R_{OUT} or R_{IN} changes will then have little CMR effect upon the output.

For example, taking the Figure 6-21 values and assuming a 10% change in R_{OUT}, will produce an output which is about 110 dB down from the noise voltage V_{NOISE}. By contrast, if all the bridge values were to be equal, the same 10% deviation would produce an output only 26 dB down. Note that there are two control point towards this. One can *lower* R_{OUT}, for a given R_{IN}, and increase CMR. Or, one can achieve the same effect by *increasing* R_{IN}, for a given R_{OUT}. This makes the point that *a high ratio between R_{IN} and R_{OUT}* aids in maintaining high CMR, as is shown by Figure 6-22.

In a real transmission system, there will be inevitable noise potentials developed between the respective driver and receiver chassis common points, since they are located separately and are powered with different power sources. The resulting noise voltage can be predicted with the aid of Figure 6-22. As a minimum, a good system should maintain an R_{IN}/R_{OUT} of at least 1000, with 10 k or more a goal. Under such conditions, with a bridge unbalance of 10%, this will still allow a theoretical CMR of 80 dB to 100 dB (see center column, with cited examples shown in boldface).

R_{IN}/R_{OUT}	CMR(dB) for K_R = 0.1	CMR(dB) for K_R = 0.01
10	40.8	60.8
100	60.1	80.1
400	72.1	92.1
1k	80	100
10k	100	120
30k	109.5	129.5
100k	120	140

Figure 6-22: High R_{IN}/R_{OUT} minimizes sensitivity to CM noise, bridge imbalance

As noted, dependent upon the bridge impedance-related sensitivity, some fraction of the CM V_{NOISE} appears as V_{OUT}. The basic process of the conversion of the CM noise voltage into a differential voltage is called *mode conversion*. It is important to understand that mode conversion can only be prevented, not fixed after the fact. Once the noise voltage appears as a differential signal, no receiver can distinguish it from a valid signal.

Finally, it is important to realize that what has been discussed thus far addresses the most basic portion of this system and the impact on CMR. The line receiver circuitry itself obviously also has a big influence, as it determines R_{IN}. This is discussed next.

The Simple Line Receiver

The simple line receiver circuit of Figure 6-23 below uses four matched resistors and an op amp for gain. Such bridge-based difference amplifiers are *critically* dependent upon the resistor ratio matching for good performance, an enormously important point. The amplifier can also be critical, but most practical limitations of this topology arises from *un*-balancing of the R_1-R_4 bridge (for either/both ac and dc).

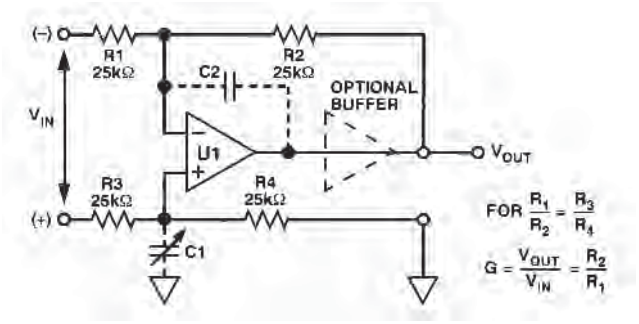

Figure 6-23: A simple line receiver with optional HF trim and buffered output

The circuit appears somewhat trivial, as the minimum ingredients are four matched film resistors and a good audio op amp. While this works functionally, how well it works in rejecting noise is another thing. C1 and C2 are optional, and can be used to trim HF CMR. Also optional is the use of an in-the-loop unity-gain buffer (more below).

A main purpose of this circuit and all line receivers is to reject CM noise, as discussed above. But even with a high quality op amp for U1, noise rejection is only as good as the resistor matching. More precisely, the resistor *ratios* R_1/R_2 and R_3/R_4 must match extremely well to reject noise (the absolute values are relatively unimportant).

With care, picking four 1% resistors from a same-vendor, same-batch lot is a step that can yield ratio matching of, say, 0.1% total error, and will achieve a common-mode rejection (CMR) of 66 dB. Four 1% tolerance resistors with just one off by 1% will yield about 46 dB CMR. In general, the worst-case CMR of a circuit of this type is:

$$CMR\,(dB) = 20 \bullet \log_{10}\left[\left(1 + \left(R_2/R_1\right)\right)/4K_R\right] \qquad \text{Eq. 6-13}$$

where here K_R is the *individual resistor tolerance* in fractional form. This form of the expression is most useful for cases using four discrete resistors (see Reference 8). More likely, a single component network with a *net matching tolerance* of K_R would be used for this function, in which case the expression then becomes:

$$CMR\,(dB) = 20 \bullet \log_{10}\left[\left(1 + \left(R_2/R_1\right)\right)/K_R\right] \qquad \text{Eq. 6-14}$$

In either case, this assumes a significantly higher *amplifier* CMR, such as ≥100 dB).

Eq. 6-13 shows that the worst-case CMR due to tolerance build-up for four unselected 1% resistors to be much worse, 34 dB in fact. Clearly for high and stable noise rejection, circuits such as these need four single-substrate resistors, made/trimmed simultaneously. Networks using thick-film and thin-film technology are available from companies such as Caddock and Vishay-Ohmtek, in ratio matches of 0.01% or better.

Some simulations may bring this point of critical matching home more clearly. Figure 6-24 shows the effect of various dc-matching of a differential amplifier such as Figure 6-23, with a single resistor mismatch in R_1 of 0.1% (top trace), 0.01% (middle trace) and perfect matching (bottom). Also, this display of CM error versus frequency indicates a reactive imbalance for the perfect dc-balanced (bottom) case. This is due to an intentional capacitive mismatch in the circuit, representing stray capacitance imbalance.

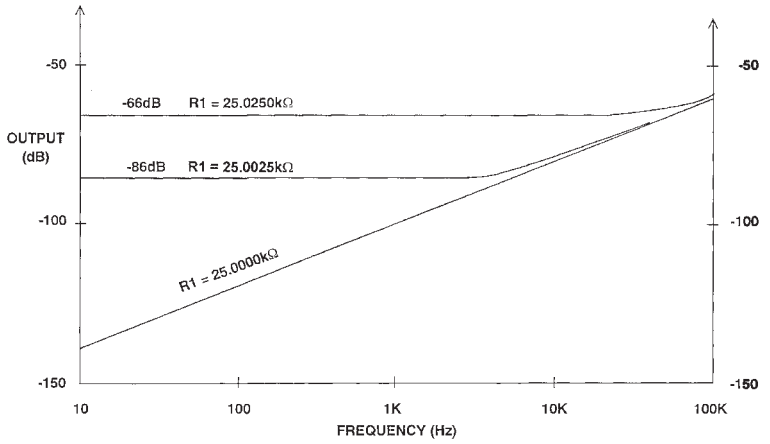

Figure 6-24: Simple line receiver CM rejection versus frequency for various R1 trims (simulation)

The effect of ac-matching on this differential amplifier using matched resistances, with C_2 matched to C_1 (10pF) results in essentially flat CM error versus frequency (not shown). In contrast, a 10% capacitive mismatch results in a CM degradation as low as 10 kHz. Clearly then, for wideband audio uses, the bridge ratio needs to be maintained for ac as well as dc, to achieve flat CMR versus frequency. Capacitances from the R_2/R_1 and R_4/R_3 nodes need to be balanced. In practice, this is best achieved with very low and/or balanced parasitic capacitances at C_1-C_2.

It is worthy of note that this circuit also has a highly desirable side property; that is, it *divides down* the input CM voltage. Thus it is inherently protected against overvoltage. In general, practical line receivers *require* some sort of input protection, for safe use in harsh environments, and to allow CM voltages to exceed the supply rails. The receiver gain-set resistors double in performing this function here. The working CM input range of Figure 6-23 is $(1+(R_3/R_4)) \times V_{CM(U1)}$, and differential input resistance is $R_1 + R_3$. Circuit gain isn't easily changed, because of the matched R_1–R_4 ratios.

Implementing the Simple Line Receiver Function

To offer a reasonably high impedance to the line, simple receivers such as these typically use input resistances of 25 kΩ or more. When working from 50 Ω sources, this allows a basic R_{IN}/R_{OUT} ratio of 500 (see previous discussion and Figure 6-22, again). Given a well-matched resistor network and low or balanced

parasitic capacitances, suggested amplifiers for U1 are the AD711, AD744 (singles), and the AD712, AD746, OP249, OP275 (duals). With 10 kΩ–25 kΩ resistances, extremely low voltage noise in the amplifier isn't critical. High slew rate (SR) and output drive allows clean high frequency, high amplitude levels, and 600 Ω load capability. If low impedance loads need to be driven, output current of a standard op amp can be boosted with an in-the-loop unity gain buffer, connected between U1 and the load/feedback point. Devices such as the BUF04 or a (follower-connected) AD811 can serve well here (discussed in the later sections).

From a dc and ac trim/balance perspective, the Figure 6-23 topology is most effective with resistors and amplifier made simultaneously in a single monolithic IC. The ADI SSM2141 and SSM2143 are such ICs, characterized as low distortion, high CMR audio line receivers with net gains of unity (SSM2141), and 0.5 (SSM2143). The SSM2141 has resistors as shown in Figure 6-23, while the SSM2143 uses 12 kΩ/6 kΩ resistors.

In applying circuits of the Figure 6-23 type (or other topologies which resistively load the source), a designer must bear in mind that all *external* resistances added to the four resistances can potentially degrade CMR, unless kept to proportional value increases. To place this in perspective, a 2.5 Ω or 0.01% mismatch can easily occur with wiring, and if not balanced out, this mismatch will degrade the CMR of otherwise perfectly matched 25 kΩ resistors to 86 dB. These circuits are therefore best fed from balanced, low impedance drive sources, preferably 25 Ω or less.

Other Issues with the Simple Line Receiver

An application point that becomes relevant for large high performance systems with multiple balanced pair lines is the issue of receiver *load balance*. Ideally, an audio line receiver should exhibit equal ac loading at the two inputs. With the simple line receiver of Figure 6-23 (and all similar circuits), this goal isn't met—i.e., the basic circuit does *not* present balanced loading to the two input lines. It is important to note at this point that this is not a function of the devices used to implement the circuit, it is more a function of the architecture itself.

When Figure 6-23 is driven from complementary sources V_{IN} and $-V_{IN}$, the simple line receiver exhibits a property of unbalanced input currents in the R_1 and R_3 legs, due generally to feedback action. For the like values of Figure 6-23, the current in R_1 is three times that in R_3. Thus the inputs load the two input lines differently, as noted.

In large systems with multiple balanced transmission line pairs, the current imbalance in the input lines is potentially serious, as associated fields will not cancel as they do for completely balanced loading. Thus there is potential for crosstalk impairment in such systems using the simple line receiver topology.

On the other hand, while not optimum from a large system and/or line balance viewpoint, the simple line receiver is nevertheless useful in more modest situations. With resistors R_1–R_3 relatively high (20 k or more), it is adequate for small-scale or confined systems where I/O lines are relatively short, few in number, they are not cabled, and the source impedances are low. In such uses, devices like the SSM2141 and SSM2143 can serve well as efficient, single IC line receiver solutions.

Balanced Line Receivers

For highest performance uses, it is a key point that audio line receivers exhibit equal loading to the source at both inputs—i.e., they should be truly balanced. At least two topologies meet this criteria and are thus suited for professional use in balanced systems.

Balanced Feedback Differential Line Receiver

David Birt of the BBC has analyzed the simple line receiver topology and presented a modified and balanced form, as shown here in Figure 6-25 (see Reference 7). Here U1 uses an 4-resistor network identical to that of Figure 6-23, while a second feedback path from unity gain inverter U2 drives the previously grounded R_4 reference terminal. This has two basic effects overall; the input currents in the R_1–R_3 input legs become equal in magnitude, or balanced, and the gain of the stage is halved.

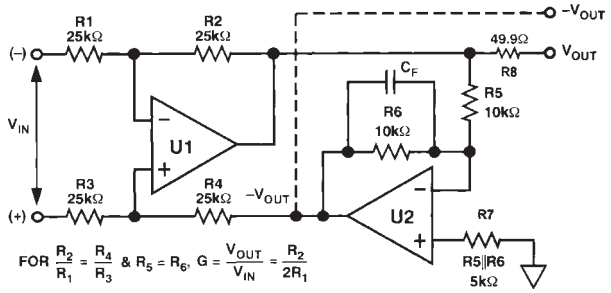

Figure 6-25: Balanced line receiver using push-pull feedback

Compared to Figure 6-23, and for like resistor ratios, the Figure 6-25 gain from V_{IN} to V_{OUT} is ½, or a gain of –6 dB (0.5) as shown. However it also offers an optional complementary output from U2, $–V_{OUT}$. Like Figure 6-23, the gain of this circuit is not easily changed, as it also involves precise resistor ratios.

Because of the two feedback paths, this circuit holds the inputs of U1 at a null for differential input signals. However CM signals are still seen by U1, and the CM range of the circuit is $(1+(R_3/R_4)) \times V_{CM(U1)}$. Differential input resistance is $R_1 + R_3$. As can be noted from the figure, the circuit can be broken into a simple line receiver (left), plus an inverter (right). Existing line receivers like Figure 6-23 can be converted to a balanced topology by adding inverter U2. A performance example of this is discussed below.

Alternate Balanced Line Receivers

Other instrumentation amplifier types can achieve the goal of fully balanced input loading, but may not be desirable for other reasons. For example, there are standard

in amp circuits not shown here which use either two or three amplifiers and have properties of high input impedance, due to the use of noninverting inputs (see References 8–11). The drawbacks of these topologies as audio line receivers lie in limited gain and CM range. Also, importantly, they require four resistors beyond those for gain, just for input overload protection. Since these resistors also influence gain and CMR, they must also be precision ratio matched types. As a net result, workable audio line receivers using these in amps aren't really highly practical (eight or more matched resistors, plus two or three op amps).

An "All Inverting" Balanced Line Receiver

Figure 6-26 is an elegantly attractive topology that seems well-suited to audio line receiver use. Using all amplifiers as inverting stages, this circuit can be configured for very high CM voltage range and high input resistance. With the resistor ratios matched as shown, the CMR of this circuit can be better than the others for a given resistor match, since both amplifiers see no CM voltage. The CM range of this circuit is set as $(R_1/R_2) \times V_{OUT(MAX)U1}$. The differential input resistance is $R_1 + R_3$.

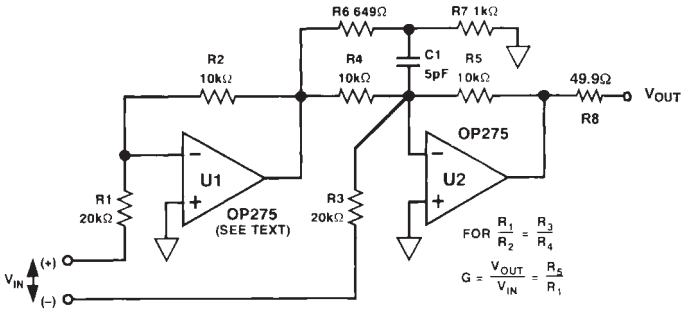

Figure 6-26: "All Inverting" balanced line receiver

The circuit has the unusual and desirable property of single resistor gain adjustment via R_5, *without* any CMR interaction. Gain can also range from below to above unity, making it flexible in that regard. As shown, it is driven with a balanced signal, but note that it can also be driven with single-ended sources at either the (+) or (–) terminal, with no gain interaction from the opposite input port, due to the use of inverting amplifiers. Multiple inputs can be summed, with additional ratio matched input resistor pairs (not shown). In this example gain is set at 0.5, consistent with general line receiver system requirements.

This circuit is also well known in basic form (see References 8–11). Note, however, that in this configuration, optional phase lead compensation is used to enhance high frequency CMR. A small capacitor shunting R_4 with a value chosen to compensate for the gain-bandwidth of U1 compensates for the lag through U1, and maximizes phase matching of the ± CM signals at U2. However, for op amps with gain bandwidths above a few MHz and practical resistor values, this can result in difficult-to-control small capacitor values.

The R_6-R_7-C_1 tee network reduces the effective value of C_1, by dividing the applied voltage. A nominal division ratio can be approximated by this expression:

$$K_C = 1 \Big/ \left(2\pi\ BW_{(U1)} R_4 C_1\right) \qquad \text{Eq. 6-15}$$

where K_C is the division ratio of R_6-R_7. For this example, with BW(U1) about 5 MHz (the closed loop bandwidth of U1), K_C is about 0.6, making C_C effectively about 3 pF. Circuit parasitics, loading effects and part variations make this inexact; however, once nominal compensation for a given layout and devices is achieved, a 30 dB CMR improvement in 10 kHz CMR is possible (vis-à-vis no phase compensation). This trim network isn't necessary to the circuit's basic function, but is nevertheless useful for audio applications.

Performance of Balanced Line Receivers

The balanced line receiver configurations of Figure 6-25 and Figure 6-26 were tested for CM performance, with common conditions of G = 0.5, Vs = ±18 V, and a 10 V rms input sweep, 20 Hz–50 kHz, filter bandwidth of 80 kHz. The Figure 6-25 topology was implemented with an SSM2141 for U1, with U2 an OP275 inverter, with C_F = 68 pF. Figure 6-26 was implemented with an OP275 and a resistor network matched to 0.005%, with the C_1 network trimmed as shown. These results are shown in Figure 6-27.

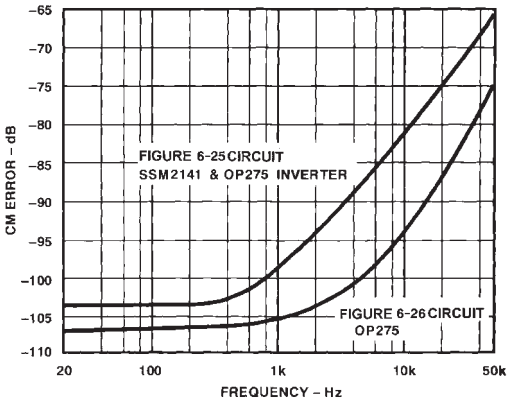

Figure 6-27: Balanced line receivers CM error versus frequency

Both circuits show excellent results, with ≤1 kHz CM errors of –100 dB or lower. The Figure 6-26 topology offers better results at the higher frequencies, perhaps due to the trimming technique used (not applicable to the Figure 6-25 circuit). In the worst case, the CM errors are no poorer than –80 dB at 10 kHz, still very good for an untrimmed circuit.

THD + N data was taken on both circuits and, while dominated by the noise floor at many levels, there are some differences worth noting between the two. Figure 6-28 shows THD + N performance of the Figure 6-25 SSM2141/OP275 circuit for loading conditions of 100 kΩ, successive input sweeps of 1, 2, 5 and 10 V rms, and ±18 V supplies. The lower level sweeps are noise dominated, while the 5 and 10 V sweeps show some distortion rise at high frequencies. Distortion of this circuit also rises with loading of 600 Ω (not shown).

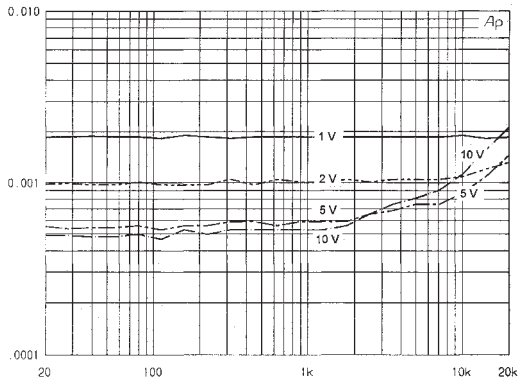

Figure 6-28: Balanced line receiver of Figure 6-25, THD + N versus frequency

The performance of the Figure 6-26 circuit for similar input drive and power supply conditions is shown in Figure 6-29, and for conditions of 600 Ω loading. These data indicate less loading and frequency dependence, due primarily to the OP275's higher slew rate, and greater available output drive into 600 Ω loads.

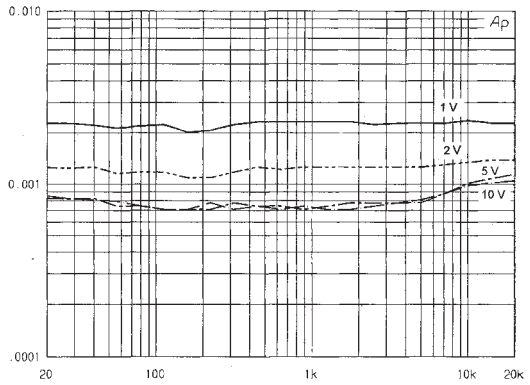

Figure 6-29: Balanced line receiver of Figure 6-26, THD + N versus frequency

In the all-inverting circuit of Figure 6-26, THD + N performance is much more limited by noise than actual distortion, over frequency. The circuit is a very flexible one, and can be set up for a variety of other op amps and input resistances, as well as the already mentioned single-resistor gain change operation.

The line receivers covered above offer good performance. However, with input resistances on the order of 25 kΩ, they can still be subject to CM errors due to driver impedance mismatches. This is not an issue that can be dealt with cleanly, as the designer of a line receiver circuit doesn't necessarily have any preknowledge of the worst-case driver impedance characteristics. So, to guarantee high CMR performance even in the instance of substantial driver impedance and/or mismatching, there are two possible solutions. One is to make the line receiver circuit input impedance as high as practical, which then allows good CM performance with impedance mismatches on the order of 10% (Figure 6-22). Alternately, a line receiver can utilize a line transformer, which offers high CM rejection and galvanic isolation. Both approaches are discussed next.

A Buffered Input Balanced Line Receiver

The circuit of Figure 6-30 represents an example of a classic three-op-amp instrumentation amplifier (in amp) topology, dressed up and optimized for use as an audio line receiver (see Reference 16). The use of FET input stage buffers in amplifiers U1A and U1B allows megohm-level bias resistance to be used for R_{IN1} and R_{IN2}, which greatly desensitizes this receiver against loading of the source and CM errors. Optional resistor R_{IN3} terminates the line differentially. Protection resistors R_{P1} and R_{P2} allow over-voltages at the two inputs, by limiting amplifier fault currents to safe levels. The input stage can use either dual or single amplifiers, with performance options described below.

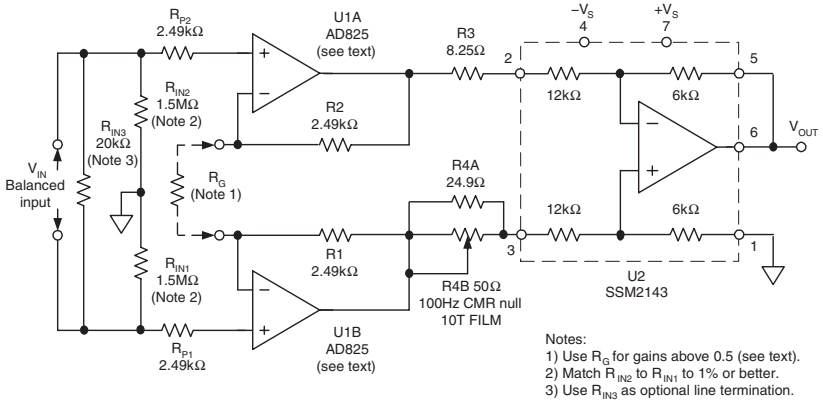

Figure 6-30: A buffered input balanced line receiver

Within the circuit, the *differential* gain of stage U1A, U1B (or G_1) is set by R_1-R_2-R_G, as:

$$G1 = 1 + \left[(2R_1) / R_G \right] \qquad \text{Eq. 6-16}$$

where $R_1 = R_2$, and R_G is used for high gains. Without R_G, the first stage gain is unity.

While the differential gain of U1 is as noted, the CM gain is unity, since the connection simply passes CM signals to the output. Thus both differential and CM forms of signal are presented to the inputs of stage U2. Note, however, because differential and CM signals are scaled differently by U1, there can be a net potential gain in CMR. Practically, it means that this overall configuration can achieve useful CMR figures higher than the intrinsic CMR of U2, whatever that figure may be.

The U2 stage, a pre-trimmed 4 resistor in amp, suppresses the CM component from U1A/U1B, while amplifying differential signals by a factor of 1/2. For an overall net gain G higher than 0.5 from this line receiver, the value of R_G is:

$$R_G - R_1 / (G = 0.5) \qquad \text{Eq. 6-17}$$

For net overall gains of 1, 2 and 4 times, the required gain resistance R_G works out to be 4.99 kΩ, 1.69 kΩ, and 715 Ω, respectively (using closest standard values).

Seasoned analog designers may wonder what's so new about this circuit, as it has been around for more than 30 years in solid-state form (Reference 9). While true, some refinements here lend it worthwhile audio utility. First, as mentioned, FET input op amps for the U1 stages allow very low bias current, and load the inputs infinitesimally. Source loading will be essentially determined by the 1% resistances used for R_{IN1} and R_{IN2}.

While FET amplifiers are most useful here, a serious selection caveat is in order. The types used for U1A and U1B must *not* be general-purpose types prone to sign-reversal, which could possibly come about with

combined large signal and CM inputs (see Chapter 7 overvoltage discussions). All of the types tested for Figure 6-30 have FET input stages, with CM ranges of at least ±10 V on ±15 V supplies. Note that any op amp can mis-behave if severely overdriven at the input (i.e., beyond the rails). Of the three types tested, the AD825 is the most robust for overload, while the AD845 is less robust, but offers best CM performance. Wideband operation is a virtue, allowing better high frequency performance before degradation sets in. Finally, an FET input structure is less susceptible to RF rectification problems, which can be critically important in an audio line receiver used within an RF environment (see Chapter 7 RFI discussions).

Selection of the U2 device also has a great bearing on CMR. Although there are a number of unity gain 4 resistor in-amps available for the U2 function, the choice here is for less than unity gain (in this case 0.5). To extract the highest possible CMR performance, the U2 network balance is externally trimmed by the R_3-R_4 resistances. R_{4B} can be either the film trimmer noted, or a selected fixed resistor. The values shown allow a trim range of more than ±0.05%, sufficient to trim any SSM2143 part to a null. In the performance data following, the SSM2143 used for U2 reflected such a trim, with a basic low frequency CMR of ~110 dB for the stage.

Buffered Input Balanced Line Receiver Performance

To demonstrate these concepts, a number of measurements were made on the Figure 6-30 circuit, using a number of single and dual IC op amps for the U1A and B positions, and an SSM2143 for U2. Although this basic 3 amplifier in amp structure can in principle offer potential gains in CM performance over the intrinsic CMR of U2, this phenomenon is less pronounced at relatively low overall gains as true here (i.e., gains of 1, 2, or 4 times). And, it is also dependent upon the specific U1 and U2 performance. Thus the CMR of both the U1 and U2 stage devices can effect the measured CM performance.

The test setup used employs an Audio Precision System 1 in a modified crosstalk test mode, where channel A drives the test circuit, which in turn has its output monitored by channel B. This allows a swept narrow band tracking analysis, over a dynamic range of 130 dB or more at low frequencies, and a frequency range of 20 Hz to 200 kHz. In the results following, the CM error curves displayed are referenced to a 0 dB calibrated output level from U2 of 1 V rms, with the circuit set for a gain of 0.5 (i.e., R_G open). The drive to the circuit was 2 V rms, and power supplies were ±13 V.

Figure 6-31 shows CM error results for paired (2) single samples of the AD825, the AD845, and the dual AD823. All devices have CM errors at or below a –90 dB level below 3 kHz, with low frequency errors of the AD845s well below –100 dB. The CM corner for all devices is enough to achieve –80 dB or better 20 kHz CM error.

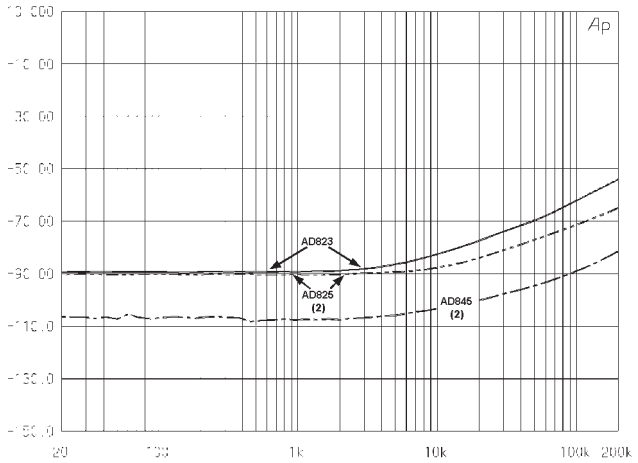

Figure 6-31: CM error (dB) versus frequency (Hz), for various U1A and U1B devices within the circuit of Figure 6-30, gain = 0.5.

While these results show generally what the various devices can do in this circuit, the data should not be taken as an absolute indication of future results. Sample-sample variations of a few dB will exist, and this should be taken into account. One point worth noting, however, is that devices with intrinsically high CMR input stages perform best. An example of this is the AD845, which uses cascode inputs for high CMR, and shows a CMR of 100 dB or more to above 20 kHz. It does however have less input dynamic range than the AD823 and AD825, because of the bias headroom required for the cascode stage.

A criticism directed towards active line receiver circuits such as the SSM2141 and SSM2143 has been their high sensitivity to source resistance mismatches. However, as the discussions above have shown, the problem comes from the relative source/load impedances, and the degree by which these are mismatched. One can specify a very well-controlled, high CMR receiver, such as, for example, the SSM2141 or SSM2143, and have the as-used CMR degrade simply due to uncontrolled source impedance(s).

In the relatively uncontrolled environment of real-world audio system interfacing, source resistance mismatches of a few ohms can be typical. This mismatch level is sufficient to ruin the CMR performance of a simple line receiver, if the receiver uses resistances on the order of 20 k, and is fed from a source resistance of 50 Ω or more. This can be readily illustrated by a sample calculation using the bridge circuit CMR relationship of Eq. 6-12, and plugging in R_{OUT} resistances of 50 Ω and 55 Ω (a 10% mismatch), using an R_{IN} resistance of 20 kΩ. This degree of mismatch for 20 kΩ loading conditions destroys CMR, as it degrades to 72 dB with a 50 Ω source mismatched 10% (see Figure 6-22).

The buffered topology of Figure 6-30 directly addresses this issue, as shown in the dual matched/mismatched source resistance CM plots of Figure 6-32. In these tests, the Figure 6-30 circuit is again exercised with the AD825 and AD845 op amp paired samples at an overall gain of 0.5, and R_{IN3} = 20 kΩ. The circuit is fed from a source resistance of 50 Ω, and is operated under both matched and mismatched source resis-

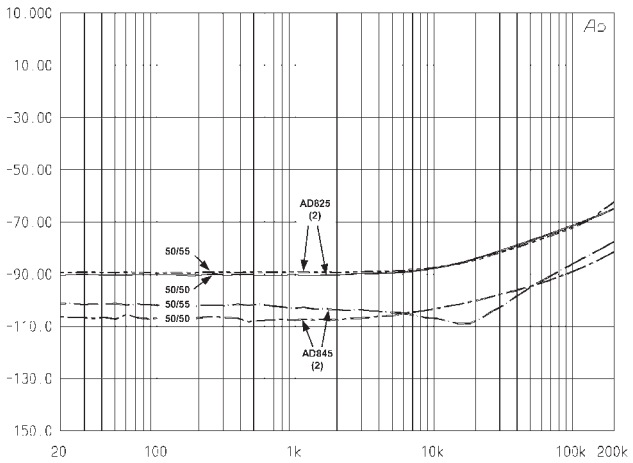

Figure 6-32: CM error (dB) versus frequency (Hz), for AD825 and AD845 pairs, nominally 50 Ω source impedances matched/mismatched 10%

tance conditions. This allows the degradation with mismatching to be clearly shown as separation between the 50/50 (matched) and 50/55 (mismatched) paired curves for each device type.

In the AD825 pair curves, the CM degradation is less than 1 dB, even for the test condition of the relatively high 10% source resistance mismatch. The AD845 device has better overall CMR than the AD825, which shows up as low frequency errors of better than –100 dB with the matched impedances. While mis-matching degrades CMR by a few dB, it is still –100 dB or below as high as 20 kHz. The AD845 can be used for U1A and U1B in the Figure 6-30 circuit for highest wideband CMR (do, however, be careful to note the device dynamic range limits). Considering its superior overload behavior, the AD825 is the best choice, and is thus recommended.

These tests make clear that higher R_{IN} aids in desensitizing system CMR degradation against source mismatching. The designer has the option of using even higher input resistance for R_{IN1} and R_{IN2}, to further reduce the source sensitivity.

Transformer-Input Line Receiver

The classic solution to the CM isolation of audio signals is the *line input* transformer (see References 4,5). This device, usually a 1:1 ratio unit, offers galvanic isolation and very high CM voltage breakdown ratings. It is a preferred (or only) solution where true galvanic isolation is a necessity. Transformers are also useful for high and consistent low to middle audio frequency CM performance, both from unit-unit, and also when high immunity to varying differential source resistance is sought. These features do come at some cost however. Quality transformers are pricey, at about 10–20 times a single IC's cost. They also occupy a relatively large package size vis-à-vis a solid-state equivalent.

All of the various factors above are the designer's ultimate decision points, dependent upon the exact system requirements. When optimized for high performance, it is not likely that either a completely solid-state or a completely transformer-based line receiver solution will be considered either simple, or low in cost. Performance comes with a price.

Interestingly, when a near-ultimate in low frequency CM rejection is required, or completely tweak-free operation is sought, a hybrid line receiver solution may be a good choice. An example of a line transformer buffered by a simple line receiver is shown in Figure 6-33. This circuit combines good features of the simple line receiver and the transformer, and offers outstanding performance with attractive simplicity.

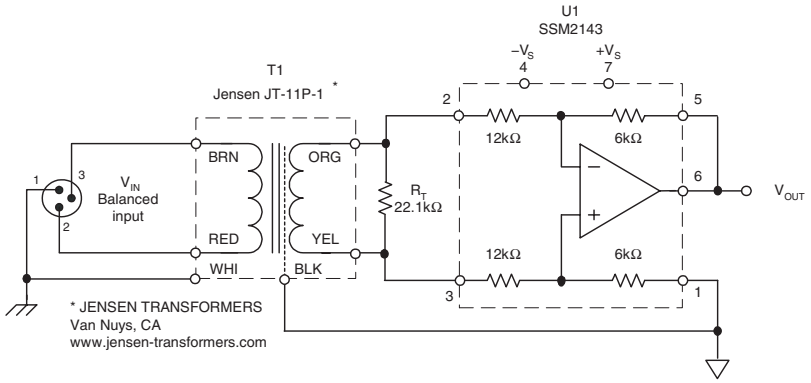

Figure 6-33: A transformer-input line receiver circuit

The circuit has only three components; T1, the secondary termination resistor, and U1. It can be noted that this combination can operate the transformer in either a balanced mode (just as shown) or in an alternate single-ended mode (with U1-2 grounded). The choice of which mode is used does make a big CMR performance difference, as will be apparent. The transformer secondary is terminated in a net 10 kΩ resistance, which here is comprised of R_T and the 12 kΩ input resistances of U1. If other forms of termination are used, or an alternate U1 part, R_T should be adjusted accordingly (see Reference 17). The net gain of the circuit is product of the loaded transformer primary/secondary voltage ratio, and the voltage gain of U1 (0.5). Inasmuch as T1 shows a voltage loss for such loaded conditions, the overall gain of the circuit is approximately 0.35 (or –9 dB). If more gain is desired, an alternate SSM2143 operational mode is possible. The 12 kΩ/6 kΩ input output resistors can be reversed, which will then allow it to operate at a gain of 2.

The CMR test results for the circuit of Figure 6-33 are shown in Figure 6.34. Conditions for this test setup are similar to those of the buffered balanced line receiver test, described above. They are referenced to a 1 V operating level at the output of U1.

Several important points should be apparent from these results. In the single-ended mode (upper curve), the basic data sheet performance of the JT-11P-1 transformer can be seen. This includes an approximate 60 Hz CM error of –107 dB. While this simply buffered operating mode does offers excellent low frequency CMR, it can also be noted that this also degrades with rising frequency. At 20 kHz the single-ended mode error is just slightly more than –50 dB—good, but not superlative. Any of the ICs tested for the Figure 6-30 circuit better this performance, by about 30 dB or more.

On the other hand, by simply letting the SSM2143 operate in a balanced mode, the lower curve CMR performance results. This is clearly a major improvement vis-à-vis the single-ended case, with the low frequency CM error reduced to –130 dB or better, approaching the noise floor of the instrumentation. The errors aren't quite as low at the higher frequencies, with a 20 kHz CMR of ~60 dB.

A point worth noting is the transformer-based line receiver cannot really compete with the buffered balanced receiver of Figure 6-30 for high frequency CMR. This is because the transformer interwinding

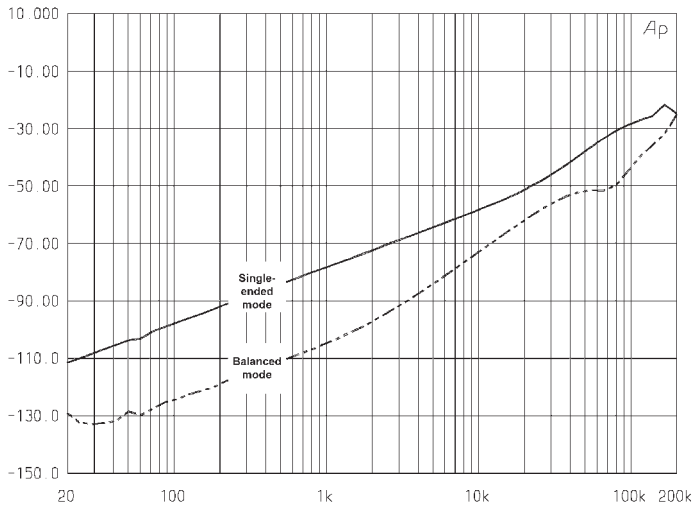

Figure 6-34: CMR errors for Figure 6-33 transformer-input line receiver circuit, operating in single-ended and balanced modes

capacitance acts as a high-pass filter for CM noise. This has the effect of passing CM noise to the output at the higher frequencies. The degree of severity for this phenomenon will of course vary with the design of the specific transformer.

Nevertheless, it is readily apparent from the performance data that the preferred method of transformer operation is to operate it in a balanced secondary mode (i.e., as shown in Figure 6-33), which does mitigate the CMR loss with frequency somewhat.

A Summary of Line Receivers

Both active and passive solutions for minimizing balanced transmission system CM noise have been explored, each with their own set of characteristics. Readers should take these data for the general trends they convey, not any absolute performance levels.

To summarize, the buffered balanced line receiver of Figure 6-30 offers excellent broadband CMR with low differential source resistance sensitivity, and can be user-customized in a variety of ways, including gain, CM input impedance, and so forth. The solid-state line receiver approach here has virtues of the best high frequency CMR in absolute terms, as well as the better CMR versus frequency flatness. While the example circuit shown works well, optimization for a production role may need some enhancement for worst-case minimum CMR. This can be done via careful trim or selection of the U2 circuit, and/or selection of an optimum pair of singles for U1A and U1B. Input dynamic range of the circuit can be optimized by selection of the U1A-U1B pair types, and the supply voltages used. All types tested can be operated at supplies of up to ±18 V (maximum), or as low as ±13 V. The typically used ±15 V supplies will provide both excellent performance and high input dynamic range.

The transformer-input approach to a line receiver offers good to superlative low frequency CMR, combined with “no tweak” operation. When the transformer used is combined with an in amp for balanced mode secondary buffering, as in Figure 6-33, further CMR reduction is possible over a range of low to middle frequencies. On the downside, there are negatives of cost, size, and eventual CMR degradation with frequency.

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Audio Buffers and Line Drivers

Audio line drivers and buffer amplifiers can take on a wide variety of forms. These include both single-ended and differential output drivers, as well as transformer isolated drivers. Within these general formats there are also many different performance options, and many of these are covered in this section. Note that a later section of this chapter also discusses buffers for a general context, as for video and instrumentation applications.

Many op amps useful as video drivers and/or buffers do well for audio drivers/buffers, because of the high current output stages necessary for good linearity over video bandwidths (see References 1–4). Some examples of video IC amplifiers that are audio-useful are the AD810, AD811 and AD812, AD815, AD817 and AD826, AD818, AD829, AD845, and AD847. Other types notable for either high or unusually linear output drives or other performance features useful towards audio are the AD797 and the OP275.

Some High Current Buffer Basics

As a preliminary to detailed application discussions, some basic circuit principles germane to high current buffers and drivers should be treated first. With output currents up to 100 mA or more, "housekeeping" details of bypassing, grounding and wiring also become important, and must be considered to achieve high performance. These are briefly discussed here in the context of high current audio buffers, using the unity gain buffer circuit of Figure 6-35, as a point of departure.

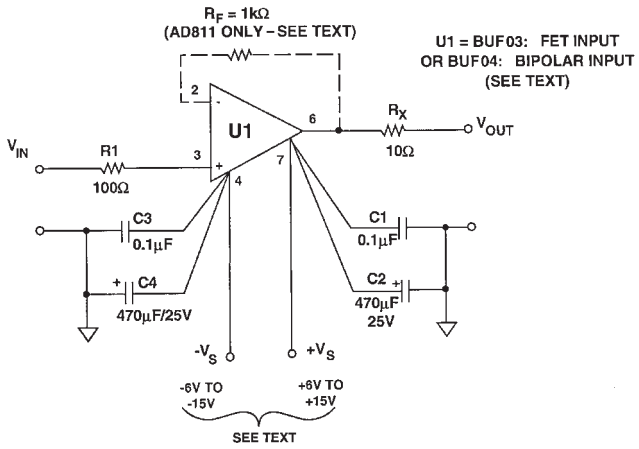


Figure 6-35: A unity-gain, standalone buffer circuit

First, despite which IC is used for U1, close attention should be given to making buffer stages free from parasitic effects, at both input, output, and supplies. Physical construction of buffer-drivers and other high current stages should be in accordance with high speed rules. A heavy copper ground plane is preferred, and circuit layout should be compact, with low capacitance high-Z nodes. Signal and ground runs should be laid out with signal coupling and load current flow in mind (see References 5–7 and Chapter 7).

In addition, the power supplies should be well bypassed close to the high current supply pins. In Figure 6-35 this is indicated by the Kelvin connections of C_1–C_4 to the U1 ±Vs pins. This should be used as standard practice for all high current stages, and is intended as a given for all the driver applications of this section.

As a minimum, local low inductance/low ESR RF bypass caps should used within 0.25" of the device supply pins, shown as C_1 and C_3. These are preferably 0.1 μF stacked polyester film, or other low inductance

capacitor type, preferably films. In addition, for high peak current loads, the high frequency bypasses are paralleled by local, short lead/large value, low ESR electrolytics such as C_2 and C_4, in a range of 470 µF/25 V and up. Note that capacitor ESR reduces in inverse proportion to electrical size and voltage rating, so larger size and/or voltage units help. These capacitors carry transient output currents, and should be aluminum electrolytic types rated for high frequency use, that is switching supply types. Such types tend to have a broad range of lowest high frequency minimum impedance and are thus less likely to cause power line resonance than are tantalum units.

Dc power management and dissipation can also be important with buffer ICs. For example, the BUF03 and the AD811 ICs can dissipate fairly large power levels even with light loading, for supplies above ±12 V. This is because the quiescent current of these devices is 15 mA–18 mA, relatively independent of operating voltage.

As a conservative general rule of reliability, any IC with a power dissipation above 300 mW should not be used without a heat sink. For buffer or driver circuits using this power or more, use the lowest thermal resistance package possible, and add the appropriate heatsink (Thermalloy 2227 for the BUF03 or other TO-99 ICs, or Aavid #5801 for the BUF04, AD811 or other high dissipation 8-pin DIP ICs).

Output resistor R_X in this circuit should be 10 Ω or more, to isolate the buffer from capacitive loading (more on this elsewhere in this chapter). For an extra safety margin against possible destabilization due to capacitive loads, make this resistor as high as feasible from a voltage loss point of view.

The input resistor R_1 is a "bullet-proof" safety item, and can serve two purposes. One is as a parasitic suppression device, which may be required for stability with some amplifiers (not absolutely essential for those here). A subtler feature of this resistance comes about when the buffer is operated within a feedback loop, and is driven from an op amp output. Internally, many buffer ICs have clamping diodes from input to output, and under overload conditions, these diodes act to clamp overdrive. With the inclusion of R_1, this prevents excess current drive into the buffer IC under this clamping condition.

Because of this stage's very high bandwidth, low phase shift, and low output impedance, fast buffers such as this can be used both "stand alone" just as shown, or as a more conventional "in loop" buffer as well, to minimize loading of a weaker, slower amplifier. The improvement raises the linear output up to ±100 mA with the AD811 or the BUF04, while maximizing linearity, preserving gain, and lowering distortion.

Buffer THD + N Performance

Operating in a pure standalone mode, THD + N tests on several unity gain buffers are shown in Figure 6-36. These tests were for common conditions of 10 V rms output into a 600 Ω load, operating from ±18 V power supplies.

The BUF03, an open-loop design, shows a distortion for these conditions of about 0.15%. The BUF04, a closed-loop current feedback design buffer, shows a very low distortion of about 0.004%. The AD811 is also a current feedback amplifier, but it is externally configured as a unity gain follower, with R_F = 1 kΩ. Note that *all current feedback ICs will require such a resistor*, but the value required may vary part to part. The AD811 shows an intermediate distortion level, under 0.01%.

As a choice among these types, both the BUF04 and AD811 are capable of more than ±100 mA of output, with input currents on the order of 1 µA–2 µA. The BUF03 has a lower output current (±70 mA), but the advantage of a much lower input current (~200 pA).

Dual Amplifier Buffers

In addition to standard operation of the various single op amps as unity-gain buffers, certain high output current *dual* op amp ICs also work exceedingly well as buffers. Using a dual IC to buffer a signal has the advantage of doubling the output drive while using basically the same package size, an obvious benefit.

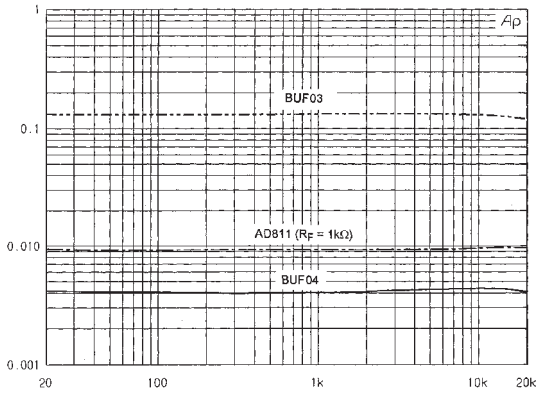


Figure 6-36: THD + N (%) versus frequency (Hz) for various buffer ICs, for V_{OUT} = V_{IN} = 10 V rms, R_{LOAD} = 600 Ω, V_S ±18 V

Two design steps allow this to be successfully implemented. The first is the selection of a basically linear single device that also is available as a dual. The second is to devise a method of combining the outputs of the two op amps in a linear fashion, without any side effects.

Among the suitable candidates for this task are the dual version of the AD817, the AD826, as well as the AD811 dual, the AD812. Figure 6-37 shows a hookup that is useful towards increasing buffer output current to more than 100 mA.

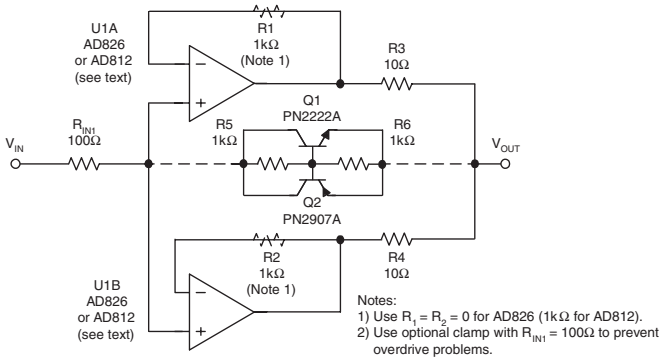


Figure 6-37: Dual op amp buffer circuit raises output current to more than 100 mA with low distortion

Ignoring Q1-Q2 for the moment, the circuit can be seen as a pair of unity-gain followers paralleled at the output, through small value resistors R_3 and R_4. These resistors provide balanced drive from the U1A and B sections, linearly combining the signals. With the use of the voltage feedback AD826 op amp, the circuit is quite simple, since R_1 and R_2 reduce to zero. If the AD812 current feedback device is used, these two resistors should be 1 kΩ (shown dotted). The Q1-Q2 bidirectional clamp circuit is optional, and when used can provide protection against input overdrive, and/or adjustable current limiting via R_5.

This circuit offers excellent performance, as shown in Figure 6-38. These THD + N plots show performance with loads of both 600 Ω and 150 Ω, at an output level of 10 Vrms, from ±18 V supplies (without clamping active). The AD826 offers the lowest distortion, due to the voltage feedback architecture, with less than 0.01% THD + N, even when driving 150 Ω, which is an approximate 100 mA combined peak output.

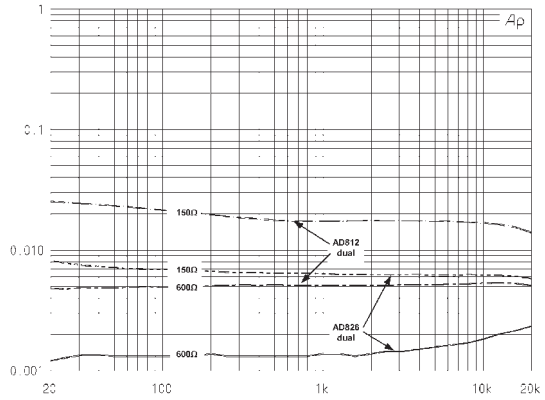


Figure 6-38: THD + N (%) versus frequency (Hz) for AD826 and AD812 dual buffer ICs, for $V_{OUT} = V_{IN}$ = 10 V rms, R_{LOAD} = 150 Ω/600 Ω, V_S ±18 V

Capacitive Loading Issues

Audio driver output stages are typically operated as voltage sources feeding high impedance loads. When connected via long transmission lines between stages, the result is that the driver sees an unterminated line, which can appear highly capacitive. Audio driver stability with capacitive loading can be a difficult design issue, but for good reason—it isn't always an easy thing to achieve. If easy, it may be at the expense of performance or circuit complexity. Fortunately, some standard techniques exist for stabilizing op amp drivers with capacitive loads, and these can be implemented in a reasonably direct fashion. These are covered in detail within the next section of this chapter. The discussions immediately following emphasize driver linearity.

Op Amp Device/Topology Related Distortions

Single-ended audio drivers can be built using a linear, noninverting gain stage as a starting point. Indeed such a circuit, given appropriate op amp choice and gain scaling, can well serve as a basic audio driver. Topologically, a noninverting gain stage is preferable, since it loads the signal source less, and, it also adds no sign inversion. However, this configuration is subject to certain distortions, which should be understood in order to extract the best performance in an application. Distortion performance for a number of audio op amps in such a line driver circuit are now discussed, in this context.

The circuit of Figure 6-39 is a test configuration that loads the U.U.T. op amp with 500 Ω and 1 nF. This is a reasonably stressful test load, which can differentiate the distortion of various devices with outputs of 7 V rms or more. A gain of 2 is used, which subjects the U.U.T. to a relatively high input CM voltage, thus this configuration is sensitive to CM distortion in the amplifier. For the following tests of this section (except as noted to the contrary), V_S = ±18 V, and the analyzer bandwidth is 10 Hz–80 kHz.

Given amplifiers with sufficient load drive and output stage linearity in this circuit, there can still be nonlinear effects due to the CM voltage. This distortion is due to the nonlinear C-V characteristic seen at the

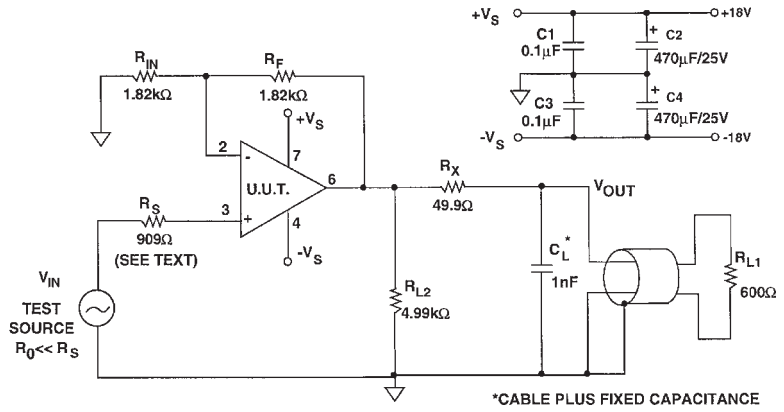


Figure 6-39: Test circuit for audio line driver amplifiers

two amplifier inputs, and can be minimized by matching the two impedances seen at the respective (+) and (–) inputs (see Reference 8). When this is done, the differential component of the error is minimized, and the distortion seen in V_{OUT} falls to a minimum.

This general point is illustrated by Figure 6-40, a family of plots for an OP275 op amp within the circuit of Figure 6-39. The OP275 use junction FET devices in the input stage, which have appreciable (nonlinear) capacitance to the substrate. The test is done with various values of source resistance R_S. As noted, distortion is lowest when R_S is equal to the parallel equivalent of R_F and R_{IN} or, in this case, about 910 Ω. For either higher or lower values of R_S, distortion rises. Appreciably higher source impedance (10 kΩ) can cause the distortion to rise lower in frequency, making performance much worse overall.

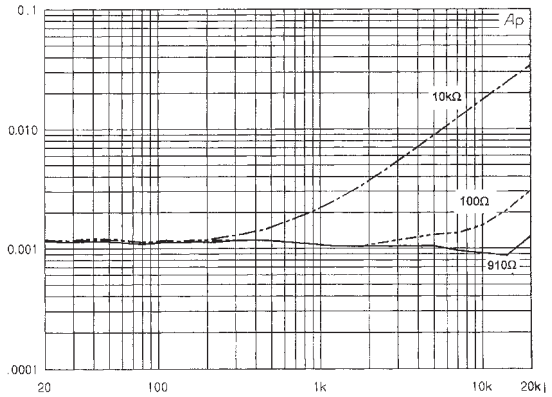


Figure 6-40: Follower mode R_S sensitivity of OP275 bipolar/JFET input op amp THD + N (%) versus frequency (Hz), V_{OUT} = 7 V rms, R_L = 500 Ω, V_S = ±18 V

It is therefore suggested that, whenever possible, amplifiers operated as voltage followers should have their source impedances balanced for lowest distortion. Note that the OP275 device is just one example, and its sensitivity to CM distortion effects is not at all unique in this regard.

While the balancing of the two source impedances is most helpful, *lowering the absolute value* can also minimize this distortion. With R_S low, this has the effect of moving the high frequency breakpoint of the distortion rise upwards in the spectrum, were it is less likely to be harmful. The best overall control of this distortion mechanism with an amplifier subject to it is the use of the lowest practical, balanced source impedances.

It is important to understand that virtually all IC op amps, *particularly those using JFET inputs*, as well as discrete JFET and bipolar transistors are subject to nonlinear C-V effects, to some degree. In the tests of other amplifiers within the Figure 6-39 circuit, R_S was maintained at 910 Ω, to minimize the effects of this distortion mechanism.

With high output, high slew rate linear amplifiers, the distortion generated for these test conditions can parallel that of the test equipment residual, as shown in Figure 6-41. Here the AD817, AD818 and AD845 amplifiers show THD + N which is essentially equal to the residual for these conditions, and appreciably below 0.001%.

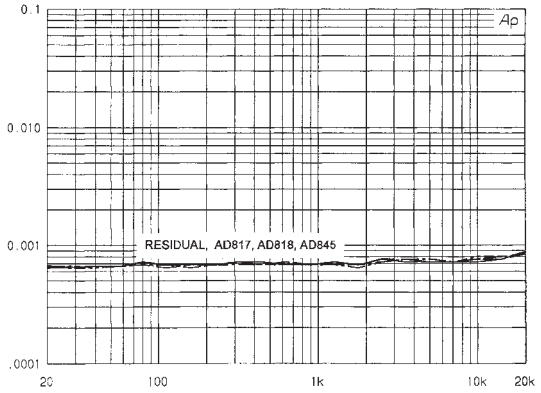


Figure 6-41: A driver group, THD + N (%) versus frequency (Hz), for V_{OUT} = 7 V rms, R_S = 909 Ω, R_L = 500 Ω, V_S = ±18 V

Amplifier types expressly designed for audio use also do well for these THD + N tests, as shown in Figure 6-42. The industry standard 5534 is near or just above the residual level, while the OP275 plot falls just above the 0.001% level and the 5532 is slightly higher.

These tests reflect performance of a variety of single amplifiers, as exercised for matched-source test conditions, with medium output loading of 600 Ω. Varying test conditions may change the absolute levels of performance. So also may different samples, or in the case of industry standard parts, alternate vendors.

The data of Figures 6-41 and 6-42 reflect older (but available) op amp devices capable of very high performance in these tests. Several more recent devices also do well for this driver test. Figure 6-43 shows performance of newer FET input op amps, the AD825, the AD8610 and the AD8065. The AD825 was tested under conditions identical to those of Figure 6-41 and 6-42. The AD8610 and AD8065 were tested under similar conditions, but with ±13 V power supplies, reflecting a lower maximum supply rating.

Note that the latter two amplifiers still can accommodate more than a 7 V rms output swing, even with the reduced supplies. Under these conditions, the AD8065 distortion is near the test set residual and the AD8610 slightly higher at high frequencies. The AD825 has somewhat higher distortion, but this is almost frequency-independent.

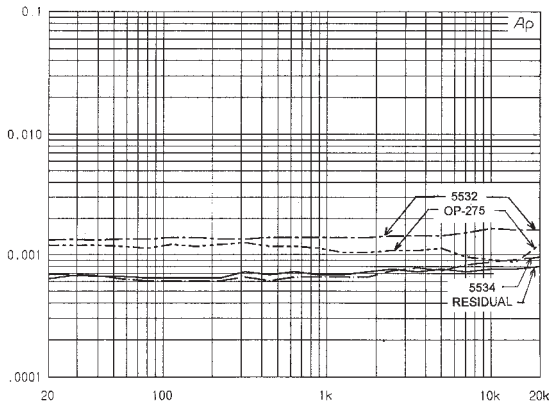


Figure 6-42: B driver group, THD + N (%) versus frequency (Hz), for V_{OUT} = 7 V rms, R_S = 909 Ω, R_L = 500Ω, V_S = ±18 V

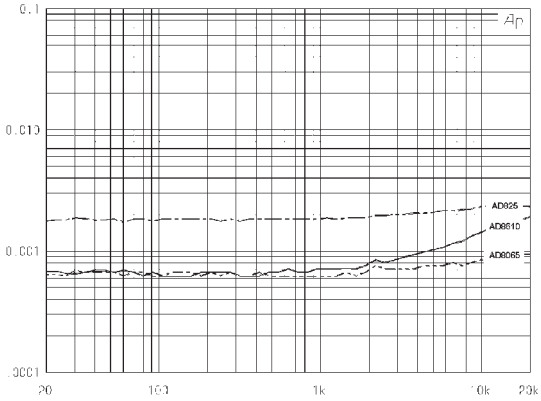


Figure 6-43: C driver group, THD + N (%) versus frequency (Hz), for V_{OUT} = 7 V rms, R_S = 909 Ω, R_L = 500 Ω, V_S = ±13 V or ±18 V

Single-Ended Line Drivers

This section discusses a variety of line driver circuit examples that drive single-ended lines, optimized for different operating environments, supply voltages, and performance.

Consumer Equipment Line Driver

One common driver application is a line output stage for consumer preamps, CD, and DVD players, and so forth. This is typically an economical audio stage with a nominal gain of 5 to 10 times, operating from supplies of ±10 V to ±18 V, usually with a rated output of 2 V rms–3 V rms, and a capability of driving loads of 10 kΩ or more.

For simplicity of biasing and minimum output dc offset, ac-coupling is used, and the circuit is typically fed from a volume control. For stereo operation, a dual channel device is typically sought for this type application, one which is also optimized for audio uses.

Such a stage is shown in Figure 6-44, and uses an OP275 dual op amp as the gain element. In this circuit input and feedback resistors R_1 and R_3 are set equal, which makes the nominal dc bias at U1's output close to zero. The U1 bias current flowing in these resistors also serves to polarize coupling capacitors C_1 and C_2 positively, as noted.

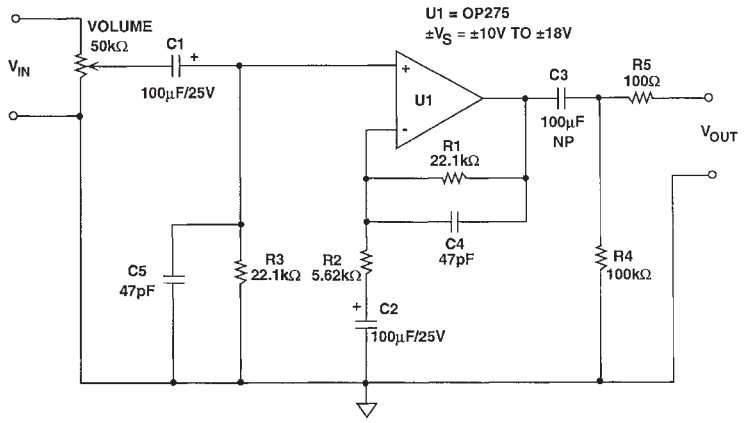


Figure 6-44: Consumer equipment line driver stage

This bias is due to the sign of the OP275's PNP input stage bias currents, so reverse C_1-C_2 if an NPN input amplifier is used.

R_2 sets the gain of the stage in conjunction with R_1. The stage gain is nominally five times for the values shown. C_2 sets the low frequency roll-off along with R_2, which in this case is ≈0.3 Hz. Although this frequency is quite low, it does allow some range of gain increase if desired, simply by lowering R_2. Output capacitor C_3 must be nonpolarized, since the worst-case dc at the output of U1 is ≤10 mV (and can be bipolar). Typically it will be about one-quarter this, so if a few mV can be tolerated, C_3 can be eliminated.

THD + N performance of the stage (not shown) was measured for outputs of 1 V rms–3 Vrms into a 10 kΩ/600 pF load, using ±18 V supplies with an R_S of 1 kΩ. At lower output levels performance is noise limited, measuring less than 0.002%. At the 3 V output level a slight increase in high frequency distortion is noted. Although this application is an example where the amplifier ± source impedances cannot be matched (due to the variations of the volume control), nevertheless the performance is still quite good.

Noise is the limiting factor for lower level signals so, if lower noise is desired, R_2 can be reduced. The ultimate practical limit to noise is the volume control's finite output impedance. This causes higher noise at positions of high output resistance, interacting with the noise current from U1. For example if the effective R_S from the volume control is 10 kΩ, a $1.2\ \text{pA}/\sqrt{\text{Hz}}$ noise current from U1 will produce an input referred $12\ \text{nV}/\sqrt{\text{Hz}}$ noise voltage, from this source alone. The Figure 6-44 driver is a flexible one, and operates at supplies as low as ±10 V with outputs up to 3 V rms, with slight distortion increases. With ±5 V supplies up to 2 V rms is available, with higher distortion (but still ≤0.01%).

Paralleled Output Line Driver

Often a modest increase in output may be needed for a driver, but circumstances may not warrant the use of additional buffer devices. Figure 6-45 shows how a second section of a dual op amp can be used to provide additional load drive.

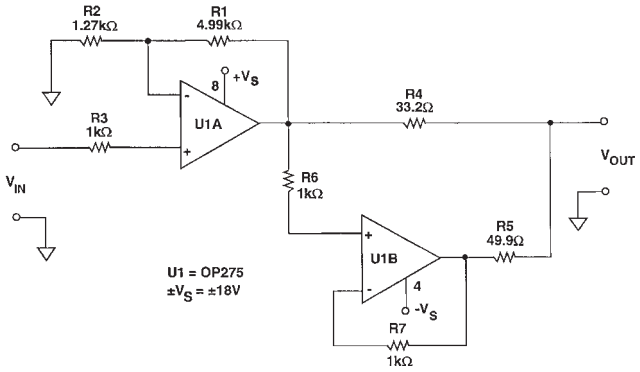


Figure 6-45: Paralleled output dual op amp line driver

In this circuit, using an OP275 dual op amp, the U1A section is a gain-of-five voltage amplifier, while the U1B section is a voltage follower, used simply to provide additional current to the load. Current sharing is determined by output summer resistors R_4 and R_5, and the parallel stage drives 600 Ω loads with less distortion than a single OP275 section.

THD + N performance data is shown in Figure 6-46, with the driver operating from ±18 V supplies, and for output levels of 1, 2, 5, and 9 V rms into 600 Ω.

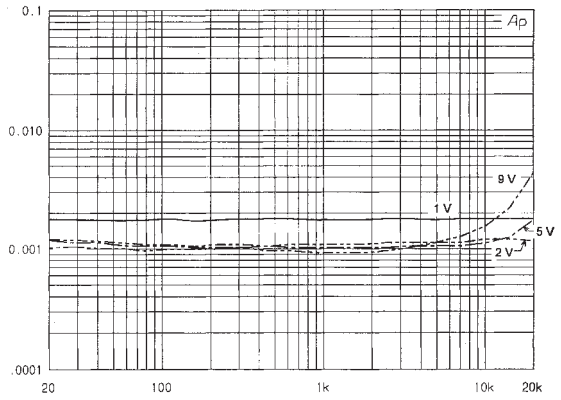


Figure 6-46: Paralleled output dual op amp line driver, THD + N (%) versus frequency (Hz), for V_{OUT} = 1, 2, 5, 9 V rms, R_L = 500 Ω, V_S = ±18 V

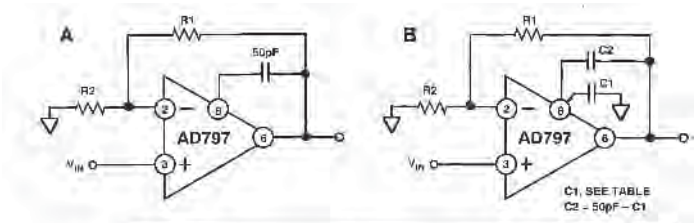
This general scheme can be used with any unity gain stable dual op amp, and also can be adapted for various gain levels, via R_1-R_2. For different devices and/or gains, the ratio of R_4 and R_5 may need adjustment, for lowest distortion into the load.

A Wide Dynamic Range Ultralow Distortion Driver

Single-ended line drivers are simple conceptually, but when pushed to performance limits in dynamic range and distortion, they challenge device choice. The AD797 answers this challenge with its input noise of $\leq 1\ nV/\sqrt{Hz}$ and a distortion canceling output stage. These features allow low and high extremes of dynamic range to be pushed simultaneously.

The AD797 uses a single voltage gain stage, comprised of a folded cascode input combined with a boot strapped current mirror load, allowing the high incremental impedance necessary for a 146 dB gain. This buffered single-stage topology is a departure from past devices using multiple stages, with performance benefits in terms of bandwidth, phase margin, settling time, and input noise (see Reference 9).

For standard uses, the AD797 is employed like any 5-pin op amp, such as shown in Figure 6-47 (neglecting the capacitors for the moment). From the A/B part of the table, relatively low values for resistors R_1-R_2 are recommended for lowest noise. Selecting these resistors should be done with care, since values ≥100 Ω will degrade noise performance. Suggested values for gains of G = 10 – 1000 are noted. The AD797 can drive loads of up to 50 mA, and is rated for distortion driving loads of 600 Ω.



	A / B		A			B		
	R1	R2	C1	C2	3dB	C1	C2	3dB
	Ω	Ω	pF	pF	BW	pF	pF	BW
G=10	909	100	0	50	6 MHz	0	50	6 MHz
G=100	1k	10	0	50	1 MHz	15	33	1.5 MHz
G=1000	10k	10	0	50	110 kHz	33	15	450 kHz

Figure 6-47: Recommended AD797 connections for distortion cancellation and/or bandwidth enhancement

For amplifier applications requiring more top grade performance, optional capacitors C_1 and C_2 can be used. In the Figure 6-47A configuration, superior performance is realized due to distortion cancellation with the use of a single extra capacitor, enabled simply by adding the 50 pF unit as shown. This provides compensation for output stage distortion without effecting the forward gain path, effective over the range of gains noted.

An additional option with the AD797 is the use of *controlled decompensation*, available with the Figure 6-47B option and the use of capacitors C_1, C_2. At gains of 100 or more, adding C_1 as in column B of the table enhances amplifier open loop bandwidth, allowing very high gain-bandwidths to be achieved—150 MHz at G = 100, and 450 MHz at G = 1000. For high gain operation this extra gain-bandwidth can be very effective.

A family of distortion curves for various AD797 gain configurations driving 600 Ω is shown in Figure 6-48. As noted, at low frequencies the data is limited by noise, while at high frequencies distortion is measurable, but still extremely low. The distortion for a gain of 10 times at 20 kHz for example, is on the order of ≈0.0001%, implying a dynamic range of about 120 dB re 3 V rms, or even more for higher level signals.

An additional point worth making at this point is one regarding the AD797's special distortion cancellation ability. Referring to Figure 6-47A, it should be noted that the 50 pF capacitor is connected between Pins 8 and 6 of the AD797. Pin 6 is of course the output of the device for standard hookups. However, in special situations, even greater output current may be required, and a unity gain buffer amplifier can be added between Pin 6 and the load. For example, one of the buffers of Figure 6-36 or 6-37 could be used to extend output current to ≥100 mA.

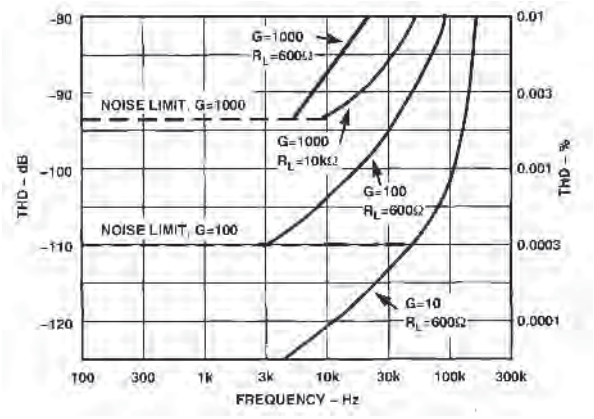


Figure 6-48: THD versus frequency at 3 V rms output for AD797 distortion cancellation and/or bandwidth enhancement circuit of Figure 6-48

The special point worth noting for this situation is that the 50 pF distortion cancellation capacitor should then be connected between the AD797 Pin 8 *and the output of the buffer* (not the AD797 Pin 6). This step allows the distortion correction to be applied not just to the AD797 internal circuits, but also extends it to include the buffer.

A case in point were this would come to useful purpose lies with the AD797 mic preamp, discussed in some detail earlier in the chapter (Figure 6-5). As mentioned therein, a BUF04 would work well as just such a buffered output option for the AD797 preamp. It would be connected as described above, with the 50 pF distortion cancellation capacitor. Details of this are left as a reader exercise (but should even so be obvious).

Current Boosted Buffered Line Drivers

When load drive capability suitable for less than 600 Ω in impedance is required, it is most likely outside the output current and/or linearity rating of even the best op amps. For such cases, a current-boosted (buffered) driver stage can be used, allowing loads down to as low as 150 Ω (or less) to be driven. Another example would a driver for long audio lines, i.e., lines more than several hundred feet in length.

Figure 6-49 is a high quality current-boosted driver example, using an AD845 at U1 as a gain stage and voltage driver, in concert with a unity voltage gain current booster stage, U2. The overall voltage gain is five times as shown, but this is easily modifiable via alternate values for R_1 and R_2. In any case, for lowest CM distortion effects, input resistor R_3 should be set equal to $R^1 \| R_2$ (this assumes a low impedance source for V_{IN}).

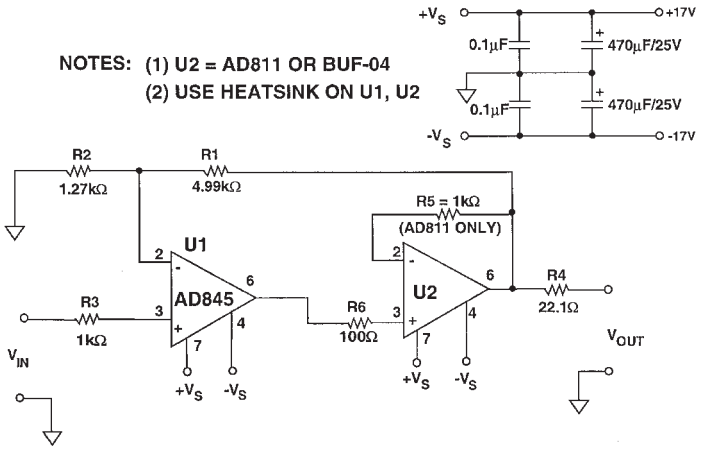


Figure 6-49: Current-boosted line driver

The amplifier used for U2 can be either the AD811 op amp, or the BUF04 buffer for simplicity. If the AD811 or similar CFB op amp is used (AD812, and so forth), it needs to be configured as a follower, with R_5 connected as shown. Since the BUF04 is internally connected as a follower, it doesn't need the R_5 external feedback resistor.

Because of the high internal dissipation of the AD845 and AD811, these devices *must* be used with a heat sink on supplies of ±17 V. However, such high supplies are only justified for extreme outputs. Supplies of ±12 V also work, and will eliminate need for a heat sink (with lower maximum outputs). In any case, power supplies should be well bypassed.

*A special note is applicable here—*Always *observe maximum device breakdown voltage ratings within applications. Production versions of this circuit should use supplies of ±17 V or less, for 36 V(max) rated parts. Similarly, 24 V(max) rated parts should use supplies of ±12 V or less. In all cases, use only enough supply voltage to achieve low distortion at the maximum required output swing.*

For loads of 150Ω, the output series isolation resistor R_4 is lowered to 22.1Ω to minimize power loss, and to allow levels of 7 V rms or more. The THD + N data for this circuit is shown in Figure 6-51, using an AD811 as the U2 buffer. The test conditions are input sweeps resulting in 1, 2, 4 and 8 V rms output, using ±18 V power supplies.

For the AD811 operating as U2, the Figure 6-50 data below shows THD + N dominated by noise and residual distortion at nearly all levels and frequencies driving 150Ω, up to 8 V rms. At this level, a slight distortion rise is noted above 10 kHz, yet it is still ≈0.001%. With the BUF04 as U2 (not shown) THD + N is comparable at lower output levels, but does show a distortion rise with 8 V rms output at high frequencies (yet still below 0.01%).

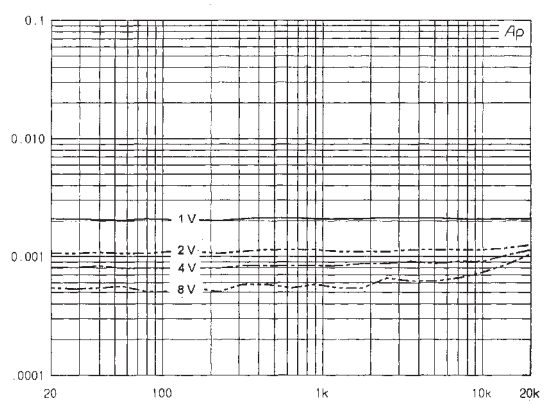


Figure 6-50: Current boosted driver of Figure 6-50 using AD811 as U2, THD + N (%) versus frequency (Hz), for V_{OUT} = 1, 2, 4, 8 V rms, R_L = 150 Ω, V_S = ±18 V

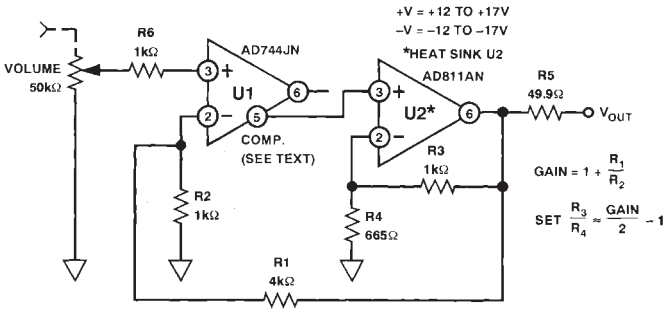


Figure 6-51: Composite current-boosted line driver one

There is a power/performance tradeoff involved with the choice between the two mentioned U2 devices which should be understood. The BUF04 has a standby dissipation of about 200 mW on ±15 V, while the AD811 is more than double this dissipation, at 500 mW. Therefore, while the AD811 does yield the lower distortion, it also should be operated more conservatively from a power standpoint. As noted above, only the minimum (±) supply voltage required to sustain a given output should be used with the circuit in general, and particularly with the AD811 employed at U2.

As for U1 in this circuit, other amplifiers can be used, but only with due caution against poor performance. Quite simply, it is difficult to improve upon the AD845's performance in this application. Three possible candidates would include the "Group C" op amps of Figure 6-43, operating on suitable power supplies;

±17 V or less for the AD825, and ±12 V or less for the AD8610 and AD8065. Of these, the AD8065 would seem to hold the greatest promise, having shown the lowest wideband distortion in the Figure 6-43 tests.

As considered within the buffered driver circuit of Figure 6-50, however, the AD8065 will be operated in an even more linear fashion; that is, it is operating essentially unloaded at the output. This is a key factor towards highest performance, as it moves the burden of linear load drive to the buffer stage. Further variations of this circuit technique will be reprised later, within other driver applications to be discussed.

Composite Current-Boosted Drivers

Another useful current-boosted circuit technique combines the positive aspects of two different amplifiers into a single composite amp structure, producing a very high performance line driver (see References 10–13 for several variations of this basic circuit). With an FET input IC used as the input stage, dc offset change from source resistance variations of a typical volume control of ≈50 kΩ is nil, allowing total direct coupling. As previously noted, with a high current, wideband booster output stage, line impedances down to 150 Ω can be driven with excellent linearity.

This type of composite amplifier allows good features of two dissimilar ICs to be exploited; each optimized for the respective input and output tasks. Figure 6-51 shows a low distortion composite amplifier using two-op-amp ICs with such performance.

A factor here aiding performance is that the U1 AD744 stage operates unloaded, and also that the AD744's compensation pin (5) drives U2. This step (unique to the AD744) removes any possibilities of U1 class AB output stage distortion. Another key point is that the overall gain bandwidth and SR of U1 are boosted by a factor equal to the voltage gain of U2, an AD811 op amp, which itself operates at a voltage gain. These factors enhance this circuit by providing both high and linear load current capability, providing a composite equivalent of an FET input power op amp.

This design operates at an *overall* voltage gain set by R_1 and R_2 (just as a conventional noninverting amplifier) which in this case is five times. Since the circuit also uses a local loop around stage U2, the R_3/R_4 ratio setting the U2 stage gain should be selected as noted. This complements the overall gain set by R_1 and R_2, and optimizes loop stability.

Also note that the U2's feedback resistor R_3 has a preferred minimum value for stability purposes (again, as is unique to CFB amplifier types). Here with the AD811, a 1 kΩ value suffices, so this value is fixed. R_4 is then chosen for the required U2 stage gain. Further design details are contained in the original references (see References 2 and 10).

The composite amplifier performance for a typical audio load of 600 Ω, THD + N at output levels of 1, 2, 4 and 8 V rms is shown in Figure 6-52, while operating from supplies of ±18 V for this test. The apparent distortion is noise or residual limited at almost all levels, rising just slightly at the higher frequencies.

Lower impedance loads can also be driven with this circuit, down to 150 Ω. Note that for operating supply voltages of more than ±12 V, a clip on heat sink is recommended for U2, as previously discussed for the AD811. Practical versions of this circuit can readily use supplies of ±12 V, and still operate very well.

The circuit of Figure 6-51 is a very flexible one, and can also be adapted in a variety of ways. Although the original version shown uses the AD744 compensation pin (5) to drive the output stage U2 device, conventional internally compensated op amps can also be used for U1, and still realize the many features of the architecture.

The ability to adapt the topology to differing devices in single and dual op amp formats allows such dual FET devices as the AD823 to be usefully employed in a stereo realization. Similarly, dual CFB op amps such as the AD812 can be used in the U2 output stage. Thus a complete stereo version of the circuit can be efficiently built, based on only two IC packages.

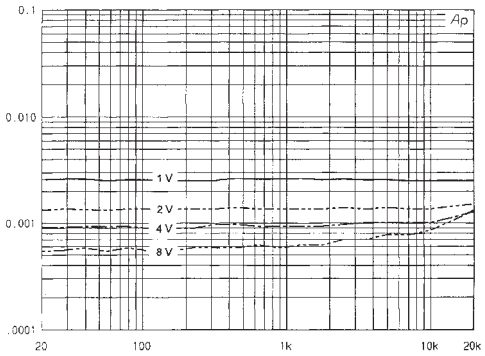


Figure 6-52: Composite current-boosted driver one of Figure 6-51, THD + N (%) versus frequency (Hz), for V_{OUT} = 1, 2, 4, 8 V rms, R_L = 600 Ω, V_S = ±18 V

This topology's flexibility also opens up a diversity of other applications beyond the basic line driver. For example, using a power-packaged dual CFB op amp such as the AD815 for U2, allows very low impedance loads such as headphones to be driven, down to as low as 10 Ω (see Reference 12).

The composite current-boosted line driver two, shown in Figure 6-53, summarizes a number of the above-mentioned options, and adds some other features as well.

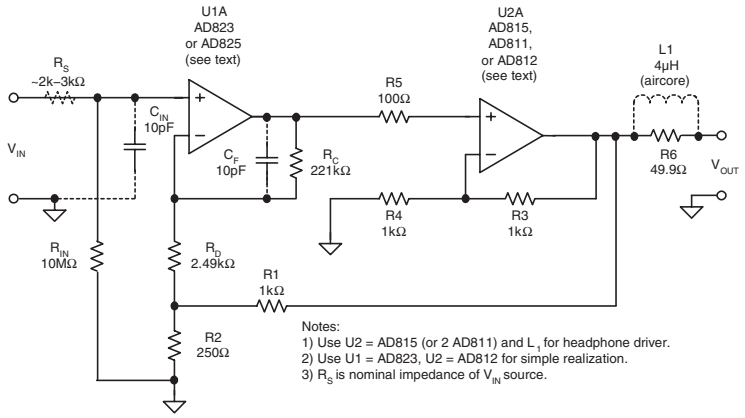


Figure 6-53: Composite current-boosted line driver two

Similarities within this circuit to the predecessor are resistances R_1–R_4, which perform similar functions to the previous version. Overall gain is again calculated via R_1-R_2, while output stage gain is set via R_3, R_4, and so forth.

Note that an additional pair of resistances, R_C and R_D, form a local feedback path around stage U1. This addition allows the effective open-loop bandwidth of U1 as it operates within the overall loop to be increased. For the values shown, using an AD823 for U1, the open-loop bandwidth is about 100 kHz. This means that the open-loop bandwidth of the entire circuit is greater than the audio bandwidth, which means phase errors within the pass band will be minimized.

An optional small capacitance (C_F, 10 pF–20 pF) can be useful for stabilizing the U1 stage, particularly if it employs a wide bandwidth device such as the AD825. When C_F is used, a like capacitor C_{IN} can also be used, to preserve high frequency impedance matching.

The primary input impedance balancing of the circuit is accomplished via resistance R_D, which has a dual role. External resistance R_S is the nominal output resistance of a volume control (typical for a 50 kΩ audio taper control at listening level). R_D is chosen to match R_S, and R_C will be approximately 100 times the R_D value when using the AD823.

The necessity of inductor output L1 depends upon whether the circuit is to be used with low impedance loads. For headphones, the L1 choke is necessary to prevent excessive voltage loss from a simple R_6 connection. R_6 is used in either a headphone or line driver case. If configured as a headphone driver, the circuit should use several square inches of PCB area around U2, to heat sink the AD815 device (see device data sheet). The AD811 and AD812 can also be used to drive higher impedance phones, such as 100 Ω or more.

Because of the vast number of options with this circuit, no performance is presented here. However, some insight into headphone driver performance is contained in Reference 12.

Differential Line Drivers

Unlike differential line receivers, a standard circuit topology for differential line *drivers* isn't nearly so clear-cut. A variety of different circuit types for driving audio lines in a balanced mode are discussed in this section, with their contrasts in performance and complexity. The virtues of balanced audio line operation are many. The largest and most obvious advantage is the inherent rejection of inevitable system ground noises, between the driver and receiver equipment locations.

There are also more subtle advantages to balanced line operation. Differential drivers tend to inject less noise onto the power supply rails. Related to this, they also produce inherently less noise onto the ground system, since by definition the return path for a differential signal is not ground. This can be a significant advantage when high currents need to be driven into a long audio line, as it can reduce multiple channel crosstalk. The circuits that follow illustrate a variety of methods for differential line driving.

"Inverter-Follower" Differential Line Driver

A straightforward approach to developing a differential drive signal of 2 V_{IN} is to amplify in complementary fashion a single-ended input V_{IN}, with equal gain inverter and follower op amp stages. With op amp gains of ±1, this develops outputs $-V_{IN}$ and V_{IN} with respec t to common, or V_{OUT} = 2 V_{IN} differentially. This "inverter/follower" driver is easily accomplished with a dual op amp such as the OP275, plus an 8 × 20k film resistor network (or discrete), as shown above, in Figure 6-54. Here U1A provides the gain of –1 channel, while U1B operates at a gain of +1. The differential output signal across the balanced output line is 2 V_{IN}, and the differential output impedance is equal to $R_A + R_B$, or 100 Ω. The output resistors $R_A + R_B$ should be well matched, for reasons discussed earlier.

Use of like-value gain resistors around the U1 sections makes the respective channel noise gains match, and also makes their purchase easy. In addition, this forces the source impedances seen by the op amp ± inputs to be matched. Capacitors C_1-C_2 provide a ultrasonic roll-off, and enhance stability into capacitive lines. Overall, this circuit is high in performance for its cost and simplicity. Note that if a resistor network is used for R_1– R_8, the entire circuit can be built with only eight components.

THD + N performance of the Figure 6-54 circuit operating on ±18 V supplies is shown in Figure 6-55, for a series of successive sweeps resulting in output levels of 1, 2, 5 and 10 V rms across 600 Ω. The distortion in most instances is about 0.001%, and somewhat higher at a 1 V output level (noise limited at this level). Maximum output level is about 12 V rms into 600 Ω before clipping (not shown).

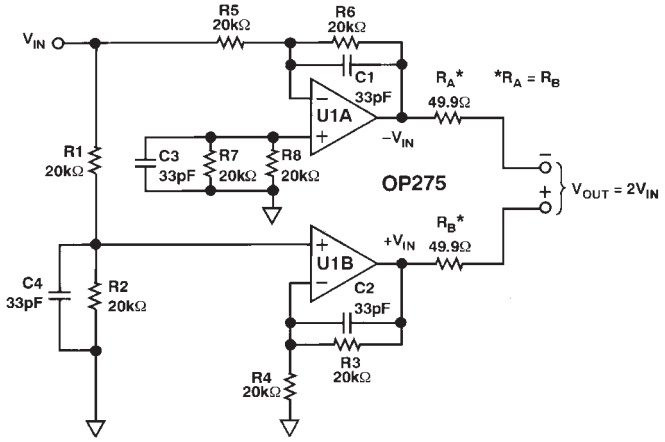


Figure 6-54: An "inverter-follower" differential line driver

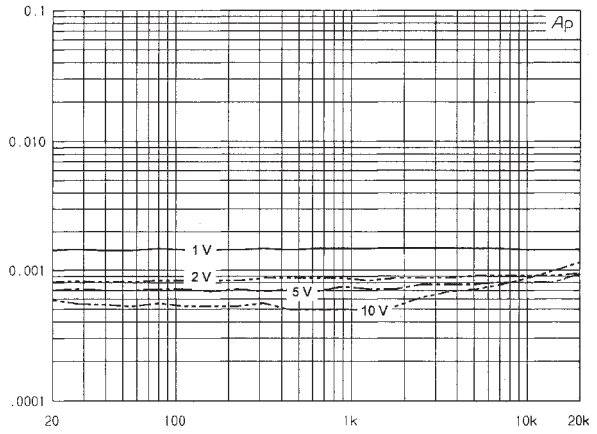


Figure 6-55: Inverter-follower driver of Figure 6-54, THD + N (%) versus frequency (Hz), for V_{OUT} = 1, 2, 5, 10 V rms, R_L = 600 Ω, V_S = ±18 V

In system terms, this type of differential line driver can potentially run into application problems, and should be used with some caveats in mind. In reality, this driver circuit uses two mirror-imaged, single-ended drivers, and they produce voltage output signals with respect to the source (VIN) common point.

At the load end of a cable being driven, if the receiver used has a high impedance differential input (such as discussed in the line receiver section) there is no real problem in application for this driver circuit. However, it should be noted that one side of the differential output from Figure 6-54 *cannot be grounded without side effect*. This is because the source drive V_{OUT} is *not* truly floating, as would be in the case of a transformer winding.

In this sense, the circuit is *pseudo differential*, and it shouldn't be used indiscriminately. Nevertheless, within small and defined systems, is still has the obvious advantage of simplicity and, as noted, it can achieve high performance. Note also that with the matched source resistances R_A and R_B of 49.9 Ω as shown, nothing will be damaged even if one output is shorted—other than a loss of half the signal. Finally, if balanced high impedance differential loading is used at the receiver, there will be no side effects.

Cross-Coupled Differential Line Driver

A more sophisticated form of differential line driver uses a pair of *cross-coupled* op amps with both positive and negative feedback paths. The general form of this type of circuit is a cross-coupled Howland circuit, after the classic resistor bridge based current pump. The cross-coupled form was described by Pontis in a solid-state transformer emulator for high performance instrumentation (see Reference 13).

Application-wise, this configuration provides maximum flexibility, allowing a differential output signal V_{OUT} to be maintained constant and independent of the load common connections. This means that either side can be shorted to common without loss of signal level, i.e., as can be done with a transformer.

Figure 6-56 shows the SSM2142 balanced line driver IC in an application. The SSM2142 consists of two Howland circuits A2 and A3, cross-coupled as noted, plus an input buffer (A1). The trimmed multiple resistor array and trio of op amps shown is packaged in an 8-pin miniDIP IC with the pinout noted.

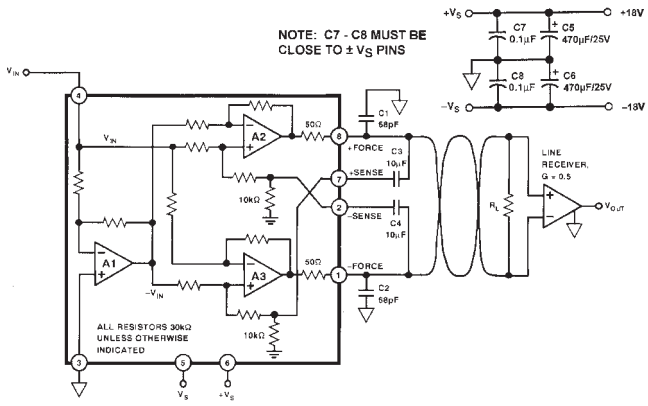


Figure 6-56: SSM2142 cross-coupled differential line driver used within balanced driver/receiver system

The SSM2142 line driver is designed for a single-ended to differential gain of 2 working into a 600 Ω load. In the simplest use, it is strapped with the respective output FORCE/SENSE pins tied together (7-8, 1-2). Small film capacitors C_1-C_2 preload the IC for stability against varying cable lengths. To decouple line dc offsets, the optional capacitors C_3-C_4 are used as shown, and should be nonpolar types, preferably films.

An additional "housekeeping" caveat with the SSM2142 involves the high frequency power supply bypassing. The 0.1 µF low inductance bypass caps C_7 and C_8 must be within 0.25" of power supply Pins 5 and 6, as noted in the figure. If this bypassing is compromised by long lead lengths, excessive THD will be evident.

In a system application, the SSM2142 is used with a complementary gain of 0.5 receiver, either an SSM2143, or one of the other line receivers discussed previously. The complete hookup of Figure 6-56 comprises an entire single-ended-to-differential and back to single-ended transmission system, with noise isolation and a net end-to-end unity gain.

Figure 6-57 shows the THD + N performance of the SSM2142 driver portion of Figure 6-56, for sweeps yielding output levels of 1, 2, 5 and 10 V rms across 600 Ω. While performance is noise limited for the 1 V output curve, distortion drops to ≤0.001% and near residual for most higher levels, rising only with higher frequencies and the 10 V output curve.

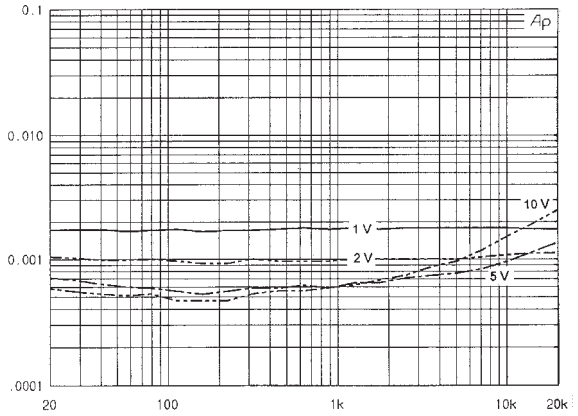


Figure 6-57: SSM2142 driver portion of Figure 6-56, THD + N (%) versus frequency (Hz), for V_{OUT} = 1, 2, 5, 10 V rms, R_L = 600 Ω, V_S = ±18 V

These two differential drivers are suited for 600 Ω or higher loads, and, within those constraints, perform well.

As should be obvious, these drivers do *not* offer galvanic isolation, which means that in all applications there must be a dc current path between the grounds of the driver and the final receiver. In practice however this isn't necessarily a problem.

The following circuits illustrate differential drivers that do offer galvanic isolation, and can therefore be used with ground potential differences up to several hundred volts (or the actual voltage breakdown rating of the transformer in use).

Transformer-Coupled Line Drivers

Transformers provide a unique method of signal coupling, which is one that allows completely isolated common potentials, i.e., *galvanic isolation*. As noted previously in the line receiver section, transformers are not without their technical and practical limitations, but their singular ability to galvanically isolate grounds maintains a place for them in difficult application areas (see References 15 and 16).

Basic Transformer-Coupled Line Driver

The circuit of Figure 6-58 uses some previously described concepts to form a basic low dc offset, high linearity driver using a high quality nickel core output transformer. U1 and U2 form a high current driver, similar to the Figure 6-49 current-boosted driver.

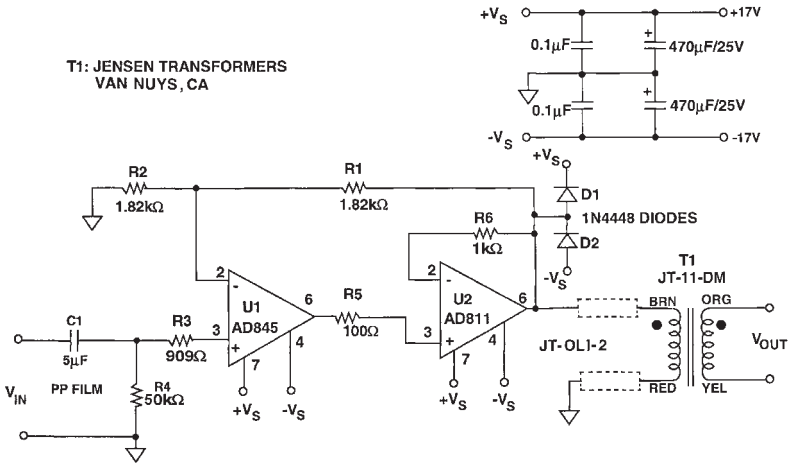


Figure 6-58: A basic transformer-coupled line driver

In this circuit U1 is a low offset voltage FET input op amp, for the purpose of holding the dc offset seen at the primary of T1 to a minimum (±12.5 mV maximum as shown, typically less). Dc current flowing into the primary winding of a transformer should be minimized, for lowest distortion. C_1, a high quality film capacitor, decouples any dc offset present on V_{IN}, for similar reasons.

The U1-U2 device combination is capable of ±100 mA or more of output, which aids greatly in the ability of this circuit to drive low impedances. The buffering of U2 is recommended for long lines, or for the absolute lowest distortion. Although T1 is shown with a 1:1 coupling ratio, other winding configurations are possible with transformer variations, that is step-up or step-down, allowing either 600 Ω or 150 Ω loads.

As can be noted, the T1 primary isn't driven directly, but is isolated by two series isolation devices, Jensen JT-OLI-2s. Each of these is an LR shunt combination of about 39 Ω and 3.7 µH. The net impedance offers a very low DCR, and an increasing impedance above 1.5 MHz for load isolation (see device data sheet and Reference 17). The use of two isolators as shown offers best output CMR rejection for the transformer, but one will also work (with less CMR performance), as will a single 10 Ω resistor.

THD + N performance for this driver-transformer combination is shown in Figure 6-59, for supplies of ±18 V and successive input sweeps, resulting in outputs of 1, 2, 4, and 8 V rms into 600 Ω. These data were taken with a single series resistance of 10 Ω driving T1 (which could be conservative compared to operation with two isolators).

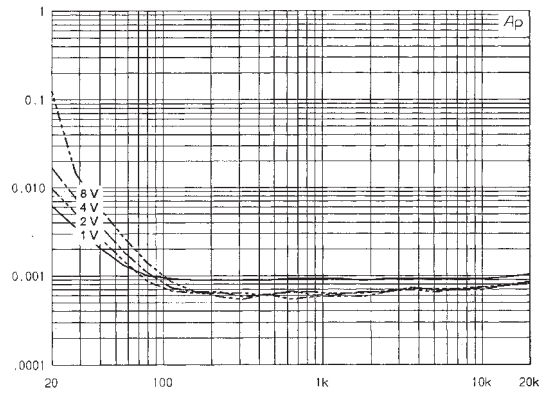


Figure 6-59: Transformer driver of Figure 6-58, THD + N (%) versus frequency (Hz), for V_{OUT} = 1, 2, 4, 8 V rms, R_L = 600 Ω, V_S = ±18 V

As with the 2x and 5x basic drivers previously described, these data are essentially distortion free above 100 Hz. At lower frequencies there is seen a level dependent, inverse-frequency dependent distortion. The measured distortion reaches a maximum at 20 Hz with output levels of 8 V rms (≈20 dBm), while at lower levels it is substantially less.

To one degree or another, this distortion phenomenon is basic to audio transformers. It is lessened (but not totally eliminated) in the higher quality transformer types, such as the nickel-core unit used in the Figure 6-58 circuit.

In practice, there are some factors that tend to mitigate the seriousness of the low frequency distortion seen in the performance data of Figure 6-59. First, rarely will maximum audio levels ever be seen at 20 Hz. Thus suitably derated operation of T1 will strongly reduce the incidence of this distortion.

However, if the lowest distortion possible independent of level is desired, then some additional effort will need to be expended on making the transformer driver more sophisticated. This can take the form of actively applying feedback around the transformer, to lower its nonlinearity to negligible levels. This is design approach is discussed with the next driver circuits.

Feedback Transformer-Coupled Line Drivers

While nonpremium core transformers are more economical than the nickel core types, as a trade-off they do have much higher distortion. To further complicate the design issue, the distortion characteristics of most transformers varies with level and frequency in complex ways, rising more rapidly at higher levels and lower frequencies. This behavior is even less forgiving than that of the nickel core types, and somewhat complicates the application of audio transformers. While a nickel core transformer has distortion characteristics sufficiently low as to allow their use without distortion correction (Figure 6-58) the same simply isn't true for other core materials.

A family of distortion curves for another transformer type illustrates this behavior, shown in Figure 6-60. This series of plots is for a Lundahl LL1517 silicon iron C core unit, with successive output levels of 0.5, 1, 2 and 5 V rms into a 600 Ω load. Individual device samples will vary, but the general pattern is typical of many audio transformers.

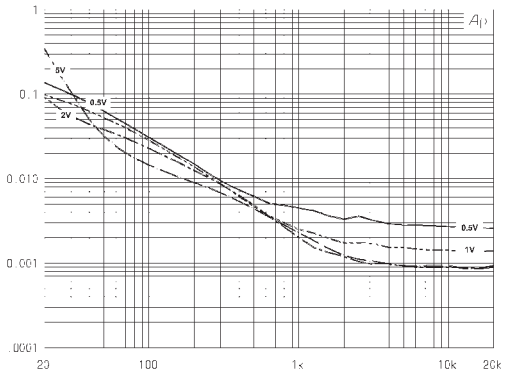


Figure 6-60: Lundahl LL1517 transformer and driver (without feedback), THD + N (%) versus frequency (Hz), for V_{OUT} = 0.5, 1, 2, 5 V rms, R_L = 600 Ω

Werner Baudisch (see Reference 18) developed a very effective driver technique for minimization of transformer distortion. The technique involves the use of a drive amplifier, connected to the transformer primary in a direct manner. The amplifier uses conventional negative feedback for gain stabilization. In addition, a primary sensing resistance develops a voltage sample proportional to primary current, and the voltage thus derived is also fed back to the amplifier. This second feedback path is positive feedback, so the arrangement is also known as a *mixed feedback* driver (see Reference 19).

This very useful technique of the mixed feedback driver can be used to advantage to integrate a line driver with the transformer primary within a feedback loop, which cancels the bulk of the objectionable distortion. In practice, with careful driver adjustment it is possible to reduce the distortion of the transformer plus driver almost to *that of the driver stage, operating without the transformer*. The beauty of the principle is that the inherent floating transformer operation is not lost, and is still effectively applied in a highly linear mode. Due to the action of the mixed feedback, the transformer primary resistance is effectively cancelled, thus appreciably lowering the net secondary output impedance.

The circuit of Figure 6-61 is a basic, single-ended mixed feedback driver using either a Lundahl LL1582 or LL2811 transformer as T1, and an AD845 or an OP275 as the amplifier. These transformers have two 1:1 primaries, as well as two 1:1 secondaries. As used, both primaries are connected in series, and the T1 net voltage transfer is unity.

To enable correct mixed feedback operation, two key ratios within the circuit must be set to match. One ratio is between the net T1 primary resistance, $R_{PRIMARY}$ and sample resistor R_4, and the other is R_2 and R_1. This relationship is:

$$R_{PRIMARY} / R_4 = R_2 / R_1 \qquad \text{Eq. 6-18}$$

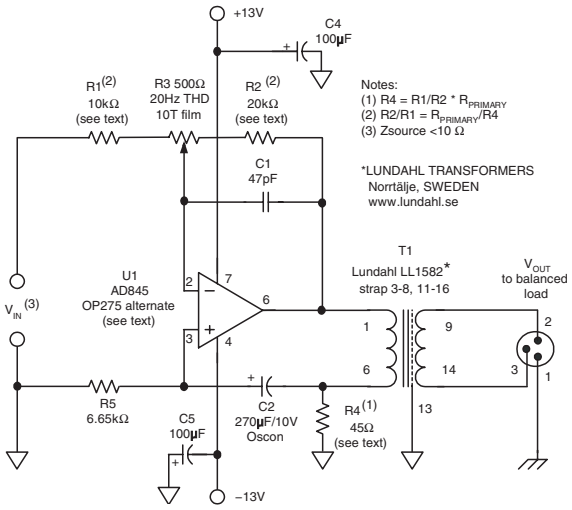


Figure 6-61: A basic single-ended mixed feedback transformer driver

It is important to note that $R_{PRIMARY}$ is the total effective dc resistance of T1. As used here, two series 45 Ω primaries are used, so $R_{PRIMARY}$ is 90 Ω. Gain of the driver circuit is established as in a standard inverter, or the R_2-R_1 ratio. For a gain of 2 ×, R_2 is then simply 2 times R_1, i.e., 20 kΩ and 10 kΩ. R_4 may then be selected as:

$$R_4 = R_1/R_2 * R_{PRIMARY} \qquad \text{Eq. 6-19}$$

With the R_1/R_2 ratio of 0.5, this makes R_4 simply one-half $R_{PRIMARY}$, or in this case 45 Ω.

Note the value of R_1 is critical, thus the V_{IN} source impedance must be low (<10 Ω). This and other subtleties are effective performance keys. One is the sensitivity of the ratio match described by Eq. 6-18. Only when trimmed optimally will the lowest frequency THD be minimum. Thus a multiturn film trimmer R_3 is used to trim out the various tolerances and the winding resistance of T1. Further, the positive feedback path is ac-coupled via C_2. This provision prevents dc latchup, should positive feedback override the negative. However, a simple time constant of, say, 8 ms (corresponding to 20 Hz) is *not sufficient* for lowest low frequency THD. To counteract this, the C_2-R_5 time constant is set quite long (≈1.8 seconds), which enables lowest possible 20 Hz THD. With the suggested AD845 for U1, distortion is lowest, as it is also with an Oscon capacitor for C_2. A larger value ordinary aluminum electrolytic can also be used for C_2, with a penalty of somewhat high distortion. Alternately, an OP275 can also be used for U1 (see following).

With the AD845 FET input op amp used for U1, the maximum dc at the T1 primary is essentially the amplifier Vos times the stage's 3× noise gain, or ≤7.5 mV. Since the AD845 can also dissipate ≈250 mW, the lowest possible supplies help keep the offset change with temperature as low as possible.

Lab THD + N measurements of Figure 6-61 were made using an LL2811, a transformer like the LL1582, but without a Faraday shield. The two transformers are very similar, but the LL1582 is recommended for single-ended drive circuits. The performance of this feedback driver is shown in Figure 6-62, for successive output levels of 0.5, 1, 2, and 5 V rms into a 600 Ω load. Comparison of these data with Figure 6-60 bears out the utility of the distortion reduction; it is decreased by orders of magnitude. More importantly, the level dependence with decreasing frequency is essentially eliminated.

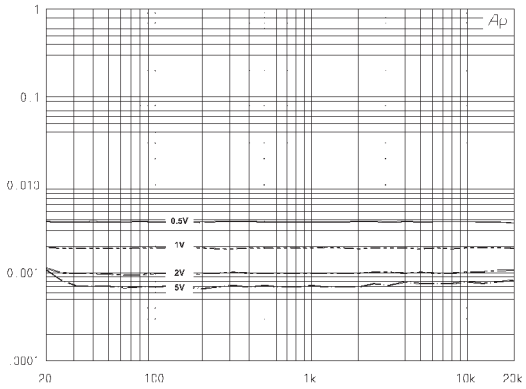


Figure 6-62: Figure 6-61 driver with Lundahl LL2811 transformer and AD845, THD + N (%) versus frequency (Hz), for V_{OUT} = 0.5, 1, 2, 5 V rms, R_L = 600 Ω

These data do in fact represent almost an ideal THD + N pattern; the distortion level is flat with frequency, and it decreases with increasing output level. An extremely slight increase in THD + N can just be discerned at 20 Hz in the 5 V curve. The alternate OP275 for U1 also works well, but does have slightly higher distortion (not shown).

Although directly comparable data is not presented for it, it is worth noting that the LL1517 transformer can also be used with the Figure 6-61 circuit, with R_4 = 9.2 Ω, and the two primaries connected in series. However, some additional data on a circuit quite similar to Figure 6-61 does reveal a potential limitation for this type of driver.

Figure 6-63 shows a set of high level THD + N curves for a mixed feedback driver using an AD8610 op amp for U1, and the LL1517 transformer. Three THD + N sweeps are made, with the lowest THD + N curve representing the best possible null. The other two curves show increased THD + N at low frequencies, for conditions of R_2/R_1 ratio mismatches of 1% and 5%, respectively. This demonstrates how critical a proper null is towards achieving the lowest possible distortion at the low end of the audio band.

It is possible to tweak the ratio via R_3 for an excellent 20 Hz high level null at room temperature, and this is recommended to get the most from one of these circuits. It must also be remembered that the TC of the T1 copper windings is about 0.39%/°C. Therefore, only a 10°C ambient temperature change would be sufficient to degrade the best null by nearly 5%. The resulting performance would then roughly represent the upper curve of Figure 6-63—still quite good, but just not quite as good as possible in absolute terms.

For the best and most consistent performance, wide temperature range applications of this type of circuit should therefore employ some means of temperature compensation for the copper winding(s) of T1. One means of achieving this would be to employ a thermally sensitive device to track the copper TC of T1. The

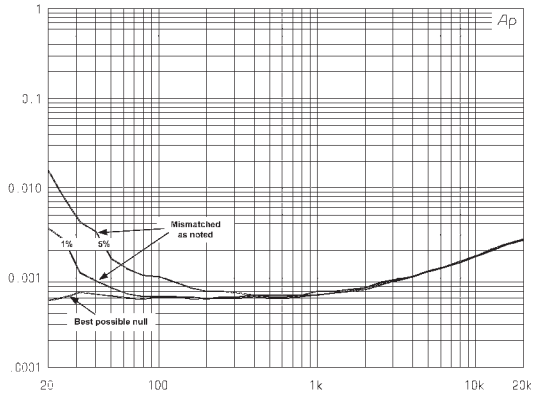


Figure 6-63: Lundahl LL1517 transformer with mixed feedback AD8610 driver, THD + N (%) versus frequency (Hz) for various null accuracies

net goal should be to hold the $R_{PRIMARY}/R_4$ ratio constant over temperature. It should also be noted that for this approach to work, it is assumed that the R_2/R_1 ratio is temperature independent. This is possible with the use of close tolerance, low TC metal film resistors, i.e., 50 ppm/°C or better (or the use of a low tracking TC network).

It should also be noted that the *output balance* of an audio transformer is a very important factor when designing audio line drivers. Poor transformer balance can lead to mode conversion of CM signals on the output line (see Reference 20). The result is that a spurious differential mode signal can be created due to poor balance. A transformer can attain good balance (i.e., 60 dB or better) by the use of sophisticated winding techniques, or the use of a Faraday shield, as is true in the case of the LL1582 and the LL1517.

Transformer drivers can of course also be operated in a balanced drive fashion. This has the advantage of doubling the available drive voltage for given supply voltages, plus lowering the distortion produced. Mixed feedback principles can be extended to a balanced arrangement, which lowers the distortion in the same manner as for the single-ended circuit just described. An example circuit is shown in Figure 6-64.

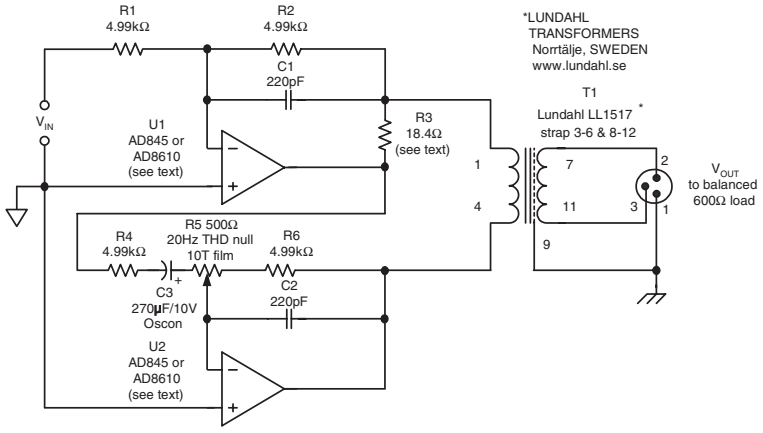


Figure 6-64: A balanced transformer driver circuit that applies mixed feedback principles of distortion minimization

In Figure 6-64, a U1-U2 low distortion op amp pair drive an LL1517 transformer. U1 is an inverting gain circuit as defined by gain resistors R_1-R_2, which drives the top of T1. Placed in series with the T1 primary, R_3 acts as a current sampling resistor, and develops a correction voltage to drive the second inverter, U2, through R_4.

This scheme is adapted from the mixed feedback balanced driver circuit of Arne Offenberg (see Reference 21). There are, however, two main differences in this version. One is operation of the U1 stage as an inverter, which eliminates any CM distortion effects in U1, and the second being the ability to easily set the overall driver gain via R_1-R_2. Within this circuit, it should be noted that the resistances R_1-R_2 do *not* affect the distortion null (as they do in the simpler circuit of Figure 6-61).

The distortion null in this form of the circuit occurs when the ratios $R_3/R_{PRIMARY}$ and R_4/R_6 match. For simplicity, the second inverter gain is set to unity, so R_3 is selected as:

$$R_3 = R_4 / R_6 * R_{PRIMARY} \qquad \text{Eq. 6-20}$$

For the R_4–R_6 values shown, R_3 then is simply equal to $R_{PRIMARY}$, or 18.4 Ω when used with the LL1517 transformer with series connected primaries.

As with any of these driver circuits, the exact op amp selection has a great bearing on final performance. Within a circuit using two amplifiers, dual devices are obviously attractive. The distortion testing below discusses amplifier options.

THD + N performance data for the balanced transformer driver of Figure 6-64 is shown in Figure 6-65, using an LL1517 transformer with successive output levels of 0.5, 1, 2, and 5 V rms into a 600 Ω load. For these tests, the supply voltages were ±13 V, and the U1-U2 op amp test devices were pairs of either the AD8610 or the AD845 (note—two AD8610 singles are comparable to a single AD8620 dual).

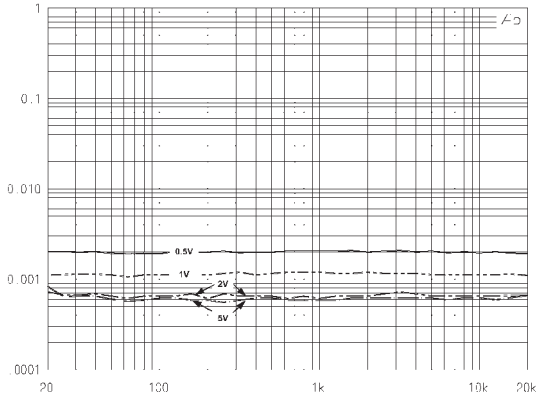


Figure 6-65: Figure 6-64 balanced driver with Lundahl LL1517 transformer and two AD8610s, THD + N (%) versus frequency (Hz), for V_{OUT} = 0.5, 1, 2, 5 V rms, R_L = 600 Ω

An interesting thing about these plots is the fact that the THD + N is both low and essentially unchanged with frequency, which is again near ideal. Low frequency nulling of the distortion is almost as critical in this circuit as in the previous, and a slight upturn in THD + N can be seen at 20 Hz, for the highest level (5 V).

For the AD8610 devices shown by these data, the wideband THD + N was slightly lower than a comparable test with the AD845 pair (the latter not shown). Both amplifier sets show essentially flat THD + N versus frequency characteristics.

Because of the balanced drive nature of this circuit, the realization offers lower distortion than the simpler single-ended version of Figure 6-61, plus a buffering of the distortion null sensitivity against the input source impedance and gain adjustment. It can thus be considered a more robust method of transformer distortion minimization. For these reasons, the balanced form of driver is recommended for professional or other high performance requirements. Note, however, that similar caveats do apply with regard to stabilizing the distortion null against temperature.

This driver can be used with the LL1517 and many other transformers with, of course, an appropriate choice of R_3. Note that the performance data above reflects use of the op amps operating unbuffered. For very low impedance loads and/or long lines, a pair of the previously described unity gain buffers should be considered, and both the U1 and U2 stages operated with output buffering. This will allow the retention of THD + N performance as is shown in Figure 6-65, but in the face of more difficult loads.

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SECTION 6-2

Buffer Amplifiers and Driving Capacitive Loads

Walt Jung, Walt Kester

Buffer Amplifiers

In the early days of high speed circuits, simple emitter followers were often used as high speed buffers. The term *buffer* was generally accepted to mean a unity-gain, open-loop amplifier. With the availability of matching PNP transistors, a simple emitter follower can be improved, as shown in Figure 6-66A. This complementary circuit offers first-order cancellation of dc offset voltage, and can achieve bandwidths greater than 100 MHz. Typical offset voltages without trimming are usually less than 50 mV, even with unmatched discrete transistors. The HOS-100 hybrid amplifier from Analog Devices represented an early implementation of this circuit. This device was a popular building block in early high speed ADCs, DACs, sample-and-holds, and multiplexers.

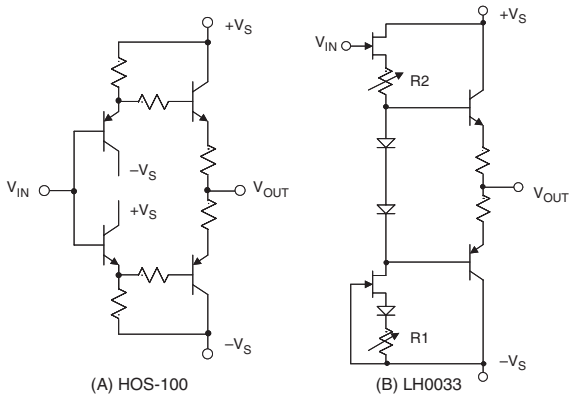


Figure 6-66: Early open-loop hybrid buffer amplifiers: (A) HOS-100 bipolar, (B) LH0033 FET input

If high input impedance is required, a dual FET can be used as an input stage ahead of a complementary emitter follower, as shown in Figure 6-66B. This form of the buffer circuit was implemented by both National Semiconductor Corporation as the LH0033, and by Analog Devices as the ADLH0033.

In the realizations of these hybrid devices, thick film resistors were laser trimmed to minimize input offset voltage. For example, in the Figure 6-66(B) circuit, R1 is first trimmed to set the bias current in the dual matched FET pair, which is from the 2N5911 series of parts. R2 is then trimmed to minimize the buffer input-to-output offset voltage.

Circuits such as these achieved bandwidths of about 100 MHz at fairly respectable levels of harmonic distortion, typically better than –60 dBc. However, they suffered from dc and ac nonlinearities when driving loads less than 500 Ω.

One of the first totally monolithic implementations of these functions was the Precision Monolithics, Inc. BUF03 shown in Figure 6-67 (see Reference 1). PMI is now a division of Analog Devices. This open-loop IC buffer achieved a bandwidth of about 50 MHz for a 2 V peak-to-peak signal.

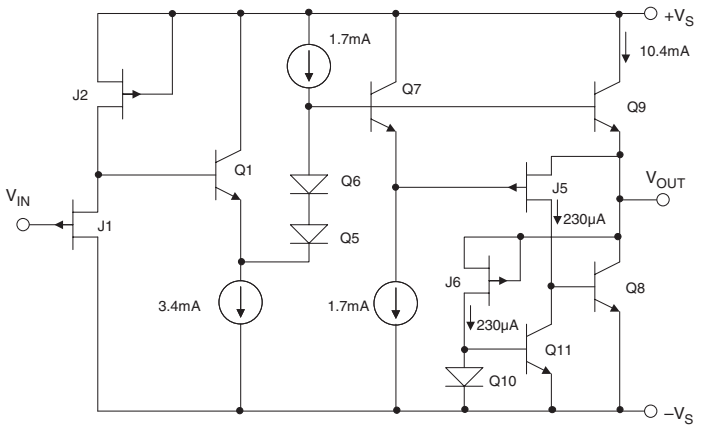


Figure 6-67: BUF03 monolithic open-loop buffer 1979 vintage

The BUF03 circuit is interesting because it demonstrates techniques that eliminated the requirement for the slow, bandwidth-limited vertical PNP transistors associated with most IC processes available at the time of the design (approximately 1979).

Within the circuit, input transistor J1 is a FET source follower that is biased by an identical FET J2, thereby making the gate-to-source voltage of J1 nominally zero. The output of J1 is applied to emitter follower Q1, and diodes Q5 and Q6 compensate for the combined base-emitter drops of Q1 and Q7/Q9.

The current through Q7 is held at a constant 1.7 mA, therefore its V_{BE} is constant. Transistors Q7 and Q9 are scaled such that the current in Q9 is six times that of Q7 for equal V_{BE} drops. If the load current changes, and Q9 is required to source more or less current, its V_{BE} attempts to increase or decrease. This change is applied between the gate and source of J5, which then reduces/increases current in the base of Q8 to maintain the current in Q9 at six times that of Q7. The localized feedback works for load currents up to ±10 mA. The current in Q9 is therefore held constant at 10.4 mA (independent of load) because its V_{BE} drop does not change with either output voltage or load current.

With a 1 kΩ load, and an output voltage of +10 V, transistor Q8 must sink 0.2 mA, and Q9 supplies 10 mA to the load, 0.2 mA to J5, and 0.2 mA to J6. For an output of −10 V, Q8 must sink 20.2 mA so that the net current delivered to the load is −10 mA. In addition to achieving a bandwidth of approximately 50 MHz (2 V peak-to-peak output), on-chip zener-zap trimming was used to achieve a dc offset of typically less than 6 mV.

One of the problems with all the open-loop buffers discussed thus far is that although high bandwidths can be achieved, the devices discussed don't take advantage of negative feedback. Distortion and dc performance suffer considerably when open-loop buffers are loaded with typical video impedance levels of 50 Ω, 75 Ω, or 100 Ω. The solution is to use a properly compensated wide bandwidth op amp in a unity-gain follower configuration. In the early days of monolithic op amps, process limitations prevented this, so the open-loop approach provided a popular interim solution.

Today, however, practically all unity-gain-stable voltage or current feedback op amps can be used in a simple follower configuration. Usually, however, the general-purpose op amps are compensated to operate over a wide range of gains and feedback conditions. Therefore, bandwidth suffers somewhat at low gains, especially in the unity-gain noninverting mode, and additional external compensation is usually required.

A practical solution is to compensate the op amp for the desired closed-loop gain, while including the gain setting resistors on-chip, as shown in Figure 6-68. Note that this form of op amp, internally configured as a buffer, may typically have no feedback pin. Also, putting the resistors and compensation on-chip also serves to reduce parasitics.

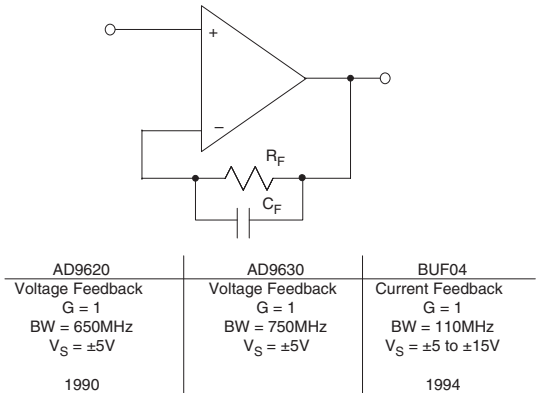


Figure 6-68: Early closed-loop unity-gain monolithic buffers

A number of op amps are optimized in this manner. Roy Gosser's AD9620 (see Reference 2) was probably the earliest monolithic implementation. The AD9620 was a 1990 product release, and achieved a bandwidth of 600 MHz using ±5 V supplies. It was optimized for unity gain, and used the voltage feedback architecture. A newer design based on similar techniques is the AD9630, which achieves a 750 MHz bandwidth.

The BUF04 unity gain buffer (see Reference 3) was released in 1994 and achieves a bandwidth of 120 MHz. This device was optimized for large signals and operates on supplies from ±5 V to ±15 V. Because of the wide supply range, the BUF04 is useful not only as a standalone unit-gain buffer, but also within a feedback loop with a standard op amp, to boost output (see discussions within "Audio Amplifiers" portion of this chapter).

Closed-loop buffers with a gain of two find wide applications as transmission line drivers, as shown below in Figure 6-69. The internally configured fixed gain of the amplifier compensates for the loss incurred by the source and load termination. Impedances of 50 Ω, 75 Ω, and 100 Ω are popular cable impedances. The AD8074/AD8075 500 MHz triple buffers are optimized for gains of 1 and 2, respectively. The dual AD8079A/AD8079B 260 MHz buffer is optimized for gains of 2 and 2.2, respectively.

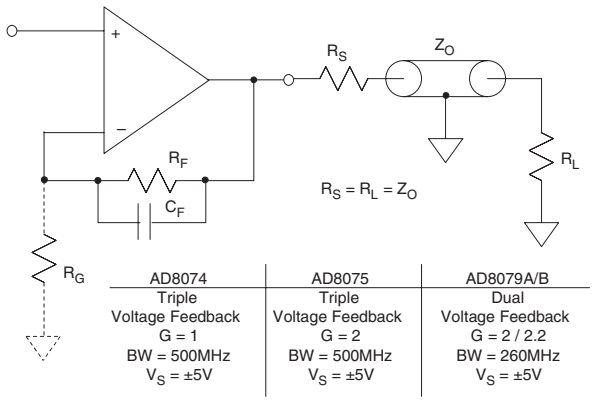


Figure 6-69: Fixed-gain video transmission line drivers

The buffer amplifiers discussed above are all dedicated to either unity or some higher fixed-gain setting. As wide bandwidth fixed-gain blocks they are simply applied, without the need for additional gain configuration components. They will, of course (as with any high-speed amplifier), require supply bypassing components as well as appropriate layout.

Buffers can also be implemented with almost any unity-gain-stable voltage or current feedback op amp. Examples that come to mind for voltage feedback devices are the single AD817 (or the dual counterpart AD826), or for current feedback devices the AD811, AD8001, AD8015, along with their dual-device cousins (as is applicable). In addition, there are op amps with feature rail-rail outputs as well as operation at low supply voltages—the AD8031/AD8032 and AD8041/AD8042 are examples.

In implementing a high speed unity-gain buffer with a voltage feedback op amp, there will typically be no resistor required in the feedback loop, which considerably simplifies the circuit. Note that this isn't a 100% hard-and-fast rule, however, so always check the device data sheet to be sure. A unity-gain buffer with a current feedback op amp will *always* require a feedback resistor, typically in the range of 500 Ω–1000 Ω. So, be sure to use a value appropriate not only to the basic part, but also the specific power supplies in use.

Driving Capacitive Loads

From either a system or signal fidelity point of view, transmission line coupling between stages is best, and is described in some detail in the next section. However, complete transmission line system design may not always be possible or practical. In addition, various other parasitic issues need careful consideration in high performance designs. One such problem parasitic is amplifier *load capacitance*, which potentially comes into play for all wide bandwidth situations that do not use transmission line signal coupling.

A general design rule for wideband linear drivers is that capacitive loading (cap loading) effects should *always* be considered. This is because PC board capacitance can build up quickly, especially for wide and

long signal runs over ground planes insulated by a thin, higher K dielectric. For example, a 0.025" PC trace using a G-10 dielectric of 0.03" over a ground plane will run about 22 pF/foot (see References 4 and 5). Even relatively small load capacitance (i.e., <100 pF) can be troublesome, since while not causing outright oscillation, it can still stretch amplifier settling time to greater than desirable levels for a given accuracy.

The effects of cap loading on high speed amplifier outputs are not simply detrimental, they are actually an anathema to high quality signals. However, before-the-fact designer knowledge still allows high circuit performance by employing various tricks of the trade to combat the capacitive loading. If it is not driven via a transmission line, remote signal circuitry should be very carefully checked for capacitive loading, and characterized as well as possible. Drivers that face poorly defined load capacitance should be bulletproofed accordingly with an appropriate design technique from the options list below.

Short of a true matched transmission line system, a number of ways exist to drive a load that is capacitive in nature, while still maintaining amplifier stability.

Custom capacitive load (cap load) compensation includes two possible options, namely a) overcompensation, and b) an intentionally forced high loop noise gain allowing crossover in a stable region. Both of these steps can be effective in special situations, as they reduce the amplifier's effective closed-loop bandwidth, so as to restore stability in the presence of cap loading.

Overcompensation of the amplifier, when possible, reduces amplifier bandwidth so that the additional load capacitance no longer represents a danger to phase margin. As a practical matter, however, amplifier compensation nodes to allow this are available on very few of the newer high speed amplifiers.

Nevertheless, there are still useful examples, and one is the AD829, compensated by a single capacitor to ac-common, at Pin 5. A more recent and analogous part is the AD8021, which is similarly compensated. In general, almost any amplifier using external compensation can always be over compensated to reduce bandwidth. This will restore stability against cap loads, by lowering the amplifier's unity gain frequency.

Forcing a high noise gain is shown in Figure 6-70, where the left side capacitively loaded amplifier with a noise gain of unity is unstable, due to a 1/β – open-loop roll-off intersection on the Bode diagram in a –12 dB/octave rolloff region. For such a case, introducing higher noise gain can restore often stability, so that the critical intersection occurs in a stable –6 dB/octave region, as depicted at the right diagram and Bode plot.

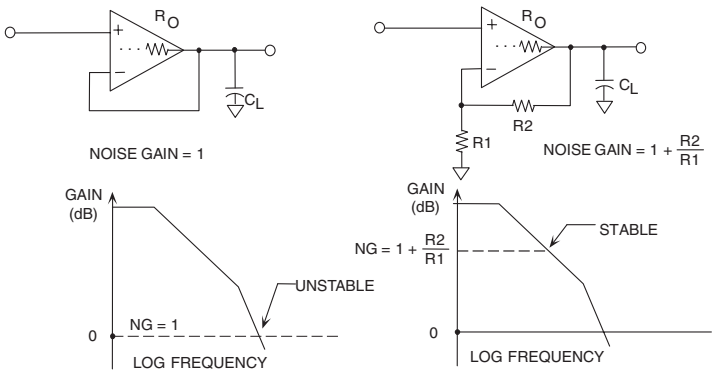


Figure 6-70: Effect of capacitive loading on op amp stability

To enable a higher noise gain (which does not necessarily need to be the same as the stage's *signal gain*), use is made of resistive or RC pads at the amplifier input, as in Figure 6-71. This trick is broader in scope than overcompensation, and has the advantage of not requiring access to any internal amplifier nodes. This generally allows use with any amplifier setup, even voltage followers (left) or inverters (right). An extra resistor, R_D, is added which works against R_F to force the noise gain of the stage to a level appreciably higher than the signal gain (unity for both cases here).

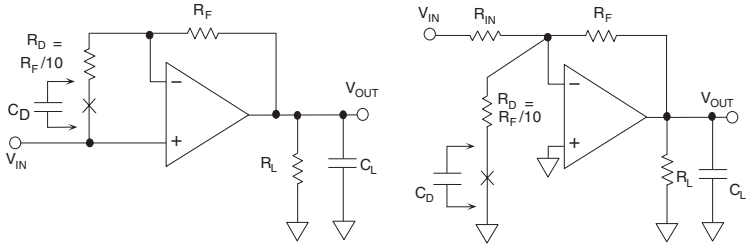


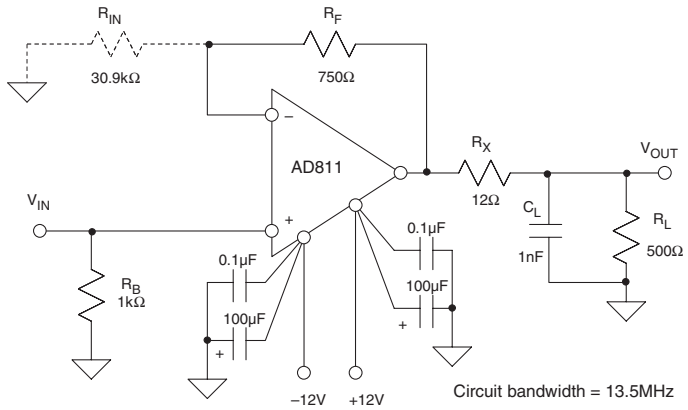
Figure 6-71: Raising noise gain (dc or ac) for follower (A) or inverter (B) stability

Assuming C_L is a value that produces a parasitic pole slightly above or near the amplifier's natural crossover, this loading combination would lead to oscillation due to the excessive phase lag. However, with R_D connected, the forced higher amplifier noise gain produces a new 1/β and open-loop roll-off intersection, purposely set about a decade lower in frequency. This is low enough that the extra phase lag from C_L near the amplifier's natural unity-gain crossover is no longer a problem, and stability is restored.

A drawback to this trick is that both the dc offset and input noise of the amplifier are raised by the value of the noise gain, when R_D is dc-connected. But, when C_D is used in series with R_D, the offset voltage of the amplifier is not raised, and the gained-up ac noise components are confined to a frequency region above $1/(2\pi \bullet R_D \bullet C_D)$. A further caution is that this technique can be somewhat tricky when separating these operating dc and ac regions, and should be applied carefully with regard to settling time (see Reference 6). Note that these simplified examples are generic, and in practice the absolute component values should be matched to a specific amplifier.

"Passive" cap load compensation, shown in Figure 6-72, is the most simple (and most popular) isolation technique available. It uses a simple "out-of-the-loop" series resistor R_X to isolate the cap load, and can be used with any amplifier, current or voltage feedback, FET or bipolar input.

Figure 6-72: Open-loop series resistance isolates capacitive load



As noted, since this technique applies to just about any amplifier, it is a major reason why it is so useful. It is shown here with a current feedback amplifier suitable for high current line driving, the AD811, and it consists of just the simple (passive) series isolation resistor, R_X. This resistor's minimum value for stability will vary from device to device, so the amplifier data sheet should be consulted for other ICs. Generally, information will be provided as to the amount of load capacitance tolerated, and a suggested minimum resistor value for stability purposes.

Drawbacks of this approach are the loss of bandwidth as R_X works against C_L, the loss of voltage swing, a possible lower slew rate limit due to I_{MAX} and C_L, and a gain error due to the R_X-R_L division. The gain error can be optionally compensated with R_{IN}, which is ratioed to R_F as R_L is to R_X. In this example, a ±100 mA output from the op amp into C_L can slew V_{OUT} at a rate of 100 V/µs, far below the intrinsic AD811 slew rate of 2500 V/µs. Although the drawbacks are serious, this form of cap load compensation is nevertheless useful because of its simplicity. If the amplifier isn't otherwise protected, then an R_X resistor of 50 Ω–100 Ω should be used with virtually any amplifier facing capacitive loading. Although a noninverting amplifier is shown, the technique applies equally to inverters.

With very high speed amplifiers, or in applications where lowest settling time is critical, even small values of load capacitance can be disruptive to frequency response, but are nevertheless sometimes inescapable. One case in point is an amplifier used for driving ADC inputs. Since high speed ADC inputs quite often look capacitive in nature, this presents an oil/water type of problem. In such cases the amplifier *must* be stable driving the capacitance, but it must also preserve its best bandwidth and settling time characteristics. To address this cap load case, R_S and C_L data for a specified settling time is appropriate.

Some applications, in particular those that require driving the relatively high impedance of an ADC, do not have a convenient back termination resistor to dampen the effects of capacitive loading. At high frequencies, an amplifier's output impedance is rising with frequency and acts like an inductance which, in combination with C_L, causes peaking or, even worse, oscillation. When the bandwidth of an amplifier is an appreciable percentage of device F_t, the situation is complicated by the fact that the loading effects are reflected back into its internal stages. In spite of this, the basic behavior of most very wide bandwidth amplifiers such as the AD8001 is very similar.

In general, a small damping resistor (R_S) placed in series with C_L will help restore the desired response (see Figure 6-73). The best choice for this resistor's value will depend upon the criterion used in determining the desired response. Traditionally, simple stability or an acceptable amount of peaking has been used, but a

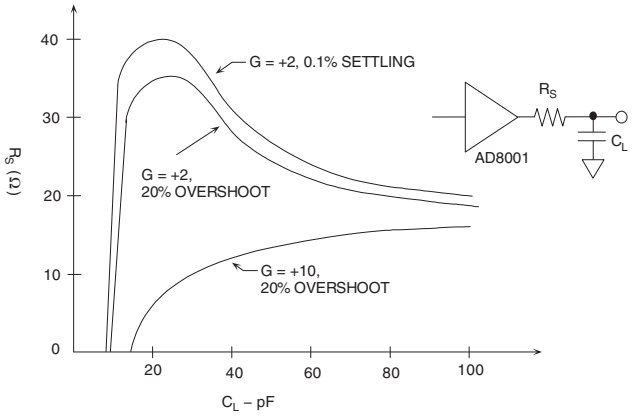


Figure 6-73: AD8001 R_S required for various C_L values

more strict measure such as 0.1% (or even 0.01%) settling will yield different values. For a given amplifier, a family of R_S-C_L curves exists, such as those of Figure 6-73. These data will aid in selecting R_S for a given application.

The basic shape of this curve can be easily explained. When C_L is very small, no resistor is necessary. When C_L increases to some threshold value an R_S becomes necessary. Since the frequency at which the damping is required is related to the $R_S \bullet C_L$ time constant, the R_S needed will initially increase rapidly from zero, and then will decrease as C_L is further increased. A relatively strict requirement, such as for 0.1%, settling will generally require a larger R_S for a given C_L, giving a curve falling higher (in terms of R_S) than that for a less stringent requirement, such as 20% overshoot. For the common gain configuration of +2, these two curves are plotted in the figure for 0.1% settling (upper-most curve) and 20% overshoot (middle curve). It is also worth mentioning that higher closed-loop gains dramatically lessen the problem, and will require less R_S for the same performance. The third (lowermost) curve illustrates this, demonstrating a closed-loop gain of 10 R_S requirement for 20% overshoot for the AD8001 amplifier. This can be related to the earlier discussion associated with Figure 6-70.

The recommended values for R_S will optimize response, but it is important to note that generally C_L will degrade the maximum bandwidth and settling time performance which is achievable. In the limit, a large $R_S \bullet C_L$ time constant will dominate the response. In any given application, the value for R_S should be taken as a starting point in an optimization process which accounts for board parasitics and other secondary effects.

Active or "in-the-loop" cap load compensation can also be used as shown in Figure 6-74, and this scheme modifies the passive configuration, providing feedback correction for the dc and low frequency gain error associated with R_X. In contrast to the passive form, active compensation can only be used with voltage feedback amplifiers, because current feedback amplifiers do not allow the integrating connection of C_F.

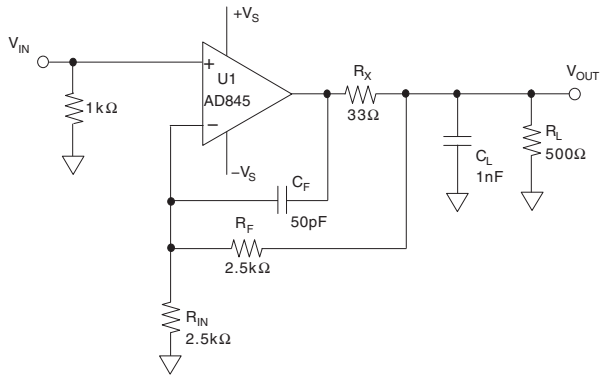


Figure 6-74: Active "in-the-loop" capacitive load compensation corrects for dc and LF gain errors

This circuit returns the dc feedback from the output side of isolation resistor R_X, thus correcting for errors. Ac feedback is returned via C_F, which bypasses R_X/R_F at high frequencies. With an appropriate value of C_F (which varies with C_L for fixed resistances) this stage can be adjusted for a well damped transient response (see References 6 and 7). There is still a bandwidth reduction, a headroom loss, and also (usually) a slew rate reduction, but the dc errors can be very low. A drawback is the need to tune C_F to C_L, as even if this is done well initially, any change to C_L will alter the response away from flat. The circuit as shown is useful

for voltage feedback amplifiers only, because capacitor C_F provides integration around U1. It also can be implemented in inverting fashion, by driving the bottom end of R_{IN}, while grounding the op amp (+) input.

Internal cap load compensation involves the use of an amplifier that has topological provisions for the effects of external cap loading. To the user, this is the most transparent of the various techniques, as it works for any feedback situation, for any value of load capacitance. Drawbacks are that it produces higher distortion than does an otherwise similar amplifier without the network, and the compensation against cap loading is somewhat signal level dependent.

The internal cap load compensated amplifier sounds at first like the best of all possible worlds, since the user need do nothing at all to set it up. Figure 6-75 is a simplified diagram of an AD817 amplifier with internal cap load compensation. The cap load compensation is the C_F-resistor network, which is highlighted by the dotted area within the unity gain output stage of the amplifier. It is important to note at this point that *this RC network only makes its presence felt for certain load conditions*.

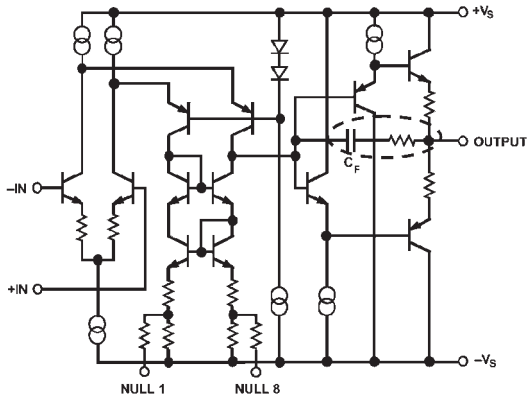


Figure 6-75: AD817 simplified schematic illustrates internal compensation for driving capacitive loads

Under normal (noncapacitive or light resistive) loading, there is limited input/output voltage error across the output stage, so the C_F network then sees a relatively small voltage drop, and has little or no effect on the AD817's high impedance compensation node. However when a capacitor (or other heavy) load is present, the high currents in the output stage produce a voltage difference across the C_F network, which effectively adds capacitance to the compensation node. With this relatively heavy loading, a net larger compensation capacitance results, and reduces the amplifier speed in a manner that is adaptive to the external capacitance, C_L. *As a point of reference, note that it requires 6.3 mA peak current to support a 2 Vp-p swing across a 100 pF load at 10 MHz.*

Since this mechanism is resident in the amplifier output stage and it dynamically affects the overall compensation characteristics, it acts independent of the specific external feedback hookup, as well as the external capacitor's size. In other words, it can be transparent to the user in the sense that no specific design conditions need be set to make it work (other than selecting the right IC). Some amplifiers using internal cap load compensation are the AD817, the AD847, and their dual equivalents, AD826 and AD827.

There are, however, some caveats also associated with this internal compensation scheme. As with the passive compensation techniques, bandwidth decreases as the device slows down to prevent oscillation with

higher load currents. Also, this adaptive compensation network has its greatest effect when enough output current flows to produce significant voltage drop across the C_F network. Conversely, at small signal levels, the effect of the network on speed is less, so greater ringing may actually be possible for some circuits, with lower-level outputs.

The dynamic nature of this internal cap load compensation is illustrated in Figure 6-76, which shows an AD817 unity gain inverter being exercised at both high (left) and low (right) output levels, with common conditions of $V_S = \pm 15$ V, $R_L = 1$ kΩ, $C_L = 1$ nF, and using 1 kΩ input/feedback resistors. In both photos the input signal is on the top trace, the output signal is on the bottom trace, and the time scale is fixed.

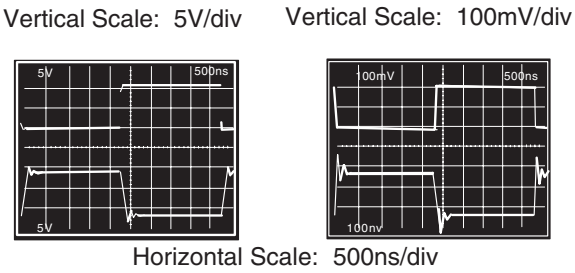


Figure 6-76: Response of internal cap load compensated amplifier varies with signal level

In the 10 V p-p output left photo, the output has slowed down appreciably to accommodate the capacitive load, but settling is still relatively clean, with a small percentage of overshoot. For this high level case, the bandwidth reduction due to C_L is most effective.

In the right photo, the 200 mV p-p output shows greater overshoot and ringing for the lower level signal. The point is that the performance of the cap load compensated amplifier is signal-dependent, but is always stable with any cap load.

Finally, because the circuit is based on a nonlinear principle, the internal network affects distortion performance and load drive ability, and these factors influence amplifier performance in video applications. Though the network's presence does not by any means make devices like the AD817 or AD847 unusable for video, it does not permit the very lowest levels of distortion and differential gain and phase that are achievable with amplifiers without this network, but otherwise comparable.

While the individual techniques for countering cap loading outlined above have various specific trade-offs as noted, all of the techniques have a common drawback of reducing speed (both bandwidth and slew rate). If these parameters cannot be sacrificed, a matched transmission line system is the solution, and is discussed in more detail, in the "Video Amplifiers" portion of this chapter.

As for choosing among the cap load compensation schemes, it would seem on the surface that amplifiers using the internal form offer the best possible solution to the problem—just pick the right amplifier and simply forget about it. And indeed, that would seem the "panacea" for all cap load situations—if you use the "right" amplifier you never need to think about cap loading again. Could there be more to it?

Yes. The "gotcha" of internal cap load compensation is subtle, and lies in the fact that the dynamic adaptive nature of the compensation mechanism actually can produce higher levels of distortion, vis-à-vis an otherwise similar amplifier, *without* the C_F-resistor network. Like the old saying about no free lunches,

to attain top-notch levels of high frequency ac performance, give the issue of whether to use an internally compensated cap load amplifier more serious thought than simply picking a trendy device. For example, the AD818, which is a gain-of-two stable video op amp, offers excellent performance in terms of video gain and phase measurements. It is simply a gain-of-two stable AD817 op amp, but without the internal cap load compensation network. For similar video stage driver applications, the AD817 will not perform as well as the more suitable AD818.

On the other hand, if you have no requirements for the lowest levels of distortion, then such an amplifier as the AD817 could be a very good choice. Such amplifiers are certainly easier to use, and are relatively forgiving about output loading issues.

References: Buffers and Driving Cap Loads

1. George Erdi, "A 300 V/μs Monolithic Voltage Follower," **IEEE Journal of Solid-State Circuits**, Vol. SC-14, No. 6, December, 1979, pp. 1059–1065.
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SECTION 6-3

Video Amplifiers

Walt Kester

Video Signals and Specifications

Before discussing some video applications for op amps, it is a good idea to review some basics regarding video signals and specifications. The standard video format is the specification of how the video signal looks from an electrical point of view. Light strikes the surface of an image sensing device within the camera, producing a voltage level corresponding to the amount of light hitting a particular spatial region of the surface. This information is then placed into the standard format and sequenced out of the camera. Along with the actual light and color information, synchronization pulses are added to the signal to allow the receiving device—a television monitor, for instance—to identify where the sequence is in the frame data.

A standard video format image is read out on a line-by-line basis from left to right, top to bottom. A technique called *interlacing* refers to the reading of all even-numbered lines, top to bottom, followed by all odd lines as shown in Figure 6-77.

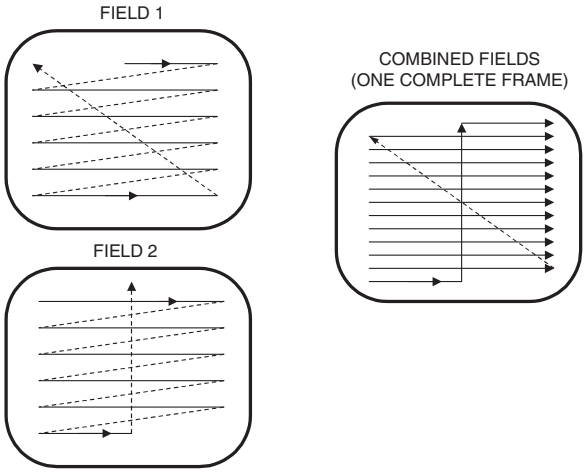


Figure 6-77: Standard broadcast television interlace format

The television picture *frame* is thus divided into even and odd *fields*. Interlacing is used to produce an apparent update of the entire frame in half the time that a full update actually occurs. This results in a television image with less apparent flicker. Typical broadcast television frame update rates are 30 Hz and 25 Hz, depending upon the line frequency. It should be noted that interlacing is not always required in graphics display systems where the refresh rate is usually greater (typically 60 Hz).

The original black and white, or *monochrome*, television specification in the USA is the EIA RS-170 specification that prescribes all timing and voltage level requirements for standard commercial broadcast video

signals. The standard American specification for color signals, NTSC, modifies RS-170 to work with color signals by adding color information to the signal which otherwise contains only brightness information.

A video signal comprises a series of analog television lines. Each line is separated from the next by a synchronization pulse called the *horizontal sync*. The fields of the picture are separated by a longer synchronization pulse, called the *vertical sync*. In the case of a monitor receiving the signal, its electron beam scans the face of the display tube with the brightness of the beam controlled by the amplitude of the video signal. A single line of an NTSC color video signal is shown in Figure 6-78.

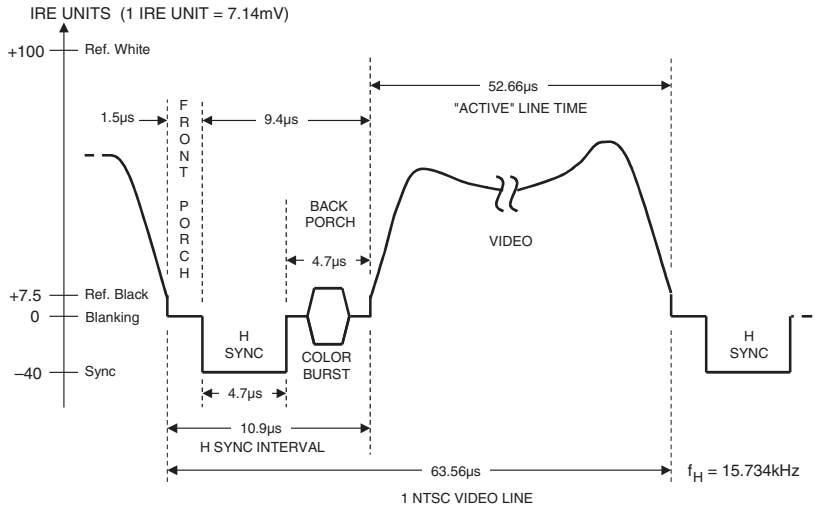


Figure 6-78: NTSC composite color video line

Whenever a horizontal sync pulse is detected, the beam is reset to the left side of the screen and moved down to the next line position. A vertical sync pulse, indicated by a horizontal sync pulse of longer duration, resets the beam to the top left point of the screen to a line centered between the first two lines of the previous scan. This allows the current field to be displayed between the previous one.

A simplified block diagram of the NTSC color processing system is shown in Figure 6-79. The three color signals (RGB: red, green, and blue) from the color camera are combined in a *matrix* unit to produce what is called the *luminance* signal (Y) and two color difference signals (I and Q). These *components* are further combined to produce what is called the *composite* color signal.

In the NTSC system (used in the U.S. and Japan), the color subcarrier frequency is 3.58 MHz. The PAL system (used in the U.K. and Germany) and SECAM system (used in France) use a 4.43 MHz color subcarrier.

In terms of their key frequency differences, a comparison between the NTSC system and the PAL system are given in Figure 6-80.

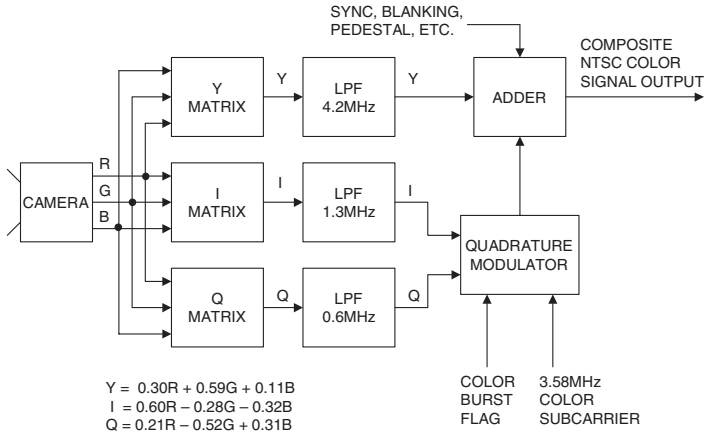


Figure 6-79: Generating the composite NTSC color signal

	NTSC	PAL
Horizontal Lines	525	625
Color Subcarrier Frequency	3.58MHz	4.43MHz
Frame Frequency	30Hz	25Hz
Field Frequency	60Hz	50Hz
Horizontal Sync Frequency	15.734kHz	15.625kHz

Figure 6-80: NTSC and PAL signal characteristics

Differential Gain And Phase Specifications

The color (or *chrominance*) information in the composite video signal is contained in the amplitude and phase of the subcarrier. The *intensity* or *saturation* of the color is determined by the amplitude of the subcarrier signal, and the precise color displayed (i.e., red, green, blue, and combinations) is determined by the phase of the subcarrier signal with respect to the phase of the color burst. The chrominance signal modulates the luminance signal which determines the relative blackness or whiteness of the color. To preserve color fidelity, it is important that the amplitude and phase of a constant-amplitude and phase color subcarrier remain constant across the range of black to white.

Any variation of the *amplitude* of the color subcarrier from black to white levels is called *differential gain* (expressed in %), and any variation in phase with respect to the color subcarrier is called *differential phase* (expressed in degrees). Degradations of up several percent of differential gain and several of degrees differential phase are acceptable for home viewing purposes, but individual components in the video signal path (amplifiers, switches, and so forth) must meet much tighter specifications. This is because the signal must pass through many circuits from the camera to the home. As a result, individual professional video systems have stringent requirements for differential gain and phase, usually limiting changes to less than 0.1% and 0.1°.

These system specifications mandate even more stringent standards for individual components, with the differential gain and differential phase requirements for op amps approaching 0.01% and 0.01°.

Video Formats in Graphics Display Systems

Several system architectures may be used to build a graphics display system. The most general approach is illustrated in Figure 6-81. It consists of a host microprocessor, a graphics controller, three color memory banks or frame buffer, one for each of the primary colors red, green, and blue (only one for monochrome systems). The microprocessor provides the image information to the graphics controller. This information typically includes position and color information. The graphics controller is responsible for interpreting this information and adding the required output signals such as sync, blanking, and memory management signals.

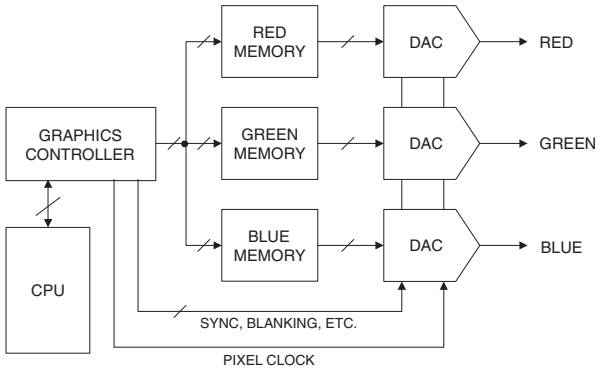


Figure 6-81: Simplified graphics control system for generating RGB signals

Unlike broadcast video, the horizontal and vertical resolution, as well as the refresh rate in a graphics display system, can vary widely depending upon the desired performance. The resolution in such a system is defined in terms of *pixels*: the number of horizontal lines (expressed as pixels) and the number of pixels in each line. For instance, a 640 × 480 monitor has 480 horizontal lines, and each horizontal line is divided into 640 pixels. So a single frame would contain 307,200 pixels. In a color system, each pixel requires RGB intensity data. This data is generally stored as 8- or 10-bit words in the memory.

The memory holds the intensity information for each pixel. The DACs use the words in the memory and information from the memory controller to write the pixel information to the monitor. Special video DACs called "RAMDACs" greatly simplify the storage of the pixel data by using color lookup tables. These DACs also have inputs to facilitate the generation of the sync and blanking signals.

Figure 6-82 shows some typical resolutions and pixel rates for common display systems, assuming a 60 Hz, noninterlaced refresh rate. Standard computer graphics monitors, like television monitors, use a display technique known as *raster scan*. This technique writes information to the screen line by line, left to right, top to bottom, as has been previously discussed. The monitor must receive a great deal of information to display a complete picture. Not only must the intensity information for each pixel be present in the signal, but information must be provided to determine when a new line needs to start (HSYNC) and when a new picture frame should start (VSYNC). The computer industry has generally standardized on formats defined in EIA video standard RS-343A. Unlike broadcast video, the refresh rate can also vary and interlacing may or may not be utilized. The pixel clock frequency gives a good idea of the settling time and bandwidth requirements for any analog component, such as the DAC, which is placed in the path of the RGB signals. The pixel clock frequency can be estimated by finding the product of the horizontal resolution times the vertical resolution times the refresh rate. An additional 30%, called the retrace factor, should be added to allow for overhead.

RESOLUTION	PIXEL RATE
640 × 480	25MHz
800 × 600	38MHz
1024 × 768	65MHz
1280 × 1024	105MHz
1500 × 1500	180MHz
2048 × 2048	330MHz

Pixel Rate ≈ Vertical Resolution × Horizontal Resolution × Refresh Rate × 1.3

Figure 6-82: Typical graphics resolution and pixel rates for 60 Hz noninterlaced refresh rate

Bandwidth Considerations in Video Applications

The bandwidth of an op amp used in a video application must be sufficient so that the video signal is not attenuated or significantly shifted in phase. This generally implies that the bandwidth of the op amp be much greater than that of the maximum video frequency. It is not uncommon to require that amplifiers in the signal path in video equipment such as switchers or special effects generators have 0.1 dB bandwidths of 50 MHz or greater. High definition television requires even higher 0.1 dB bandwidth. Circuit parasitics as well as the load impedance can significantly affect the 0.1 dB bandwidth at high frequencies. This implies careful attention to layout, decoupling, and grounding as well as the use of transmission line techniques at the op amp output. It is common to use source and load terminations with high quality 75 Ω coaxial cable so that the load presented to the op amp output appears as a 150 Ω resistive load. Maintaining accurate control of 0.1 dB bandwidth is almost impossible with reactive loads.

Achieving the highest 0.1 dB bandwidth flatness is therefore important in many video applications. Voltage feedback op amps can be optimized for maximum 0.1dB bandwidth provided the closed-loop gain and load conditions are known. In video applications, closed-loop gains of +1 and +2 are the most common with a 100 Ω or 150 Ω output load, representing the impedance of 50 Ω or 75 Ω source and load terminated cables.

As an example, the AD8074 (G = +1) and AD8075 (G = +2) are triple video buffers optimized for driving source and load terminated 75 Ω cables. These devices use a voltage feedback architecture and have on-chip gain-setting resistors. Figure 6-83 shows the frequency response of the AD8075 buffer on two vertical scales: 1 dB/division and 0.1 dB/division. The plots labeled "GAIN" show a 3 dB bandwidth of 350 MHz (□), and the plots labeled "FLATNESS" show a 0.1 dB bandwidth of 70 MHz (○). Note that the small-signal (200 mV p-p) and large-signal (2 V p-p) bandwidths are approximately equal.

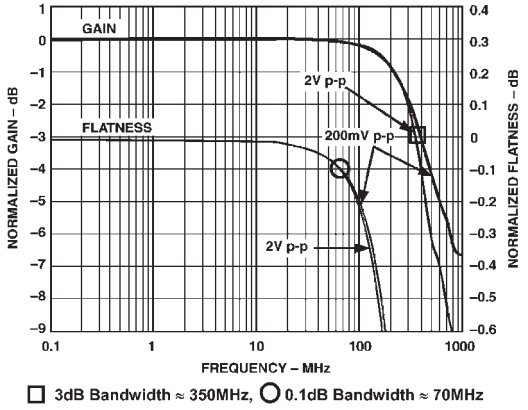


Figure 6-83: AD8075 triple video buffer gain and gain flatness, G = +2, R_L = 150 Ω

Voltage feedback op amps are optimized for bandwidth flatness by adjusting both the compensation capacitor, which sets the dominant pole, and the external feedback network. However, because of the critical relationship between the feedback resistor and the bandwidth of a current feedback op amp, optimum bandwidth flatness is highly dependent on the feedback resistor value, the resistor parasitics, as well as the op amp package and PCB parasitics. Figure 6-84 shows the bandwidth flatness (0.1 dB/division) plotted versus the feedback resistance for the AD8001 in a noninverting gain of 2. The 100 Ω load resistor represents a source and load terminated 50 Ω cable. These plots were made using the AD8001 evaluation board with surface mount resistors.

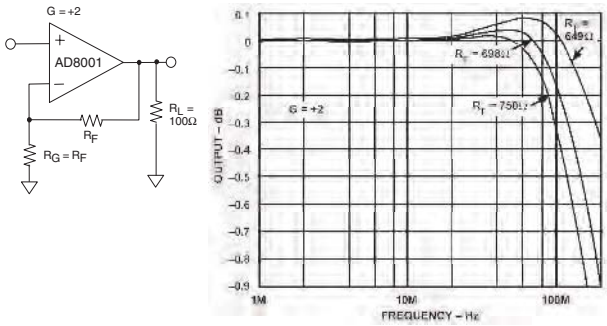
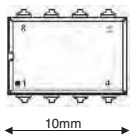


Figure 6-84: AD8001 current feedback op amp bandwidth flatness versus feedback resistor value

It is recommended that once the optimum resistor values have been determined, 1% tolerance values should be used. In addition, resistors of different construction have different associated parasitic capacitance and inductance. Surface-mount resistors are an optimum choice, thus leaded components aren't recommended for high frequency use.

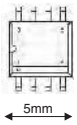
Slightly different resistor values may be required to achieve optimum performance of the AD8001 in the DIP versus the SOIC packages (see Figure 6-85). The SOIC package exhibits slightly lower parasitic capacitance and inductance than the DIP. The data shows the optimum feedback (R_G) and feedforward (R_F) resistors for highest 0.1 dB bandwidth for the AD8001 in the DIP and the SOIC packages. As you might suspect, the SOIC package can be optimized for higher 0.1 dB bandwidth because of lower parasitics.

AD8001AN
(DIP)



GAIN	–1	+1	+1
R_F	649Ω	1050Ω	750Ω
R_G	649Ω	-	750Ω
0.1dB Flatness	105MHz	70MHz	105MHz

AD8001AR
(SOIC)



GAIN	–1	+1	+1
R_F	604Ω	953Ω	681Ω
R_G	604Ω	-	681Ω
0.1dB Flatness	130MHz	100MHz	120MHz

Figure 6-85: Optimum values of R_F and R_G for AD8001 DIP and SOIC packages for maximum 0.1 dB bandwidth

As has been discussed, the current feedback op amp is relatively insensitive to capacitance on the inverting input when it is used in the inverting mode (as in an I/V application). This is because the low inverting input impedance is in parallel with the external capacitance and tends to minimize its effect. In the noninverting mode, however, even a few picofarads of stray inverting input capacitance may cause peaking and instability. Figure 6-86 shows the effects of adding summing junction capacitance to the inverting input of the

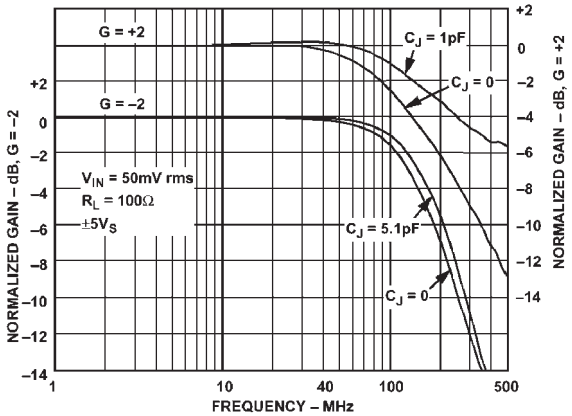


Figure 6-86: AD8004 current feedback op amp sensitivity to inverting input capacitance for G = +2, G = –2

AD8004 (SOIC package) for G = +2. Note that only 1 pF of added inverting input capacitance (C_J) causes a significant increase in bandwidth and an increase in peaking. For G = –2, however, 5 pF of additional inverting input capacitance causes only a small increase in bandwidth and no significant increase in peaking.

It should be noted that high-speed voltage feedback op amps are sensitive to stray inverting input capacitance when used in either the inverting or noninverting mode, because both positive and negative inputs are high impedance.

Video Signal Transmission

High quality video signals are best transmitted over terminated coaxial cable having a controlled characteristic impedance. The characteristic impedance is given by the equation $Z_0 = \sqrt{(L/C)}$ where L is the distributed inductance per foot, and C is the distributed capacitance per foot. Popular values are 50 Ω, 75 Ω, and 93 Ω or 100 Ω.

If a length of coaxial cable is properly terminated, it presents a *resistive* load to the driver. If left unterminated, however, it may present a predominately capacitive load to the driver depending on the output frequency. If the length of an unterminated cable is much less than the wavelength of the output frequency of the driver, the load appears approximately as a lumped capacitance. For instance, at the audio frequency of 20 kHz (wavelength ≈ 50,000 feet, or 9.5 miles), a 5-foot length of unterminated 50 Ω coaxial cable would appear as a lumped capacitance of approximately 150 pF (the distributed capacitance of coaxial cable is about 30 pF/ft).

At 100 MHz (wavelength ≈ 10 feet), however, the unterminated coax must be treated as a transmission line in order to calculate the standing wave pattern and the voltage at the unterminated cable output. Figure 6-87 summarizes transmission line behavior for different frequencies.

- All interconnections are really transmission lines which have a characteristic impedance (even if not controlled).
- The characteristic impedance is equal to $\sqrt{(L/C)}$, where L and C are the distributed inductance and capacitance.
- Correctly terminated transmission lines have impedances equal to their characteristic impedance.
- Unterminated transmission lines behave approximately as lumped capacitance if the wavelength of the output frequency is much greater than the length of the cable.
  - Example: At 20kHz (wavelength = 9.5 miles), 5 feet of unterminated 50Ωcable (30pF/ft) appears like a 150pF load
  - Example: At 100MHz, (wavelength = 10 feet), 5 feet of 50Ω must be properly terminated to prevent reflections and standing waves.

Figure 6-87: Driving cables

Because of skin effect and wire resistance, coaxial cable exhibits a loss that is a function of frequency. This varies considerably between cable types. For instance at 100 MHz the attenuation RG188A/U is 8 dB/100 ft, RG58/U is 5.5 dB/100 ft, and RG59/U 3.6 dB/100 ft (see Reference 4). Skin effect also affects the pulse response of long coaxial cables. The response to a fast pulse will rise sharply for the first 50% of the output swing, then taper off during the remaining portion of the edge. Calculations show that the 10% to 90% waveform risetime is 30 times greater than the 0% to 50% rise time when the cable is skin effect limited (Reference 4).

Transmission Line Driver Lab

It is useful to examine the fidelity of a pulse signal, for conditions of proper/improper transmission line source/load terminations. Some lab experiments were set up to do this.

To illustrate the behavior of a high speed op amp driving a coaxial cable, consider the circuit of Figure 6-88. Here the AD8001 drives 5 feet of 50 Ω coaxial cable, which is load-end terminated in the characteristic impedance of 50 Ω. No termination is used at the amplifier (driving) end. The pulse response is also shown in the figure.

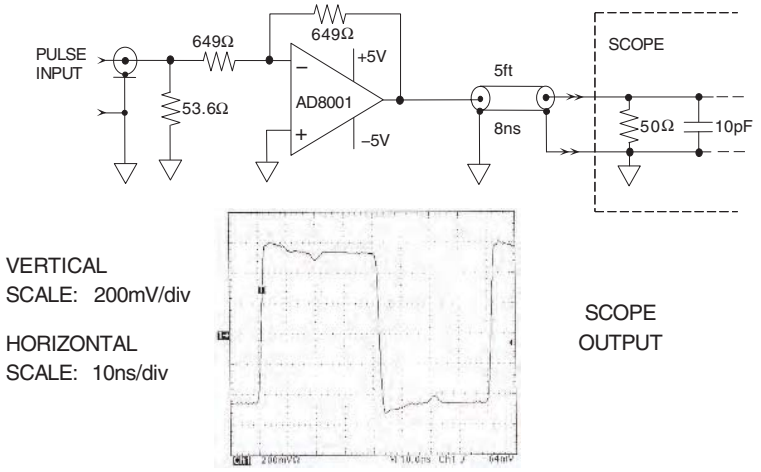


Figure 6-88: Pulse response of AD8001 driving 5 feet of load-only terminated 50 Ω coaxial cable

The output of the cable was measured by connecting it directly to the 50 Ω input of a 500 MHz Tektronix 644A digitizing oscilloscope. The 50 Ω resistor termination is actually the input of the scope. However, this 50 Ω load is not a perfect line termination, it is lower at high frequencies (due to the scope shunt input capacitance of about 10 pF).

As a consequence some of the positive going pulse edge is reflected out of phase to the source. When this reflection reaches the op amp, it sees the op amp closed-loop output impedance, which, at 100 MHz, is approximately 100 Ω (higher than line impedance).

Upon arriving at the op amp output, the negative-going reflection from the load is then rereflected back towards the load, without undergoing another phase reversal. This then accounts for the negative going "blip" seen on the upper plateau of the waveform, which occurs approximately 16 ns after the leading edge. This time difference is equal to the round-trip delay of the cable (2 • 5ft • 1.6 ns/ft = 16 ns). An additional point worth noting is that, in the frequency domain (which is not shown by these tests) the cable mismatch will also cause a loss of bandwidth flatness at the load.

Figure 6-89 shows a second case, the results of driving the same coaxial cable, but now used with both a 50 Ω source-end as well as the 50 Ω load-end termination at the scope. It should be noted that this case is the preferred way to drive a transmission line, because a portion of the reflection from the load impedance mismatch is absorbed by the amplifier's source termination resistor of 50 Ω. A disadvantage is that there is a gain loss of 6 dB, because of the 2/1 voltage division which occurs between the equal value source and load terminations, i.e., 50 Ω/50 Ω.

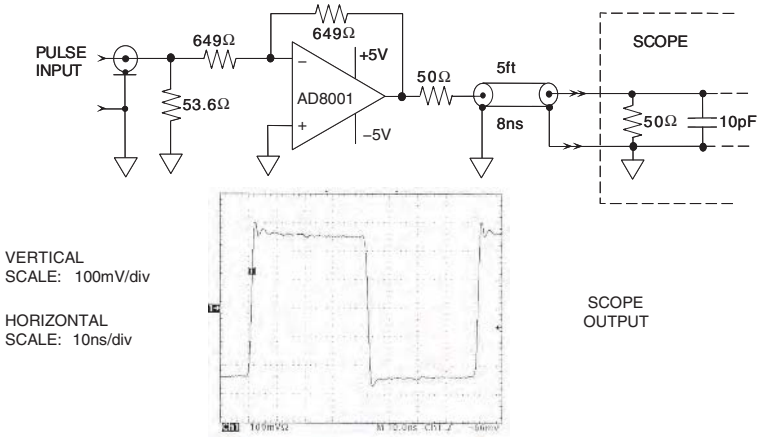


Figure 6-89: Pulse response of AD8001 driving 5 feet of source and load terminated 50 Ω coaxial cable

However, a major positive attribute of this configuration, with the line impedance matched source and load terminations in conjunction with a low-loss cable, is that *the best bandwidth flatness is ensured*, especially at lower operating frequencies. In addition to this, the amplifier is operated with a near optimum load condition, i.e., into a resistive load. The load in this case is 50 Ω plus 50 Ω, or 100 Ω. In general, it will be twice the impedance of the transmission line in use, i.e., 150 Ω for a 75 Ω line, and so forth.

In practice, the gain loss associated with the 2/1 source/load impedance is easily made up, simply by operating the line driver stage at a gain of 2x. Typically, video driver stages are noninverting to preserve the waveform sign, and operate at a fixed and precise gain of 2 times. Thus they will inherently provide a net signal transfer gain of unity, as measured from input to the final end-of-line load termination (this neglects any associated transmission line losses, and assumes precise resistor ratios for the gain resistors). Another very practical point is that the same driver can be used for a wide variety of transmission lines, simply by changing the value of the source termination resistor.

Source-end (only) terminations can also be used as shown in Figure 6-90, where the op amp is now source-terminated by the 50 Ω resistor which drives the cable. At the load end, the scope is set for 1 MΩ input impedance, which represents an approximate open circuit. The initial leading edge of the pulse at the op amp output sees a 100 Ω load (the 50 Ω source resistor in series with the 50 Ω coax impedance. When the pulse reaches the load, a large portion is reflected in phase, because of the high load impedance, resulting in a full-amplitude pulse at the load. When the reflection reaches the source-end of the cable, it sees the 50 Ω source resistance in series with the op amp closed-loop output impedance (approximately 100 Ω at the frequency represented by the 2 ns rise time pulse edge). The rereflected portion remains in phase, and then appears at the scope input as the positive going "blip," approximately 16 ns after the leading edge.

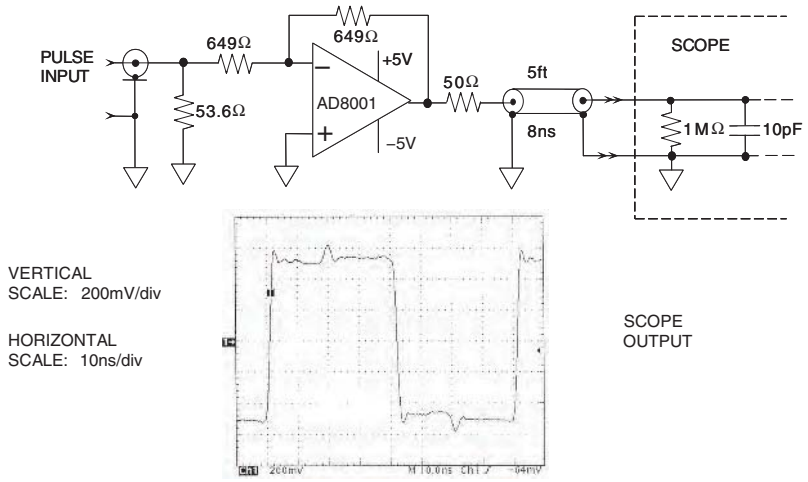


Figure 6-90: Pulse response of AD8001 driving 5 feet of source-only terminated 50 Ω coaxial cable

From these experiments, one can easily see that the preferred method for minimum reflections (and therefore maximum bandwidth flatness) is to use both source and load terminations and try to minimize any reactance associated with the load. The experiments represent a worst-case condition, where the frequencies contained in the fast edges are greater than 100 MHz. (using the rule-of-thumb that bandwidth = 0.35/rise time).

At less demanding video frequencies, either load-only, or source-only terminations may give acceptable results, but the op amp data sheet should always be consulted to determine the op amp's closed-loop output impedance at the maximum frequency of interest; i.e., is it less than the line impedance? A major disadvantage of the source-only termination is that it requires a truly high impedance load (high resistance and minimal parasitic capacitance) for minimum absorption of energy. It also places a burden on the driving amplifier, to maintain the low output impedance at high frequencies.

Now, for a truly worst-case, let us replace the 5 feet of coaxial cable with an uncontrolled-impedance cable (one that is largely capacitive with little inductance). Also, let's use a capacitance of 150 pF to simulate the cable (corresponding to the total capacitance of 5 feet of coaxial cable, whose distributed capacitance is about 30 pF/foot). Figure 6-91 shows the output of the AD8001 op amp, driving a lumped 160 pF capacitance (including the scope input capacitance of 10 pF).

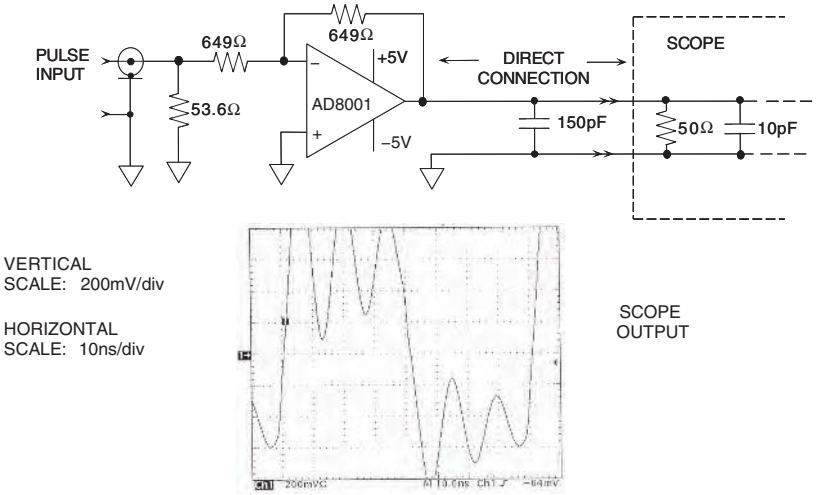


Figure 6-91: Pulse response of AD8001 driving 160 pF||50 Ω load

Overshoot and severe ringing on the pulse waveform is noted, due to the capacitive loading. This example illustrates the need to use good quality controlled-impedance coaxial cable in the transmission of high frequency signals, even over short distances. Failure to adhere to controlled-impedance lines for signal distribution can result in severe loss of pulse waveform fidelity, and loss of bandwidth flatness in the frequency domain.

To summarize, transmission line driver circuits should use proper line terminations for best response. The ideal method of line termination is matching line-impedance-value resistances at both source and load end (Figure 6-89). The associated 6dB gain loss is easily made up in the amplifier. Next best is a source-only termination (Figure 6-90), with due care towards maintaining a high impedance at the load end, and a low drive impedance amplifier. This type of termination provides near-full amplitude level at the load end, making the gain of the driver less critical. Load-only termination can also be used (Figure 6-88), but may be more critical of load end parasitic effects and the amplifier performance. It also provides near-full amplitude level at the load end.

Direct drive of uncontrolled load impedances, especially lumped capacitive lines, should be avoided wherever signal fidelity is important (Figure 6-91).

Video Line Drivers

The AD8047 and AD8048 voltage feedback op amps have been optimized to offer outstanding performance as video line drivers. They utilize the "quad core" g_m stage as previously described for high slew rate and low distortion (see Chapter 1). The AD8048 (optimized for G = +2) has a differential gain of 0.01% and a differential phase of 0.02°, making it well suited for HDTV applications.

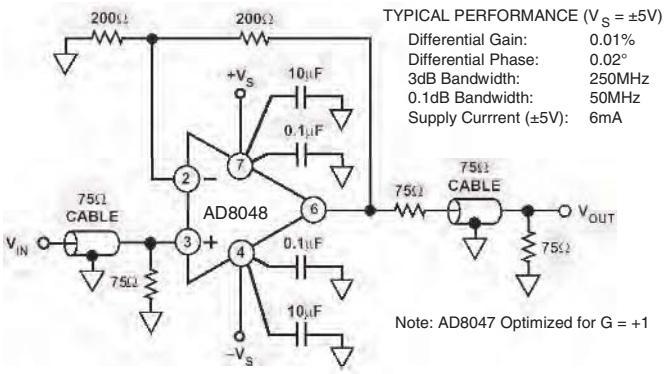


Figure 6-92: High performance video line driver using the AD8048

In the configuration using the AD8048 shown in Figure 6-92, the 0.1 dB bandwidth is 50 MHz for ±5 V supplies, slew rate is 1000 V/μs, and 0.1% settling time is 13 ns. The total quiescent current is 6 mA (±5 V), and quiescent power dissipation 60mW. Performance of this circuit will be optimum with the gain-of-two stable AD8048 op amp, as its parameters have been optimized for this gain. Alternately, if a gain-of-one stable op amp is desired, the AD8047 can be used.

Note that a very wide variety of both voltage feedback and current feedback devices can be used similarly as a gain-of-two line driver (although the required feedback resistances may vary by device). Examples would be the AD818/AD828, AD8055/AD8056, AD8057/AD8058, and AD8061/AD8062/AD8063 families of voltage feedback op amps, and the AD811/AD812/AD813, AD8001/AD8002, AD8012 families as a partial list. There are differences among all of these devices for applicable supply ranges, single-supply compatibility, and so forth, so consult device data sheets.

It is often desirable to drive more than one coaxial cable, which represents a dc load of 150 Ω to a driver. The typical maximum video signal level is 1 V into 75 Ω, which represents 2 V at the output of the driver, and a current of 13.3 mA. Thus a 50 mA output current video op amp such as the AD8047 or AD8048 would theoretically be capable of driving three source and load-terminated 75 Ω loads. But, there are other important subtle considerations for this application. Differential gain and phase may be degraded for high output currents. Also, the op amp closed-loop output impedance affects crosstalk between the driven output channels. So it is often better to select a video driver fully specified for the required fan-out and load, especially if the fan-out is greater than two.

Video Distribution Amplifier

The AD8010 op amp is optimized for driving multiple video loads in parallel. Video performance of 0.02% differential gain and 0.03% differential phase is maintained, while driving eight 75 Ω source and load-terminated video lines. The AD8010 uses the current feedback architecture and has a 0.1 dB bandwidth of 60 MHz with eight video loads. Typical supply current (neglecting load current) is 15.5 mA on ±5 V supplies. A typical connection diagram is shown in Figure 6-93. The AD8010 is offered in three packages: an 8-lead DIP (θ_{JA} = 90ºC/W), 16-lead wide body SOIC (θ_{JA} = 73ºC/W), and a low thermal resistance, 8-lead SOIC (θ_{JA} = 122ºC/W).

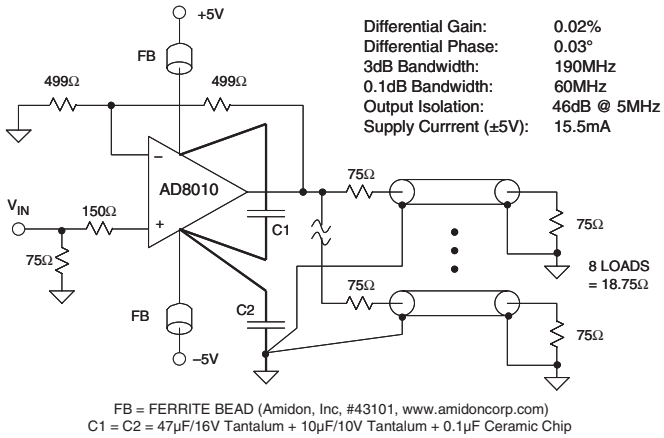


Figure 6-93: The AD8010 video distribution amplifier

The power supply decoupling scheme used for the AD8010 requires special attention. The conventional technique of bypassing each power supply pin individually to ground can have an adverse effect on the differential phase error of the circuit. This is because there is an internal compensation capacitor in the AD8010 that is referenced to the negative supply. The recommended technique shown in Figure 6-93 is to connect three parallel bypass capacitors from the positive supply to the negative supply, and then to bypass the negative supply to ground with a similar set, as shown. For high frequency decoupling, 0.1 µF ceramic surface-mount capacitors are recommended. The high currents that can flow through the power supply pins require additional large tantalum electrolytic decoupling capacitors. As shown, a 47 µF/16 V tantalum in parallel with a 10 µF/10 V tantalum capacitor is desirable. The grounded side of the C2 capacitors bypassing the negative supply should be brought to a single-point output return ground. In addition to the bypass capacitors described above, ferrite beads such as those noted should be placed in series with both positive and negative supplies for further decoupling.

Another important consideration for driving multiple cables is high frequency isolation between the outputs. Due largely to its low output impedance, the AD8010 achieves better than 46 dB output-to-output isolation at 5 MHz, while driving 75 Ω source and load-terminated cables.

Differential Line Drivers/Receivers

There are a number of applications for differential signal drivers and receivers. Among these are analog-digital-converter (ADC) input buffers, where differential operation can provide lower levels of second-order distortion for certain converters. Other uses include high frequency bridge excitation, and drivers for balanced transmission twisted pair lines such as in ADSL and HDSL.

The transmission of high quality signals across noisy interfaces (either between individual PC boards or between racks) has always been a challenge to designers. Differential techniques using high common-mode rejection ratio (CMRR) instrumentation amplifiers largely solves the problem at low frequencies. Examples of this have already been discussed, under the "Audio Amplifiers" portion of this chapter.

At audio frequencies, transformers, or products such as the SSM2142 balanced line driver and SSM2141/SSM2143 line receivers offer outstanding CMRRs and the ability to transmit low level signals in the presence of large amounts of noise, as noted. At high frequencies, small bifilar-wound toroid transformers are effective.

In contrast to this, the problem of signal transmission at video frequencies is a more complex one. Transformers suitable for video coupling aren't very effective, because the baseband video signal has low frequency components down to a few tens of Hz, and an upper bandwidth limit that can be in the tens (hundreds) of MHz. This make a workable video transformer an item extremely difficult to make.

Another point is that video signals are generally processed in single-ended form, and therefore don't adapt easily to balanced transmission line techniques. Related to this, shielded twin-conductor coaxial cable with good bandwidth is usually somewhat bulky and expensive, and has not found great acceptance.

As a result of these factors, designing high bandwidth, low distortion differential video drivers and receivers with high CMRR at high frequencies is an extremely difficult task.

Nevertheless, even in the face of all of the above problems, there are various differential techniques available right now that offer distinct advantages over single-ended methods. Some of these techniques make use of discrete components, while others utilize state-of-the-art video differential amplifiers.

Approaches To Video Differential Driving/Receiving

Two solutions to differential transmission and reception are shown in Figure 6-94. One is the ideal case (top), where a balanced differential driver drives a balanced twin-conductor coaxial cable, which then drives a terminated differential line receiver. However, as discussed, this circuit is difficult to implement fully at video frequencies.

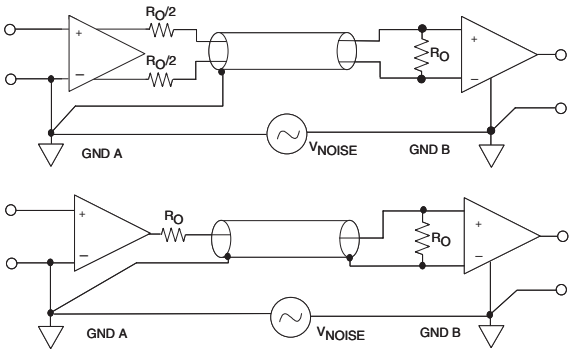


Figure 6-94: Two approaches to differential line driving and receiving

A second, most often used approach uses a single-ended driver driving a source-terminated coaxial cable (bottom), with the cable shield grounded at the transmitter. At the receiver, the coaxial cable is terminated in its characteristic impedance, but the shield is left floating in order to prevent a ground loop between the two systems. Common-mode ground noise is rejected by the CMRR of the differential line receiver.

Inverter-Follower Differential Driver

The circuit of Figure 6-95 is a useful differential driver for high speed 10-12-bit ADCs, differential video lines, and other balanced loads at 1–4 V rms output levels.

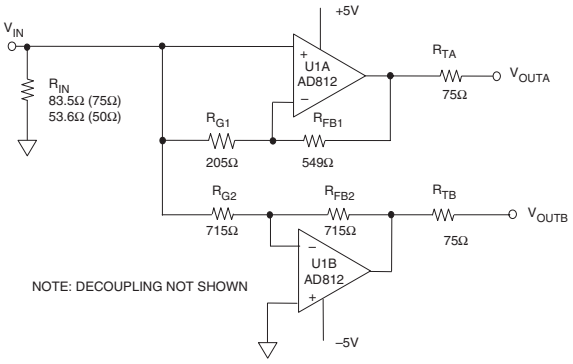


Figure 6-95: Differential driver using an inverter and a follower

It is shown operating from ±5 V supplies, but it can also be adapted to supplies in the range of ±5 to ±15 V. When operated directly from ±5 V as here, it minimizes potential for destructive ADC overdrive when higher supply voltage buffers drive a ±5 V powered ADC, in addition to also minimizing driver power.

In many of these differential drivers the performance criteria is often high. In addition to low output distortion, the two signals should maintain gain and phase flatness. In this topology, two sections of an AD812 dual current feedback amplifier are used for the channel A and B buffers. This provides inherently better open-loop bandwidth matching than using two singles, where bandwidth varies between different manufacturing lots. The two buffers here operate with precise gains of ±1, as defined by their respective feedback and input resistances. Channel B buffer U1B is conventional, and uses a matched pair of 715 Ω resistors—an optimum value for the AD812 on ±5 V supplies.

In channel A, noninverting buffer U1A has an inherent signal gain of 1, by virtue of the bootstrapped feedback network R_{FB1} and R_{G1} (see Reference 5). It also has a higher noise gain, for phase matching. Normally a current feedback amplifier operating as a simple unity gain follower would use one (optimum) resistor R_{FB1}, and no gain resistor at all. Here, with input resistor R_{G1} added, a U1A noise gain like that of U1B results. Due to the bootstrap connection of R_{FB1}-R_{G1}, the signal gain is maintained at unity. Given the matched open-loop bandwidths of U1A and U1B, similar noise gains in the A-B channels provide closely matched output bandwidths between the driver sides, a distinction that greatly impacts overall matching performance.

In setting up a design for the driver, the effects of resistor gain errors should be considered for R_{G2}-R_{FB2}. Here a worst-case 2% mismatch will result in less than 0.2 dB gain error between channels A and B. This error can be improved simply by specifying tighter resistor ratio matching, avoiding trimming.

If desired, phase match can be trimmed via R_{G1}, so that the phase of channel A matches that of B. This can be done by using a pair of closely matched (0.1% or better) resistors to sum the A and B channels, as R_{G1} is adjusted for the best null conditions at the sum node. The A-B gain and phase matching is quite effective in this driver; the test results of the circuit as shown 0.04 dB and 0.1° between the A and B output signals at 10 MHz, when operated into dual 150 Ω loads. The 3 dB bandwidth of the driver is about 60 MHz.

Net input impedance of the circuit is set to a standard line termination value such as 75 Ω (or 50 Ω), by choosing R_{IN} so that the desired value results when paralleled with $R_{G2.}$ In this example, an R_{IN} value of 83.5Ω provides a standard input impedance of 75 Ω when paralleled with 715 Ω. For the circuit just as shown, dual voltage feedback amplifier types with sufficiently high speed and low distortion can also be used. This allows greater freedom with regard to resistor values using such devices as the AD826 and AD828.

Gain of the circuit can be changed if desired, but this isn't totally straightforward. An easy step to satisfy diverse gain requirements is to simply use a triple amplifier such as the AD813 or AD8013, with the third channel as a variable gain input buffer. Note that if an amplifier is used with specifications substantially different than the AD812, some adjustment of resistor values may be necessary.

Cross-Coupled Differential Driver

Another differential driver approach uses cross-coupled feedback to get very high CMR and complementary outputs at the same time. In Figure 6-96, AD8002 dual current feedback amplifier sections are used as cross-coupled inverters, the outputs are forced equal and opposite, assuring zero output common-mode voltage (see Reference 6).

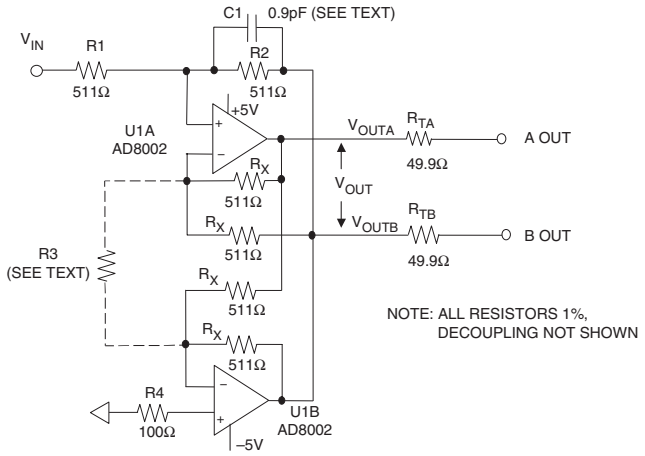


Figure 6-96: Cross-coupled differential driver provides balanced outputs and 250 MHz bandwidth

The gain cell that results, U1A and U1B plus cross-coupling resistances R_X, is fundamentally a differential input/output topology, but it behaves as a voltage feedback amplifier with regard to the feedback port at the U1A (+) node. The V_{IN} to V_{OUT} gain is:

$$G = \frac{V_{OUT}}{V_{IN}} = \frac{2R2}{R1} \qquad \text{Eq. 6-21}$$

where V_{OUT} is the differential output, equal to $V_{OUTA}–V_{OUTB}$.

The relationship of Eq. 6-21 may not be obvious, so it can be derived as follows:

Using the conventional inverting op amp gain equation, the input voltage V_{IN} develops an output voltage V_{OUTB} given by:

$$V_{OUTB} = -V_{IN}\frac{R2}{R1} \qquad \text{Eq. 6-22}$$

Also, $V_{OUTA} = -V_{OUTB}$, because V_{OUTA} is inverted by U1B.

However, $V_{OUT} = V_{OUTA} - V_{OUTB} = -2\,V_{OUTB}$.

Therefore,

$$V_{OUT} = -2\left(-V_{IN}\frac{R2}{R1}\right) = 2V_{IN}\frac{R2}{R1} \qquad \text{Eq. 6-23}$$

and

$$\frac{V_{OUT}}{V_{IN}} = \frac{2R2}{R1}. \qquad \text{Eq. 6-24}$$

This circuit has some unique benefits. First, the differential voltage gain is set by a single resistor ratio, so there is no necessity for side-side resistor matching with gain changes, as is the case for conventional differential amplifiers (see line receivers, below). Second, because the (overall) circuit emulates a voltage feedback amplifier, these gain resistances are not as restrictive as in the case of a conventional current feedback amplifier. Thus, they are not highly critical as to value as long as the equivalent resistance seen by U1A is reasonably low (≤1 kΩ in this case).

A third and important advantage is that cell bandwidth can be optimized to a desired gain by a single optional resistor, R3, as follows. If, for instance, a gain of 20 is desired (R2/R1=10), the bandwidth would otherwise be reduced by roughly this amount, since without R3, the cell operates with a constant gain-bandwidth product (voltage feedback mode). With R3 present however, advantage can be taken of the AD8002 current feedback amplifier characteristics. Additional internal gain is added by the connection of R3, which, given the appropriate value, effectively raises gain-bandwidth to a level so as to restore the bandwidth which would otherwise be lost by the higher closed loop gain.

In the circuit as shown, no R3 is necessary at the low working gain of 2, since the 511 Ω R_X resistors are already optimized for maximum bandwidth. Note that these four matched R_X resistances are somewhat critical, and will change in absolute value with the use of another current feedback amplifier. At higher gain closed loop gains, R3 can be chosen to optimize the working transconductance in the input stages of U1A and U1B, as follows:

$$R3 \cong \frac{R_X}{(R2/R1) - 1} \qquad \text{Eq. 6-25}$$

As in any high speed inverting feedback amplifier, a small high-Q chip type feedback capacitance, C1, may be needed to optimize flatness of frequency response. In this example, a 0.9 pF value was found optimum for minimizing peaking. In general, provision should be made on the PC layout for an NPO chip capacitor in the range of 0.5 pF–2 pF. This capacitor is then value selected at board characterization for optimum frequency response.

Performance for the circuit of Figure 6-96 was examined with a dual trace, 1 MHz–500 MHz swept frequency response plot, as is shown in Figure 6-97. The test output levels were 0 dBm into matched 50 Ω loads, through back termination resistances R_{TA} and R_{TB}, as measured at V_{OUTA} and V_{OUTB}.

In this plot the vertical scale is 2 dB/div, and it shows the 3 dB bandwidth of the driver measuring about 250 MHz, with peaking about 0.1 dB. The four R_X resistors, along with R_{TA} and R_{TB} control low frequency amplitude matching, which was within 0.1 dB in the lab tests, using 511 Ω 1% resistor types. For tightest amplitude matching, these resistor ratios can be more closely controlled.

Due to the very high gain bandwidths involved with the AD8002, the construction of this circuit should only be undertaken by following RF rules. This includes the use of a heavy ground plane, and the use chip

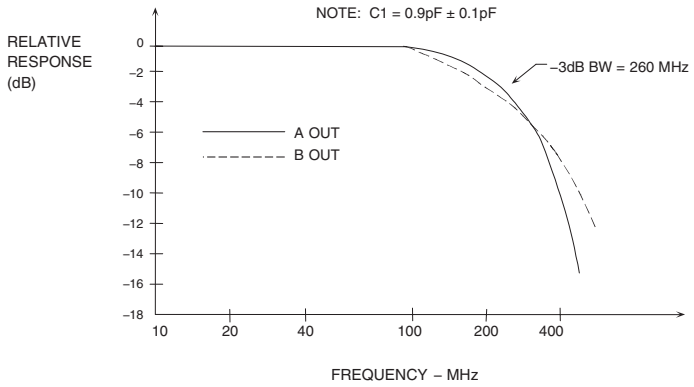


Figure 6-97: Frequency response of AD8002 cross-coupled driver

bypass capacitors of zero lead length at the ±5 V supply pins. For lowest parasitic effect and low inductance, chip style resistors are also recommended for this circuit (see Reference 7). The optimization of C1 has already been noted, above. While a chip style NP0 is good in general for C1, a small film trimmer may also be useful, as it will allow optimizing peaking on an individual circuit basis.

Although this circuit example illustrates a wideband video driver, it should be noted that lower bandwidth applications could also find this push-pull topology useful. An audio frequency application could, for example, use an AD812 for U1A and U1B, or pair of AD811s. Operating on ±15 V, these will allow a high level of balanced, linear output.

Fully Integrated Differential Drivers

A block diagram of the new AD813x family of fully differential amplifiers optimized for differential driving is shown in Figure 6-98. Figure 6-98A shows the details of the internal circuit, and Figure 6-98B shows the equivalent circuit. The gain is set by the external R_F and R_G resistors, and the common-mode voltage is

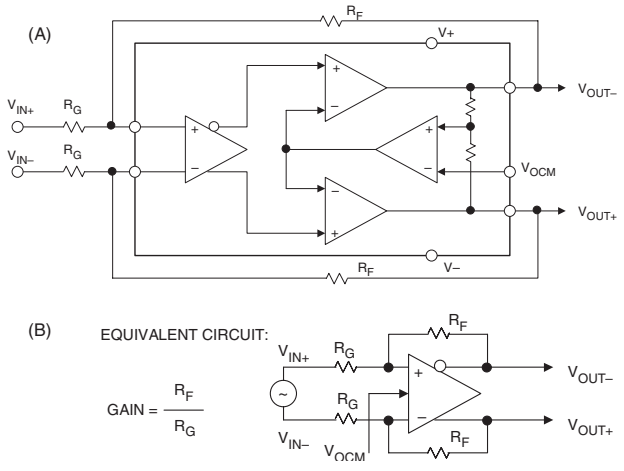


Figure 6-98: AD8138 differential driver amplifier functional schematic (A) and equivalent circuit (B)

set by the voltage on the V_{OCM} pin. The internal common-mode feedback forces the V_{OUT+} and V_{OUT-} outputs to be balanced, i.e., the signals at the two outputs are always equal in amplitude but 180° out of phase per the equation:

$$V_{OCM} = (V_{OUT+} + V_{OUT-})/2 \qquad \text{Eq. 6-26}$$

The circuit can be used with either a differential or a single-ended input, and the voltage gain is equal to the ratio of R_F to R_G.

The AD8138 has a 3 dB small-signal bandwidth of 320 MHz (G = +1) and is designed to give low harmonic distortion as an ADC driver (see Chapter 3). The circuit provides excellent output gain and phase matching, and the balanced structure suppresses even-order harmonics.

It should be noted that the AD8131 differential driver is a sister device to the AD8138 in terms of the function illustrated in Figure 6-98A, and includes internal gain-set resistors.

A 4-Resistor Differential Line Receiver

Figure 6-99 shows a low cost, medium performance line receiver using a high speed op amp that is rated for video use. It is actually a standard 4-resistor difference amplifier optimized for high speed, with a differential to single-ended gain of R2/R1. Using low value, dc-accurate, ac-trimmed resistances for R1–R4, and a high speed, high CMR op amp, provides the good performance.

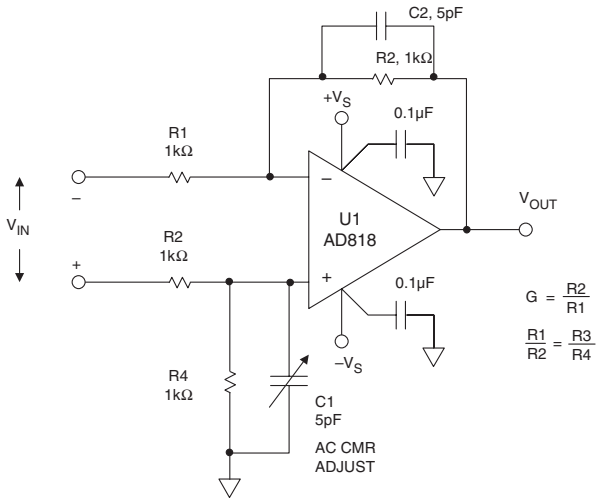


Figure 6-99: Simple video line receiver using the AD818 op amp

Practically speaking, however, at low frequencies resistor matching can be more critical to overall CMR than the rated CMR of the op amp. For example, the worst-case CMR (in dB) of this circuit due to resistor mismatch is:

$$CMR = 20\log_{10}\left(\frac{1+\frac{R2}{R1}}{4Kr}\right) \qquad \text{Eq. 6-27}$$

In this expression *Kr* is a single resistor tolerance in fractional form (1% = 0.01, and so forth), and it is assumed the amplifier has significantly higher CMR (100 dB). Using discrete 1% metal films for R1/R2 and R3/R4 yields a worst-case CMR of 34 dB, 0.1% types 54 dB, and so forth. Of course four random 1% resistors will on the average yield a CMR better than 34 dB, but not dramatically so. A single substrate dual matched pair thin film network is preferred, for reasons of best noise rejection and simplicity. One type suitable is the Vishay VTF series part 1005, (see Reference 7) which has a ratio match of 0.1%, and will provide a worst-case low frequency CMR of 66 dB.

This circuit has an interesting and desirable side property. Because of the resistors it divides down the input voltage, and the amplifier is protected against overvoltage. This allows CM voltages to exceed ±5 V supply rails in some cases without hazard. For operation with ±15 V supplies, inputs should not exceed the supply rails.

At frequencies above 1 MHz, the bridge balance is dominated by ac effects, and a C1-C2 capacitive balance trim should be used for best performance. The C1 adjustment is intended to allow this, providing for the cancellation of stray layout capacitance(s) by electrically matching the net C1-C2 values.

Within a given PC layout with low and stable parasitic capacitance, C1 is best adjusted once in 0.5 pF increments, for best high frequency CMR. Using designated PC pads, production values would then use the trimmed value. Good ac matching is essential to achieving good high frequency CMR. C1-C2 should be physically similar types, such as NPO ceramic chip capacitors.

While the circuit as shown has unity gain, it can be gain-scaled in discrete steps, as long as the noted resistor ratios are maintained. In practice, this means using taps on a multi-ratio network for gain change, so as to raise both R2 and R4, in identical proportions. There is no other simple way to change gain in this receiver circuit.

Alternately, a scheme for continuous gain control without interaction with CMR is to simply follow this receiver with a scaling amplifier/driver, with adjustable gain. The use of an AD828 amplifier (AD818 dual) allows this, with the addition of only two resistors.

Video gain/phase performance of this stage is dependent upon the device used for U1 and the operating supply voltages. Suitable voltage feedback amplifiers work best at supplies of ±10 to ±15 V, which maximizes op amp bandwidth. And, while many high speed amplifiers function in this circuit, those expressly designed with very low distortion video operation perform best.

The circuit just as shown can be used with supplies of ±5 V to ±15 V, but lowest NTSC video distortion occurs for supplies of ±10 V or more using the AD818, where differential gain/differential phase errors are less than 0.01%/0.05°. With the AD818 operating at ±5 V supplies, the distortion rises somewhat, but the lowest power drain of 70 mW occurs. If low distortion and lowest power operation on ±5 V is important, the use of an AD8055 (or AD8056 section) should be considered for the U1 function; they will dissipate 50 mW. A drawback to this circuit is that it does load a 75 Ω video line to some extent, and so should be used with this loading taken into account. On the plus side, it has wide dynamic range for both signal and CM voltages, plus the inherent overvoltage protection.

Active Feedback Differential Line Receiver

The AD8129/AD8130 differential line receivers, along with their predecessor the AD830, utilize a novel amplifier topology called *active feedback* (see Reference 8). A simplified block diagram of these devices is shown in Figure 6-100.

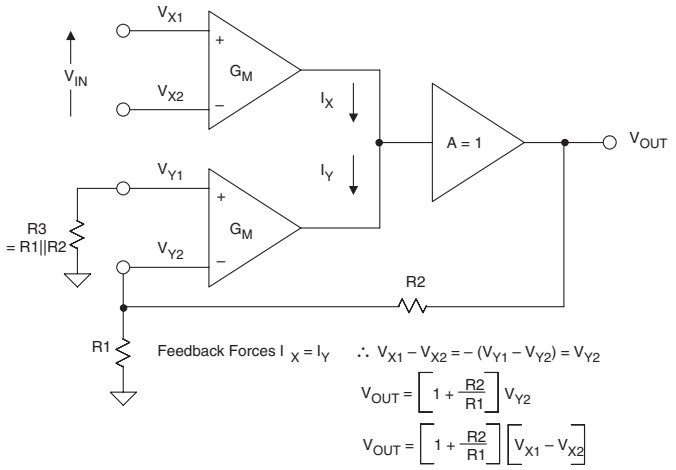


Figure 6-100: The AD830/AD8129/AD8130 active feedback amplifier topology

The AD830 and the AD8129/AD8130 have two sets of fully differential inputs, available at V_{X1}–V_{X2} and V_{Y1}–V_{Y2}, respectively. Internally, the outputs of the two GM stages are summed and drive a buffer output stage.

In this device the overall feedback loop forces the internal currents I_X and I_Y to be equal. This condition forces the differential voltages V_{X1}–V_{X2} and V_{Y1}–V_{Y2} to be equal and opposite in polarity. Feedback is taken from the output back to one input differential pair, while the other pair is driven directly by an input differential input signal.

An important point of this architecture is that high CM rejection is provided by the two differential input pairs, so *CMR is not dependent on resistor bridges* and their associated matching problems. The inherently wideband balanced circuit and the quasi-floating operation of the driven input provide the high CMR, which is typically 100 dB at dc.

The general expression for the stage's gain "G" is like a non-inverting op amp, or:

$$G = \frac{V_{OUT}}{V_{IN}} = 1 + \frac{R2}{R1} \qquad \text{Eq. 6-28}$$

As should be noted, this expression is identical to the gain of a noninverting op amp stage, with R2 and R1 in analogous positions.

The AD8129 is a low noise high gain (G = 10 or greater) version of this family, intended for applications with very long cables where signal attenuation is significant. The related AD8130 device is stable at a gain of one. It is used for those applications where lower gains are required, such as a gain-of-two, for driving source and load terminated cables.

The AD8129 and AD8130 have a wide power supply range, from single +5 V to ±12 V, allowing wide common-mode and differential-mode voltage ranges. The wide common-mode range enables the driver/receiver pair to operate without isolation transformers in many systems where the ground potential difference between driver and receiver locations is several volts. Both devices include a logic-controlled power-down function.

Both devices have high, balanced input impedances, and achieve 70 dB CMR @ 10MHz, providing excellent rejection of high frequency common-mode signals. Figure 6-101 shows AD8130 CMR for various supplies. As can be noted, it can be as high as 95 dB at 1 MHz, an impressive figure considering that no trimming is required.

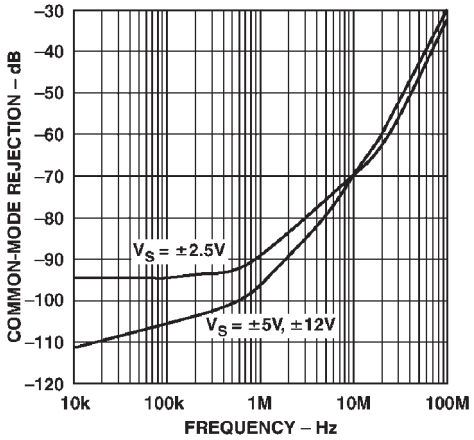


Figure 6-101: AD8130 common-mode rejection versus frequency for ±2.5 V, ±5 V, and ±12 V supplies

The typical 3 dB bandwidth for the AD8129 is 200 MHz, while the 0.1 dB bandwidth is 30 MHz in the SOIC package, and 50 MHz in the µSOIC package. The conditions for these specifications are for V_S = ±5 V and G = 10.

The typical 3 dB bandwidth for the AD8130 is 270 MHz, and the 0.1 dB bandwidth is 45 MHz, in either package. The conditions for these specifications are for V_S = ±5 V and G = 1. Typical differential gain and phase specifications for the AD8130 for G = 2, V_S = ±5 V, and R_L = 150 Ω are 0.13% and 0.15°, respectively.

A Cable-Tap or Loopthrough Amplifier

Figure 6-102 shows an example of a video *cable-tap* amplifier (or *loopthrough*) connection where the input signal is tapped from a coax line and applied to one input stage of the AD8130, with the output signal tied to the second input stage. The net gain is unity. Functionally, the input and local grounds are isolated by the CMR of the AD8130, which is typically 70 dB at 10 MHz. Note that in order to provide a dc path for the input bias currents of the upper stage, there must be a common path between the source and local grounds (shown as Z_{CM}). This impedance is not critical, but must be low enough that 60 Hz noise and other voltage components remain within the AD8130's CM range.

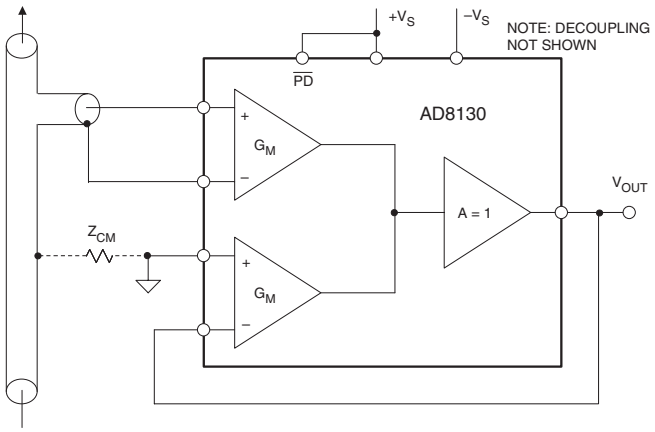


Figure 6-102: Video "cable-tap" amplifier using the AD8130

The circuit is efficient with the simplicity as shown, and requires no gain set resistors, and so forth to implement. Normal bypass capacitors and supply decoupling must of course be used, as in any high speed circuit. Other than the necessary dc path for the two inputs, it has little affect on the video cable it is monitoring, due to the high impedance AD8130 inputs. The circuit just as shown operates on supplies of ±5 V to ±12 V, but a ±15 V version can also be implemented by using the AD830 (without the AD8130's power-down function).

This circuit can also act as a video repeater, by connecting equal value feedforward and feedback resistors to implement a gain-of-two, for driving a source and load-terminated video cable (i.e., R2 and R1, as in Figure 6-100).

Further application examples of this family of active feedback amplifiers are contained in the "Amplifier Ideas" section of this chapter plus, of course the device data sheets.

High Speed Clamping Amplifiers

There are many situations where it is desirable to *clamp* the output of an op amp, to prevent overdriving following circuitry. Specially designed high speed, fast recovery clamping amplifiers offer an attractive alternative to designing external clamping/protection circuits. The AD8036/AD8037 low distortion, wide bandwidth clamp amplifiers represent a significant breakthrough in this technology. These devices allow the designer to specify a high (V_H) and low (V_L) clamp voltage. The output of the device clamps when the input exceeds either of these two levels. The AD8036/AD8037 offer superior clamping performance compared to competing devices that use output-clamping. Recovery time from overdrive is less than 5 ns, and small signal bandwidth is 240 MHz (AD8036) and 270 MHz (AD8037).

The key to the AD8036 and AD8037's fast, accurate clamp and amplifier performance is their proprietary input clamp architecture. This new design reduces clamp errors by more than 10 times over previous output clamp based circuits, as well as substantially increasing the bandwidth, precision, and versatility of the clamp inputs.

Figure 6-103 is an idealized block diagram of the AD8036 clamp amplifier, connected as a unity gain voltage follower. The primary signal path comprises A1 (a 1200 V/µs, 240 MHz high voltage gain, differential-to-single-ended amplifier) and A2 (a G = + 1 high current gain output buffer). The AD8037 differs from the AD8036 only in that A1 is optimized for closed-loop gains of two or greater.

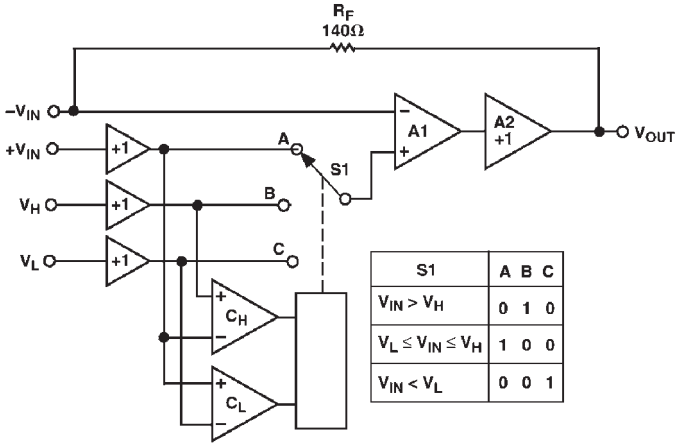


Figure 6-103: AD8036/AD8037 clamp amplifier equivalent circuit

The input clamp section is comprised of comparators C_H and C_L, which drive switch S1 through a decoder. The unity-gain buffers before the $+V_{IN}$, V_H, and V_L inputs isolate the input pins from the comparators and S1, without reducing bandwidth or precision. The two comparators have about the same bandwidth as A1 (240 MHz), so they can keep up with signals within the useful bandwidth of the AD8036. To illustrate the operation of the input clamp circuit, consider the case where V_H is referenced to 1 V, V_L is open, and the AD8036 is set for a gain of +1 by connecting its output back to its inverting input through the recommended 140 Ω feedback resistor. Note that the main signal path always operates closed loop, since the clamping circuit only affects A1's noninverting input.

If a 0 V to +2 V voltage ramp is applied to the AD8036's $+V_{IN}$ for the connection, V_{OUT} should track $+V_{IN}$ perfectly up to +1 V, then limit at exactly 1 V as $+V_{IN}$ continues to +2 V. In practice, the AD8036 comes close to this ideal behavior. As the $+V_{IN}$ input voltage ramps from zero to 1 V, the output of the high limit comparator C_H starts in the off state, as does the output of C_L. When $+V_{IN}$ just exceeds V_H (practically, by about 18 mV), C_H changes state, switching S1 from "A" to "B" reference level. Since the + input of A1 is now connected to V_H, further increases in $+V_{IN}$ have no effect on the AD8036's output. The AD8036 is now operating as a unity-gain buffer for the V_H input, as any variation in V_H, for $V_H > 1$ V, will be faithfully produced at V_{OUT}.

AD8036 operation for negative inputs and negative V_L clamp levels is similar, with comparator C_L controlling S1. Since the comparators see the voltage on the $+V_{IN}$ pin as their common reference level, the voltage

V_H and V_L are defined as "High" or "Low" with respect to $+V_{IN}$. For example, if V_{IN} is zero volts, V_H is open, and V_L is +1 V, comparator C_L will switch S1 to "C," and the AD8036 will buffer the V_L voltage and ignore $+V_{IN}$.

The AD8036/AD8037 performance closely matches the described ideal. The comparator's threshold extends from 60 mV inside the clamp window defined by the voltages on V_L and V_H to 60 mV beyond the window's edge. Switch S1 is implemented with current steering, so that A1's + input makes a continuous transition from, say, V_{IN} to V_H as the input voltage traverses the comparator's input threshold from 0.9 V to 1.0 V for V_H = 1.0 V.

The practical effect of the nonideal operation softens the transition from amplification to clamping modes, without compromising the absolute clamp limit set by the input clamping circuit. Figure 6-104 is a graph of V_{OUT} versus V_{IN} for the AD8036 and a typical *output* clamp amplifier. Both amplifiers are set for G = +1 and V_H = +1 V. The worst-case error between V_{OUT} (ideally clamped) and V_{OUT} (actual) is typically 18 mV times the amplifier closed-loop gain. This occurs when V_{IN} equals V_H (or V_L). As V_{IN} goes above and/or below this limit, V_{OUT} will stay within 5 mV of the ideal value.

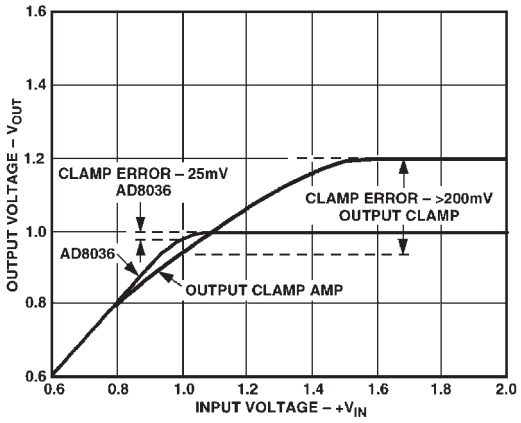


Figure 6-104: Comparison between input and output clamping

In contrast, the output clamp amplifier's transfer curve typically will show some compression starting at an input of 0.8 V, and can have an output voltage as far as 200 mV over the clamp limit. In addition, since the output clamp causes the amplifier to operate open-loop in the clamp mode, the amplifier's output impedance will increase, potentially causing additional errors, and the recovery time is significantly longer.

Flash Converter with Clamp Amp Input Protection

Figure 6-105 shows the AD9002 8-bit, 125 MSPS flash converter driven by the AD8037 (240 MHz bandwidth) clamping amplifier. The clamp voltages on the AD8037 are set to +0.55 V and –0.55 V, referenced to the ±0.5 V input signal, with the twin 806 Ω/100 Ω external resistive dividers. The AD8037 also supplies a gain of two, and an offset of –1 V (using the AD780 voltage reference), to match the 0 V to –2 V input range of the AD9002 flash converter. The output signal is clamped at +0.1 V and –2.1 V.

This multifunction clamping circuit therefore performs several important functions as well as preventing damage to the flash converter (which would otherwise occur should the input exceed 0.5 V, thereby forward

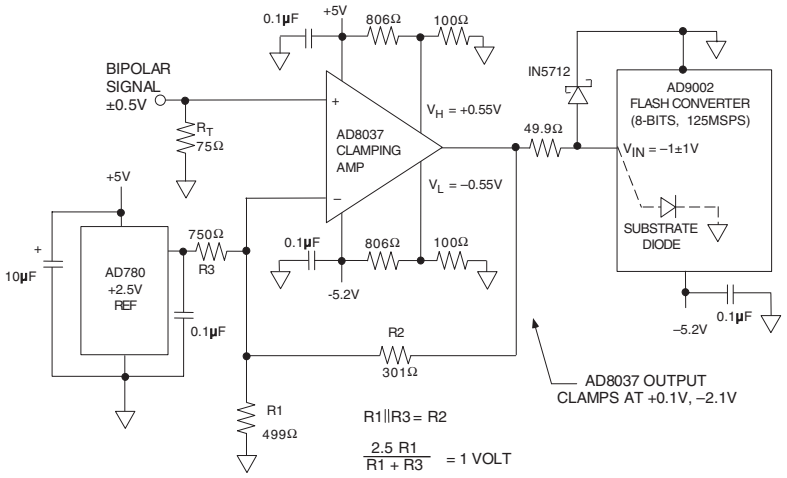


Figure 6-105: AD9002 8-bit, 125MSPS flash converter driven by AD8037 clamp amplifier

biasing the substrate diode). The 1N5712 Schottky diode is a safety-valve device, adding further protection for the flash converter during power-up.

Multiple criteria must be met in designing the feedback network around the AD8037. These are a specified gain and a fixed offset which will enable the output swing of the clamped amplifier to match the target input range of the converter.

The feedback resistor, R2 = 301 Ω, is selected for optimum bandwidth per the data sheet recommendation. For a gain of two, the parallel combination of R1 and R3 must also equal R2:

$$\frac{R1 \cdot R3}{R1 + R3} = R2 = 301\ \Omega \qquad \text{Eq. 6-29}$$

(nearest 1% standard resistor value).

In addition, the Thevenin equivalent output voltage from the AD780 +2.5 V reference and the R3/R1 divider must be +1 V, to provide the required –1 V offset at the output of the AD8037. This will cause the output swing of the AD8037 to be biased at –1 V when V_{IN} is zero, and to range from 0 to –2 V as V_{IN} ranges from –0.5 V to 0.5 V.

$$\frac{2.5 \cdot R1}{R1 + R3} = 1V \qquad \text{Eq. 6-30}$$

Solving these equations yields resistance values of R1 = 499 Ω, R3 = 750 Ω, using the nearest 1% standard values.

Other input and output voltages ranges can also be accommodated, by appropriate changes in the external resistors.

Further fast clamping op amp application examples are given in Reference 9, and the “Amplifier Ideas” section of this chapter (plus, of course, the device data sheets).

High Speed Video Multiplexing with Op Amps Utilizing Disable Function

A common video circuit function is the multiplexer, a stage which selects one of "n" video inputs and transmits a buffered version of the selected signal to the output. A number of video op amps (AD810, AD813, AD8013, AD8074/AD8075) have a *disable* mode which, when activated by applying the appropriate control level to a pin on the package, disables the op amp output stage and drops the power to a lower value.

In the case of the AD8013 (triple current-feedback op amp), asserting any one of the disable pins about 1.6 V from the negative supply will put the corresponding amplifier into a disabled, powered-down state. In this condition, the amplifier's quiescent current drops to about 0.3 mA, its output becomes a high impedance, and there is a high level of isolation from the input to the output. In the case of the gain-of-two line driver, for example, the impedance at the output node will be about equal to the sum of the feedback and feedforward resistors (1.6 kΩ) in parallel with about 12 pF capacitance. Input-to-output isolation is about 66 dB at 5 MHz.

Leaving the disable pin disconnected (floating) will leave the corresponding amplifier operational (i.e., enabled). The input impedance of the disable pin is about 40 kΩ in parallel with 5 pF. When driven to 0 V, with the negative supply at –5 V, about 100 µA flows into the disable pin.

When the disable pins are driven by CMOS logic, on a single +5 V supply, the disable and enable times are about 50 ns. When operated on dual supplies, level shifting will be required from standard logic outputs to the disable pins.

The AD8013's input stages include protection from the large differential voltages that may be applied when disabled. Internal clamps limit this voltage to about ±3 V. The high input-to-output isolation will be maintained for voltages below this limit.

Wiring the amplifier outputs together as shown in Figure 6-106 forms a 3:1 multiplexer with about 50 ns switching time between channels. The 0.1 dB bandwidth of the circuit is 35 MHz, and the OFF channel isolation is 60 dB at 10 MHz. The simple logic level-shifting circuit shown on the diagram does not significantly affect switching time.

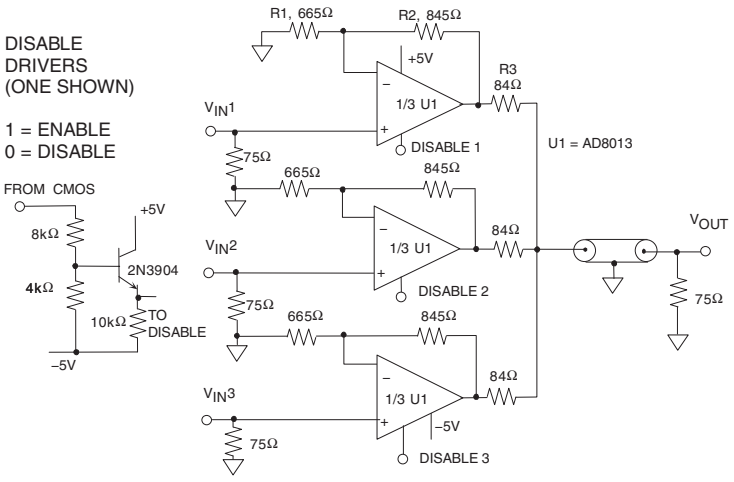


Figure 6-106: AD8013 3:1 video multiplexer switches in 50 ns

Setting up this amplifier is not entirely straightforward, and some explanation will help with subtleness. The feedback resistor R2 of 845 Ω was chosen first, to allow optimum bandwidth of the AD8013 current feedback op amp. The analogous resistors of the other channels use an identical value, for similar reasons.

Note that when any given channel is ON, it must drive both the termination resistor R_L, and the net dummy resistance, $R_X/2$, where R_X is an equivalent series resistance equal to R1 + R2 + R3. To provide a net overall gain of unity, as well as an effective source resistance of 75 Ω, the other resistor values must be as shown. In essence, the Thevenin equivalent value of $R_X/2$ and R3 should equal the desired source termination impedance of 75 Ω (which it does).

It is also desirable that the ON channels have a net gain of 2x, as seen behind the 75 Ω output impedance. The lower value of R1 vis-à-vis R2, along with the above relationship, allows these mutual criteria to be met.

Configuring two amplifiers of an AD8013 as unity gain followers with the third to set the gain results in a high performance 2:1 multiplexer, as shown in Figure 6-107.

This circuit takes advantage of the low crosstalk between the amplifiers, and achieves an OFF channel isolation of 50 dB at 10 MHz. The differential gain and phase performance of the circuit is 0.03% and 0.07°, respectively. The output stage operates at a gain of 2x, and can drive a 75 Ω source terminated line if desired.

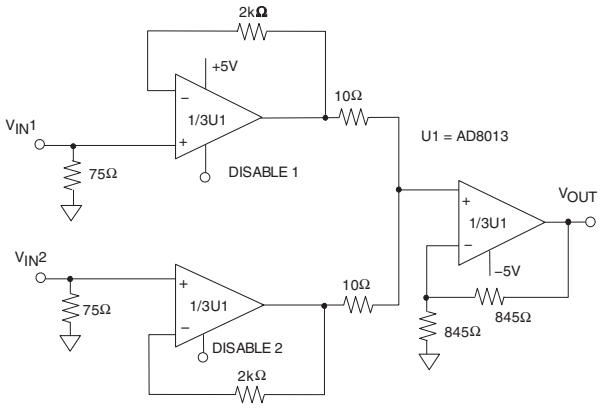


Figure 6-107: 2:1 video multiplexer based on the AD8013

Programmable Gain Amplifier using the AD813 Current Feedback Video Op Amp

Closely related to the multiplexers described above is a programmable gain video amplifier, or PGA, as shown in Figure 6-108. In the case of the AD813, the individual channels are disabled by pulling the disable pin about 2.5 V below the positive supply. This puts the corresponding amplifier in its powered down state. In this condition, the amplifier's quiescent supply current drops to about 0.5 mA, its output becomes a high impedance, and there is a high level of isolation between the input and the output.

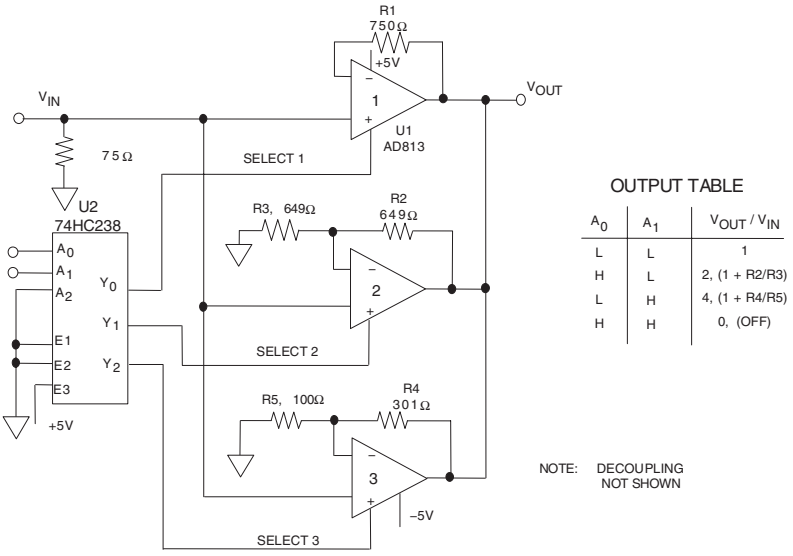


Figure 6-108: Programmable gain video amplifier using the AD813 triple current feedback amplifier

Leaving the disable pin disconnected (floating) will leave the amplifier operational, in the enabled state. When grounded, about 50 µA flows out of a disable pin when operating on ±5 V supplies. The switching threshold is such that the disable pins can be driven directly from +5 V CMOS logic as shown, with no level shifting (as in the previous example).

With a two-line digital control input, this circuit can be set up to provide three different gain settings. This makes it a useful circuit in various systems that can employ signal normalization or gain ranging prior to A/D conversion, such as CCD systems, ultrasound, and so forth. The gains can be binary-related as here, or they can be arbitrary. An extremely useful feature of the AD813 CFB current feedback amplifier is the fact that the bandwidth does not reduce as gain is increased. Instead, it stays relatively constant as gain is raised. Thus, more useful bandwidth is available at the higher programmed gains than would be true for a fixed gain-bandwidth product VFB amplifier type.

In the circuit, channel 1 of the AD813 is a unity gain channel, channel 2 has a gain of 2, and channel 3 a gain of 4, while the fourth control state is OFF. As is indicated by the table, these gains can easily be varied by adjustment of the R2/R3 or R4/R5 ratios. For the gain range and values shown, the PGA will be able to maintain a 3 dB bandwidth of about 50 MHz or more for loading as shown (a high impedance load of 1 kΩ or more is assumed). Fine tuning the bandwidth for a given gain setting can be accomplished by lowering the resistor values at the higher gains, as shown in the circuit, where for G = 1, R1 = 750 Ω, for G = 2, R2 = 649 Ω, and for G = 4, R4 = 301 Ω.

Integrated Video Multiplexers and Crosspoint Switches

Traditional CMOS switches and multiplexers suffer from several disadvantages at video frequencies. Their switching time (typically 100 ns or so) is not fast enough for today's applications, and they require external buffering in order to drive typical video loads. In addition, the small variation of the CMOS switch "on" resistance with signal level (R_{ON} *modulation*) introduces unwanted distortion in differential gain and phase. Multiplexers based on complementary bipolar technology offer a better solution at video frequencies.

Functional block diagrams of the AD8170/AD8174/AD8180/AD8182 bipolar video multiplexer are shown in Figure 6-109. The AD8183/AD8185 video multiplexer is shown in Figure 6-110. These devices offer a high degree of flexibility and are ideally suited to video applications, with excellent differential gain and phase specifications. Switching time for all devices in the family is 10 ns to 0.1%.

The AD8170/AD8174 series of muxes include an on-chip current feedback op amp output buffer whose gain can be set externally. Off channel isolation and crosstalk are typically greater than 80 dB for the entire family.

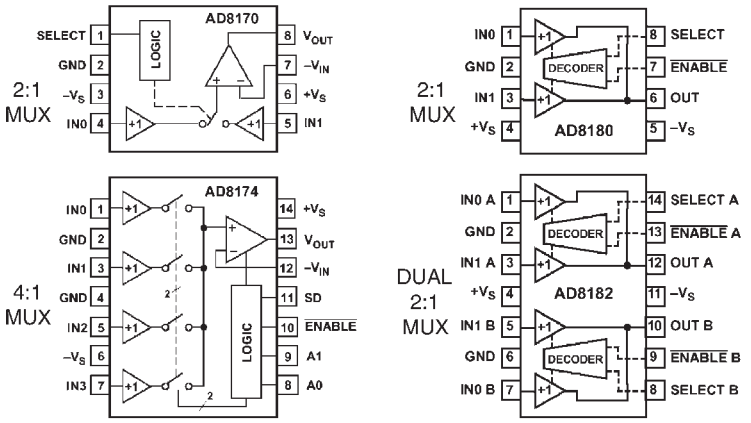


Figure 6-109: AD8170/AD8174/AD8180/AD8182 bipolar video multiplexers

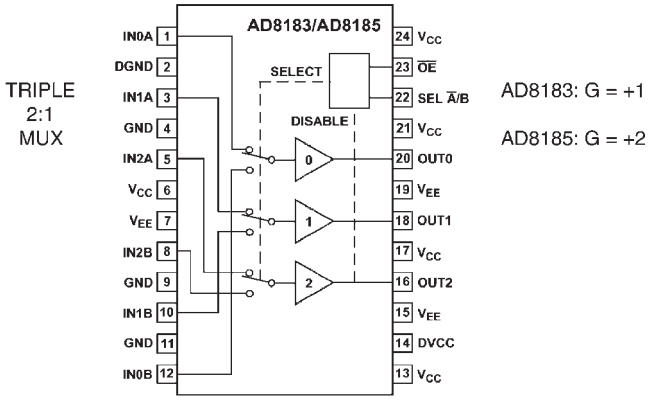


Figure 6-110: AD8183/AD8185 triple 2:1 video multiplexers

Dual RGB Source Video Multiplexer

Figure 6-111 shows an application circuit for three AD8170 2:1 muxes, where a single RGB monitor is switched between two RGB computer video sources.

In this setup, the overall effect is that of a three-pole, double-throw switch. The three video sources constitute the three poles, and either the upper or lower of the video sources constitute the two switch states.

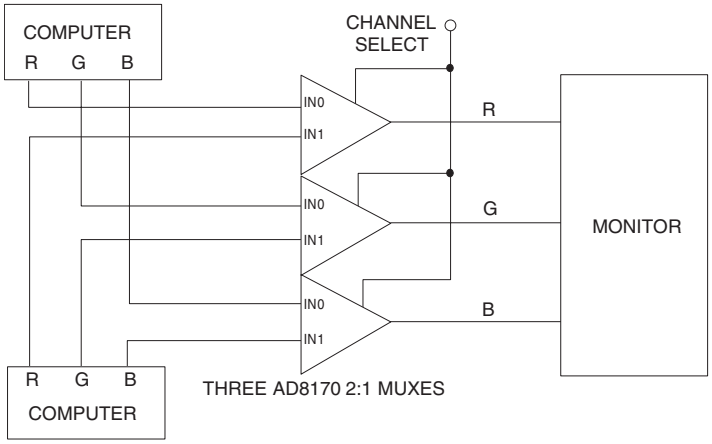


Figure 6-111: Dual source RGB multiplexer using three 2:1 muxes

Digitizing RGB Signals with One ADC

The AD8174 4:1 mux is used in Figure 6-112, to allow a single high speed ADC to digitize the RGB outputs of a scanner.

The RGB video signals from the scanner are fed in sequence to the ADC, and digitized in sequence, making efficient use of the scanner data with one ADC.

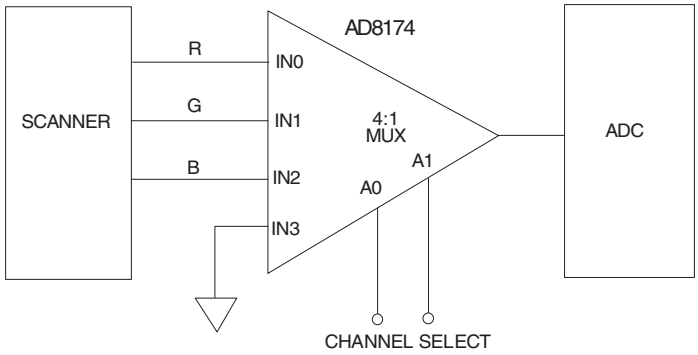


Figure 6-112: Digitizing RGB signals with one ADC and a 4:1 mux

Figure 6-113 shows two AD8174 4:1 muxes functionally expanded into an 8:1 multiplexer. The A0 and A1 inputs are conventional, with complemented Enable inputs.

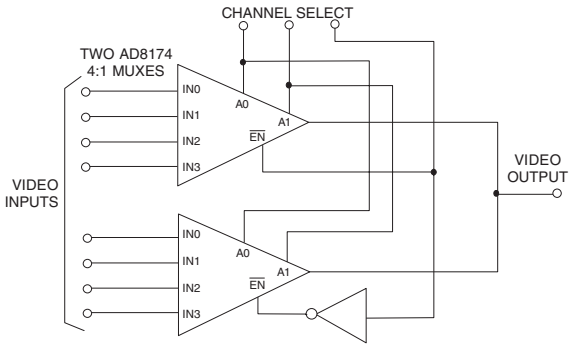


Figure 6-113: Expanding two 4:1 muxes into an 8:1 mux

The AD8116 extends the mux concepts to a fully integrated, 16×16 buffered video crosspoint switch matrix (Figure 6-114). The 3 dB bandwidth is greater than 200 MHz, and the 0.1 dB gain flatness extends to 60 MHz. Channel switching time is less than 30 ns to 0.1%. Channel-to-channel crosstalk is −70 dB measured at 5 MHz. Differential gain and phase is 0.01% and 0.01° for a 150 Ω load. Total power dissipation is 900 mW on ±5 V.

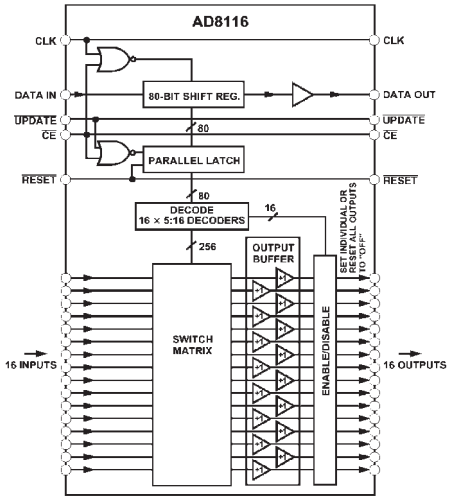


Figure 6-114: AD8116 16×16 200 MHz buffered video crosspoint switch

The AD8116 includes output buffers that can be put into a high impedance state for paralleling crosspoint stages so that the off channels do not load the output bus. The channel switching is performed via a serial digital control that can accommodate “daisy chaining” of several devices. The AD8116 package is a

128-pin 14 mm × 14 mm LQFP. Other members of the crosspoint switch family include the AD8110/AD8111 260 MHz 16 × 8 buffered crosspoint switch, the AD8113 audio/video 60 MHz 16 × 16 crosspoint switch, and the AD8114/AD8115 low cost 225 MHz 16 × 16 crosspoint switch.

Single Supply Video Applications

Optimum video performance in terms of differential gain and phase, bandwidth flatness, and so forth, is generally achieved using dual supplies of ±5 V or ±12 V. In many applications, however, stringent broadcast standards are not required, and single-supply operation may be desirable from a cost and power standpoint. This section illustrates a few op amp single-supply applications. All of the op amps are fully specified for both ±5 V and +5 V (and +3 V where the design supports it). Both rail-to-rail and nonrail-to-rail applications are shown (details of rail-to-rail op amp topologies are discussed in Chapter 1).

Single-Supply RGB Buffer

Op amps such as the AD8041/AD8042 and AD8044 can provide buffering of RGB signals that include ground, while operating from a single +3 V or +5 V supply. The signals that drive an RGB monitor are usually supplied by current output DACs that operate from a single +5 V supply. Examples are triple video DACs such as the ADV7120/ADV7121/ADV7122 from Analog Devices.

During the horizontal blanking interval, the current output of the DACs goes to zero, and the RGB signals are pulled to ground by the termination resistors. If more than one RGB monitor is desired, it cannot simply be connected in parallel because this would be a mis-termination. Therefore, buffering must be provided before connecting a second monitor.

RGB signals include ground as part of their dynamic output range. Previously a dual supply op amp had been required for this buffering, with sometimes this being the only component requiring a negative supply. This makes it quite inconvenient to incorporate a multiple monitor feature. Figure 6-115 shows a diagram of one channel of a single supply op amp gain-of-two buffer, for driving a second RGB monitor. No current is required when the amplifier output is at ground. The termination resistor at the monitor helps pull the output down at low voltage levels.

Note that the input and output are at ground during the horizontal blanking interval. The RGB signals are specified to output a maximum of 700 mV peak. The peak output of the AD8041 is 1.4 V, with the termination resistors providing a divide-by-two. All three channels (RGB) signals can be buffered in a like manner with duplication of this circuit. Another possibility is to use three sections of the (similar) quad AD8044 op amp.

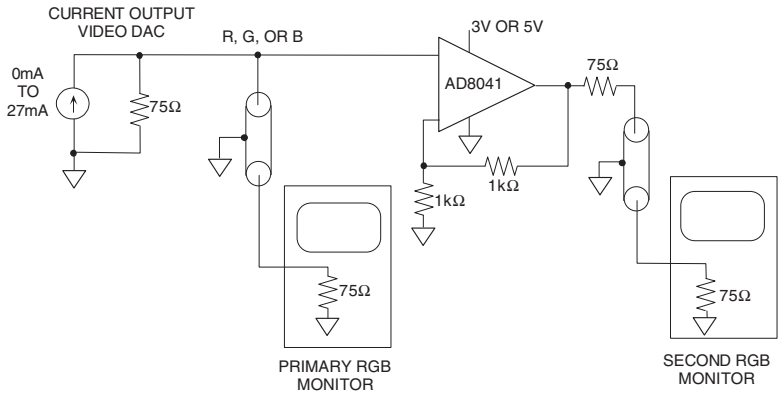


Figure 6-115: Single-supply RGB buffer operates on +3 V or +5 V

Single-Supply Sync Stripper

Some RGB monitors use only three cables total and carry the synchronizing signals and the Green (G) signal on the same cable (Green-with-sync). The sync signals are pulses that go in the negative direction from the blanking level of the G signal.

In some applications, for example prior to digitizing component video signals with ADCs, it is desirable to remove or strip the sync portion from the G signal. Figure 6-116 is a circuit using the AD8041 running on a single 5 V supply to perform this function. The signal at V_{IN} is the Green-with-sync signal from an ADV7120, a single supply triple video DAC.

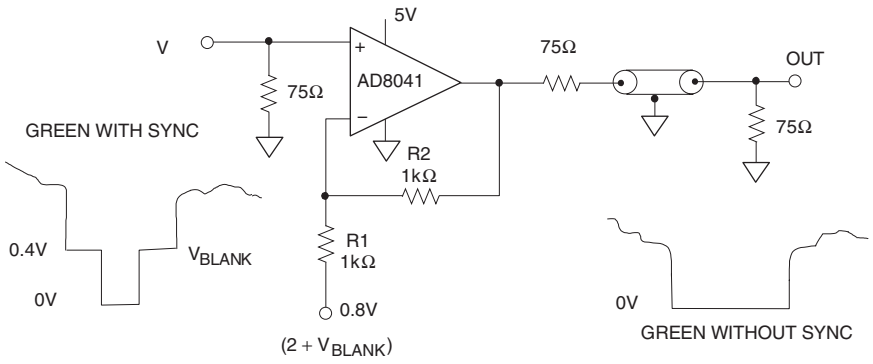


Figure 6-116: Single-supply video sync stripper

Because of the fact that the DAC used is single supply, the lowest level of the sync tip is at ground or slightly above. The AD8041 is set for a gain of two to compensate for the divide-by-two of the output terminations.

In this setup, the op amp used must have a CM capability that includes zero (as is true for the AD8041 family). For voltages *above* one-half the 0.8 V reference level applied to R1, the op amp operates as a linear amplifier, going positive from ground level at the output. For inputs *below* the reference level, the op amp saturates, with the output going to ground as used here. The result is that the negative sync tips are removed.

The reference voltage for R1 is twice the dc blanking level of the G signal; normally, this is $2 \times 0.4\ V = 0.8\ V$. Alternately, if the blanking level is at ground and the sync tip is negative (as in some dual supply systems), then R1 is tied to ground. The resulting VOUT will have the sync removed, and the blanking level at ground, as noted.

A Low Distortion, Single-Supply Video Line Driver with Zero-Volt Output

When operated with a single supply, the AD8031 80 MHz rail-to-rail voltage feedback op amp has optimum distortion performance when the signal has a common mode level of $V_S/2$, and when there is also about 500 mV of headroom to each rail. If this rule is violated, distortion performance suffers. But, if low distortion is required for signals close to ground, a level-shifting emitter follower can be used at the op amp output.

Figure 6-117 shows an AD8031 op amp, configured as a single supply gain-of-two line driver. With the output driving a back terminated 50 Ω line, the overall gain is unity from V_{IN} to V_{OUT}. In addition to minimizing reflections, the 50 Ω back termination resistor protects the transistor from damage if the cable is short circuited.

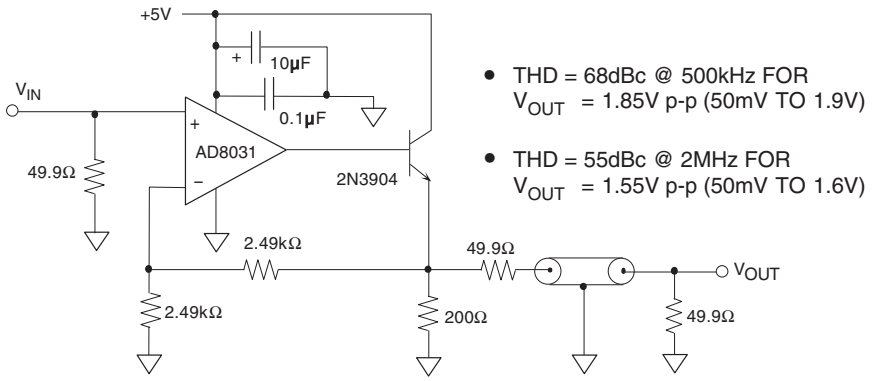


Figure 6-117: Low distortion zero-volt output single-supply line driver using the AD8031

The 2N3904 emitter follower inside the feedback loop ensures that the output voltage from the AD8031 always stays about 700 mV (or more) above ground, which minimizes distortion. Excellent distortion is obtained using this circuit, even when the output signal swings to within 50 mV of ground.

The circuit was tested at 500 kHz and 2 MHz using a single 5 V supply. For the 500 kHz signal, THD was 68 dBc with a peak-to-peak swing at a V_{OUT} of 1.85 V (50 mV to +1.9 V). This corresponds to a signal at the emitter follower output of 3.7 V p-p (100 mV to 3.8 V). Data was taken with an output signal of 2 MHz, and a THD of 55 dBc was measured with a V_{OUT} of 1.55 V p-p (50 mV to 1.6 V).

This circuit can also be used to drive the analog input of a single supply high speed ADC whose input voltage range is ground-referenced. In this case, the emitter of the external transistor is connected to the ADC input, and the termination resistor is deleted. In this case, peak positive voltage swings of approximately 3.8 V are possible before significant distortion begins to occur.

Headroom Considerations in ac-Coupled Single-Supply Video Circuits

The ac coupling of arbitrary waveforms can actually introduce problems that don't exist at all in dc-coupled or dc restored systems. These problems have to do with the waveform duty cycle, and are particularly acute with signals that approach the rails, as they can in ac-coupled, low supply voltage systems.

In Figure 6-118(A), an example of a 50% duty cycle square wave of about 2 V p-p level is shown, with the signal swing biased symmetrically between the upper and lower clip points of a 5 V supply amplifier.

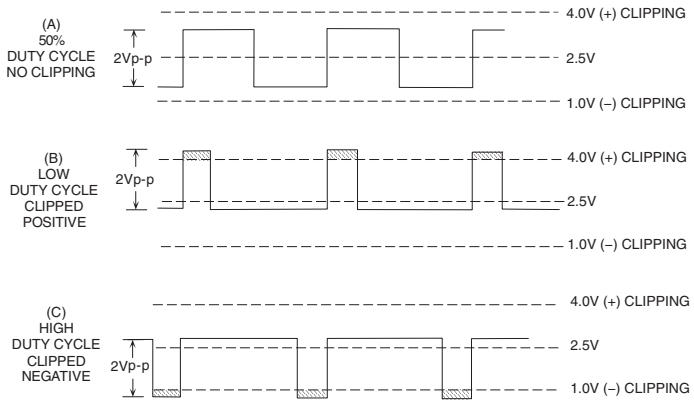


Figure 6-118: Waveform duty cycle taxes headroom in ac-coupled single-supply op amps

Assume that the amplifier has a complementary emitter follower output and can only swing to the limited dc levels as marked, about 1 V from either rail. In cases (B) and (C), the duty cycle of the input waveform is adjusted to both low and high duty cycle extremes *while maintaining the same peak-to-peak input level*. At the amplifier output, the waveform is seen to clip either negative or positive, in (B) and (C), respectively.

Since standard video waveforms *do* vary in duty cycle as the scene changes, the point is made that low distortion operation on ac-coupled single supply stages must take the duty cycle headroom degradation effect into account. If a stage has a 3 V p-p output swing available before clipping, and it must cleanly reproduce an *arbitrary* waveform, then the maximum allowable amplitude is less than one-half this 3 V p-p swing, that is <1.5 V p-p.

An example of violating this criteria are the 2 V p-p waveforms of Figure 6-118(B) and (C), which clip for both the low and high duty cycles. Note that the criteria set down above is based on avoiding hard clipping, while subtle distortion increases may in fact take place at lower levels. This suggests an even more conservative criterion for lowest distortion operation, such as in composite NTSC video amplifiers.

Single-Supply AC-Coupled Composite Video Line Driver

Figure 6-119 shows a single supply gain-of-two composite video line driver using the AD8041. Since the sync tips of a composite video signal extend below ground, the input must be ac-coupled and shifted positively to prevent clipping during negative excursions. The input is terminated in 75 Ω and ac-coupled via the 47 µF to a voltage divider that provides the dc bias point to the input. Setting the optimal common-mode bias voltage requires some understanding of the nature of composite video signals and the video performance of the AD8041.

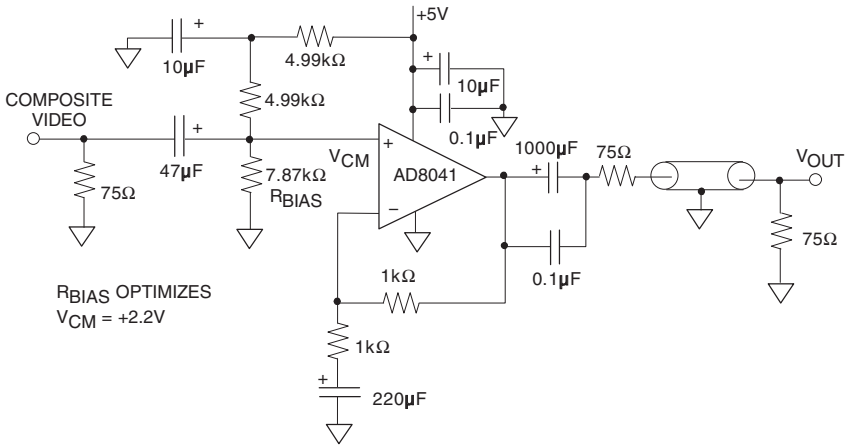


Figure 6-119: Single-supply ac-coupled composite video line driver has ΔG = 0.06% and Δϕ = 0.06°

As discussed above, signals of bounded peak-to-peak amplitude that vary in duty cycle require larger dynamic swing capability than their peak-to-peak amplitude after ac coupling. As a worst case, the dynamic signal swing required will approach twice the peak-to-peak value. The two bounding cases are for a duty cycle that is mostly low, but occasionally goes high at a fraction of a percent duty cycle, and vice versa.

Composite video is not quite this demanding. One bounding extreme is for a signal that is mostly black for an entire frame, but occasionally has a white (full intensity), minimum width spike at least once per frame.

The other extreme is for a video signal that is full white everywhere. The blanking intervals and sync tips of such a signal will have negative going excursions in compliance with composite video specifications. The combination of horizontal and vertical blanking intervals limit such a signal to being at its highest level (white) for about 75% of the time.

As a result of the duty cycle variations between the extremes presented above, a 1 V p-p composite video signal that is multiplied by a gain-of-two requires about 3.2 V p-p of dynamic voltage swing at the output for the op amp, to pass a composite video signal of arbitrary duty cycle without distortion.

The AD8041 device family not only has ample signal swing capability to handle the dynamic range required, but also has excellent differential gain and phase when buffering these signals in an ac-coupled configuration.

To test this, the differential gain and phase were measured for the AD8041 while the supplies were varied. As the lower supply is raised to approach the video signal, the first effect is that the sync tips become compressed before the differential gain and phase are adversely affected. Thus, there must be adequate swing in the negative direction to pass the sync tips without compression.

As the upper supply is lowered to approach the video, the differential gain and phase were not significantly adversely affected until the difference between the peak video output and the supply reached 0.6 V. Thus, the highest video level should be kept at least 0.6 V below the positive supply rail.

Taking the above into account, it was found that the optimal point to bias the noninverting input was at +2.2 V dc. Operating at this point, the worst case differential gain was 0.06% and the differential phase 0.06°.

The ac coupling capacitors used in the circuit may at first glance appear quite large. There is a reason for this. Note that a composite video signal has a lower frequency band edge of 30 Hz. The resistances at the various ac coupling points—especially at the output—are quite small. In order to minimize phase shifts and baseline tilt, the large value capacitors shown are required for best waveform reproduction.

For video system performance that is not to be of the highest quality, the value of these capacitors can be reduced by a factor of up to five with only a slight observable change in the picture quality.

Single-Supply AC-Coupled Single-Ended-to-Differential Driver

The circuit shown in Figure 6-120 provides a flexible solution to differential line driving in a single-supply application and utilizes the dual AD8042. The basic operation of the cross-coupled configuration has been described earlier in this section. The input, V_{IN}, is a single-ended signal that is capacitively coupled into the feedforward resistor, R1. The noninverting inputs of each half of the AD8042 are biased at 2.5 V.

The gain from single-ended input to the differential output is equal to 2R2/R1, as noted in the figure. If desired, this gain can be varied by simply changing one resistor (either R1 or R2). The input capacitor may need increase, for the processing of low frequency information with low phase shift.

It should also be noted that there is no output coupling capacitor, as none is required for differentially connected loads. The output terminals will be biased at approximately 2.5 V.

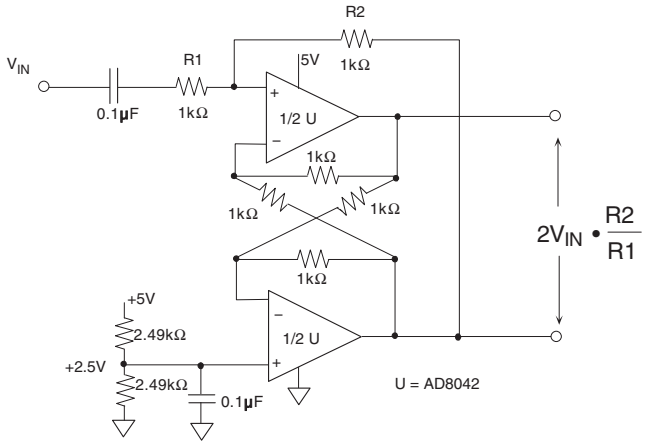


Figure 6-120: Single-supply ac-coupled differential driver

References: Video Amplifiers

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SECTION 6-4

Communication Amplifiers

Walt Kester

Components used in the signal path in communications systems must have wide dynamic range at high frequencies. Dynamic range is primarily limited by distortion and noise introduced by the active elements in amplifiers, mixers, and so forth. In the past, amplifiers for communications applications consisted primarily of "gain blocks" with appropriate specifications. Typically such amplifiers are specified for gain, bandwidth, distortion, and so forth, as a system is designed, and purchased as a self-contained package. This package itself is actually a communications amplifier subsystem.

Today, however, op amps with bandwidths of hundreds of megahertz, low noise, high dynamic range and flexible supply voltages also make popular building blocks in communications systems. They are easily configured for a given gain, and can deliver good performance.

Communications-Specific Specifications

As a necessity, this means that high frequency op amps must be fully specified not only in terms of traditional op amp ac specifications (bandwidth, slew rate, settling time), but also in terms of *communications-specific specifications*. These latter specifications would include performance for harmonic distortion, spurious free dynamic range (SFDR), intermodulation distortion, intercept points (IP2, IP3), noise, and noise figure (NF). Figure 6-121 illustrates these specifications.

- Noise
  - Noise referred to input (RTI)
  - Noise referred to output (RTO)
- Distortion
  - Second and third order intercept points (IP2, IP3)
  - Spurious free dynamic range (SFDR)
  - Harmonic distortion
    - Single-tone
    - Multi-tone
    - Out-of-band
  - Multitone Power Ratio (MTPR)
  - Noise Factor (NF), Noise Figure (NF)

Figure 6-121: Dynamic range specifications in communications systems

This portion of the chapter will examine these specifications, and how they apply to the amplifiers used in wireless and wired communications systems. In addition, several application specific amplifiers such as variable gain amplifiers (VGAs), CATV drivers, and xDSL drivers will also be discussed.

Distortion Specifications

When a spectrally pure sinewave passes through an amplifier (or other active device), various harmonic distortion products are produced, depending upon the nature and the severity of the nonlinearity. However, simply measuring harmonic distortion produced by single tone sinewaves of various frequencies does not give all the information required to evaluate the amplifier's potential performance in a communications application. In most communications systems there are a number of channels which are "stacked" in frequency. It is often required that an amplifier be rated in terms of the intermodulation distortion (IMD) produced with two or more specified tones applied.

Intermodulation distortion products are of special interest in the IF and RF area, and a major concern in the design of radio receivers. Rather than simply examining the harmonic distortion or total harmonic distortion (THD) produced by a single tone sinewave input, it is often useful to look at the distortion products produced by two tones.

As shown in Figure 6-122, two tones will produce second and third order intermodulation products. The example shows the second and third order products produced by applying two frequencies, f_1 and f_2, to a nonlinear device. The second order products located at f_2+f_1 and $f_2–f_1$ are located far away from the two tones, and may be removed by filtering. The third order products located at $2f_1+f_2$ and $2f_2+f_1$ may likewise be filtered. The third order products located at $2f_1–f_2$ and $2f_2–f_1$, however, are close to the original tones, and filtering them is difficult.

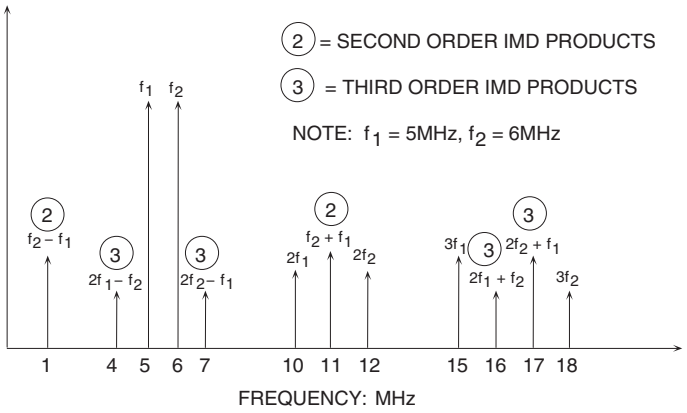


Figure 6-122: Second and third order intermodulation distortion products

Third order IMD products are especially troublesome in multichannel communications systems where the channel separation is constant across the frequency band. Third order IMD products can mask out small signals in the presence of larger ones.

Third order IMD is often specified in terms of the *third order intercept* point, as is shown by Figure 6-123. Two spectrally pure tones are applied to the system. The output signal power in a single tone (in dBm) as well as the relative amplitude of the third order products (referenced to a single tone) is plotted as a function of input signal power. The fundamental is shown by the *slope = 1* curve in the diagram. If the system nonlinearity is approximated by a power series expansion, it can be shown that second order IMD amplitudes increase 2 dB for every 1 dB of signal increase, as represented by *slope = 2* curve in the diagram.

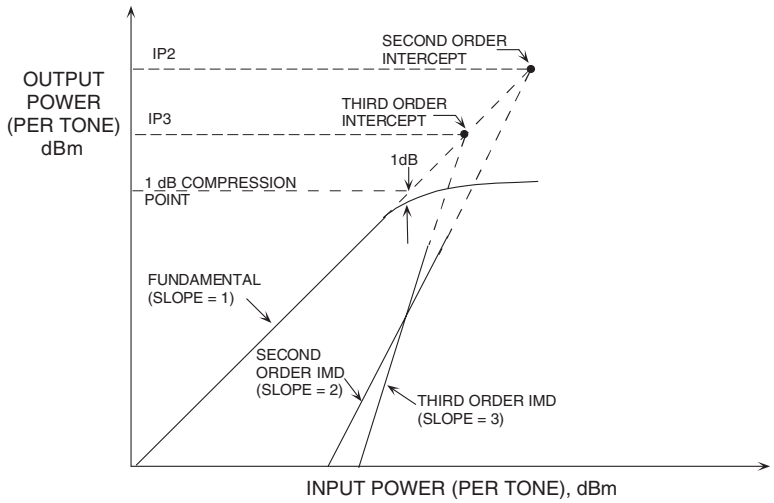


Figure 6-123: Intercept points and 1 dB compression point

Similarly, the third order IMD amplitudes increase 3 dB for every 1 dB of signal increase, as indicated by the *slope = 3* plotted line. With a low level two-tone input signal, and two data points, one can draw the second and third order IMD lines as they are shown in Figure 6-123 (using the principle that a point and a slope define a straight line).

Once the input reaches a certain level, however, the output signal begins to soft-limit, or compress. A parameter of interest here is the *1 dB compression point*. This is the point at which the output signal is compressed 1 dB from an ideal input/output transfer function. This is shown in Figure 6-123 within the region where the ideal slope = 1 line becomes dotted, and the actual response exhibits compression (solid).

Nevertheless, both the second and third order intercept lines may be extended, to intersect the (dotted) extension of the ideal output signal line. These intersections are called the *second* and *third order intercept points*, respectively, or IP2 and IP3. These power level values are usually referenced to the output power of the device delivered to a matched load (usually, but not necessarily 50 Ω) expressed in dBm.

It should be noted that IP2, IP3, and the 1 dB compression point are all a function of frequency, and as one would expect, the distortion is worse at higher frequencies.

For a given frequency, knowing the third order intercept point allows calculation of the approximate level of the third order IMD products as a function of output signal level. Figure 6-124 shows the third order intercept value as a function of frequency for a typical wideband low-distortion amplifier.

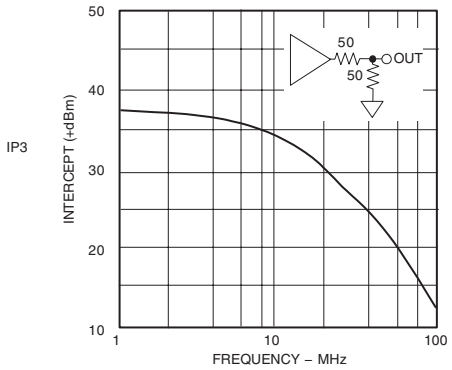


Figure 6-124: Third order intercept point (IP3) versus frequency for a low distortion amplifier

Assume the op amp output signal is 5 MHz and 2 V peak-to-peak into a 100 Ω load (50 Ω source and load termination). The voltage into the 50 Ω load is therefore 1 V peak-to-peak, corresponding to +4dBm. From Figure 6-124, the value of the third order intercept at 5 MHz is 36 dBm. The difference between +36 dBm and +4 dBm is 32 dB. This value is then multiplied by 2 to yield 64 dB (the value of the third-order intermodulation products referenced to the power in a single tone). Therefore, the intermodulation products should be –64 dBc (dB below carrier frequency), or at an output power level of –60 dBm.

Figure 6-125 shows the graphical analysis for this example. A similar analysis can be performed for the second-order intermodulation products, using data for IP2.

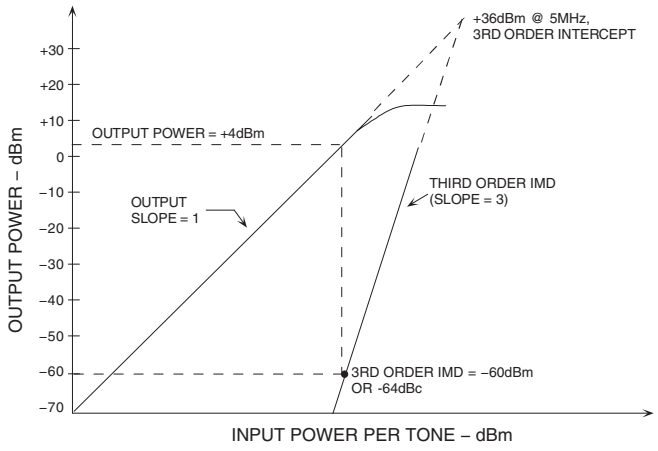


Figure 6-125: Using IP3 to calculate the third order IMD product amplitude

Another popular specification in communications systems is *spurious free dynamic range*, or SFDR. Figure 6-126 shows two variations of this specification. Single-tone SFDR (left) is the ratio of the signal (or carrier) to the *worst* spur in the bandwidth of interest. This spur may or may not be harmonically related to the signal. SFDR can be referenced to the signal or carrier level (dBc), or to full scale (dBFS).

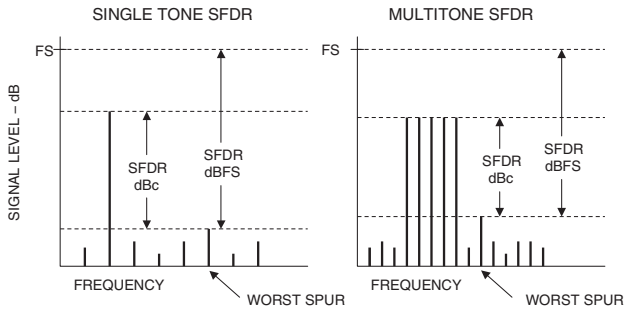


Figure 6-126: Spurious free dynamic range (SFDR) in communications systems

Because most amplifiers are soft limiters, the dBc unit is more often used. However, in systems that have a hard-limiter that precisely defines full scale (such as with ADCs), both dBc and dBFS may be used. It is important to understand that they both describe the worst spur amplitude. SFDR can also be specified for two tones or multitones (right), thereby simulating complex signals that contain multiple carriers and channels.

Multitone power ratio is another way of describing distortion in a multichannel communication system. Figure 6-127 shows the frequency partitioning in an xDSL system. The QAM signals in the upstream data path are represented by a number of equal amplitude tones, separated equally in frequency. One channel is completely eliminated from the input signal (shown as an empty bin), but intermodulation distortion caused by the system nonlinearity will cause a small signal to appear in that bin.

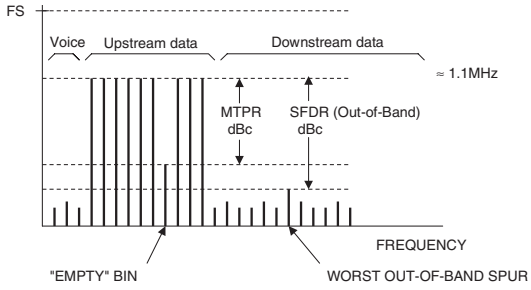


Figure 6-127: Multitone power ratio (MTPR) and out-of-band SFDR in xDSL applications

The ratio of the tone amplitude to the amplitude of the unwanted signal in the empty bin is defined as the multitone power ratio, or MTPR. It is equally important that the amplitude of the intermodulation products caused by the multitone signal (simulating multiple channels) not interfere with signals in either the voice band or the downstream data band. The amplitude of the worst spur produced in these bands to the amplitude of the multitone signal is therefore defined as the *out-of-band SFDR*.

Noise Specifications

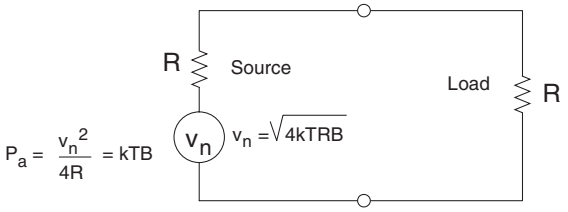
Op amp noise is generally specified in terms of input current and voltage noise, as previously discussed in Chapter 1 of this book. In communications systems, however, noise is often specified in terms of *noise figure* (NF)—see Figure 6-128. This can lead to confusion, especially when op amps are used as gain blocks and the noise figure of the op amp is not specified for the specific circuit conditions. In order to understand how to apply noise figure to op amps, we will first review the basic theory behind noise figure.

- NF is usually specified for matched input/output conditions, but this is not always a system requirement
- Noise Figure is a popular figure of merit in RF applications: LNAs, Mixers, etc.
- Difficulties arise when applying NF to op amps. NF is dependent on
  - Impedance levels
  - Feedback network
  - Closed loop gain
- Other difficulties arise due to different definitions of NF as found in various textbooks
- We will start with the basics and work up to the op amp issues

Figure 6-128: Noise figure in communications applications

The first concept is that of *available power* from a source. The available power of a source is the maximum power that can be drawn from the source. Figure 6-129 shows a resistor of value R as the noise source. The thermal noise of this source is $\sqrt{(4kTBR)}$. The maximum noise that can be transferred to an ideal noiseless load occurs when the load resistance is also equal to R.

The *available power*, P_a, of a source is the maximum power that can be drawn from the source. This occurs when the load resistance is equal to the source resistance.



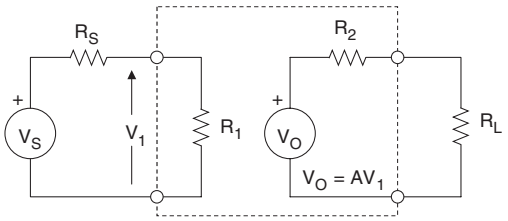
k = 1.38 × 10^{-23} Joules/K (Boltzman's Constant)
T = Temperature (assume 300K, room temperature)
B = Noise bandwidth (Hz)

$$P_{a\,(dBm)} = -174dBm + 10 \log B$$

Figure 6-129: Available noise power from a source

Under these conditions, the maximum available noise power from the source reduces to kTB, where k is Boltzmann's constant, T is the absolute temperature, and B is the noise bandwidth. Note that this power is independent of the value of the source resistance, R.

The next important concept is that of *available power gain* of a two-port network, as shown in Figure 6-130. The two-port network is driven from a signal source having an impedance. The equations show the available signal power from the source and the available signal power from the output of the network. The available power gain is simply the ratio of the available output power to the available power from the source.



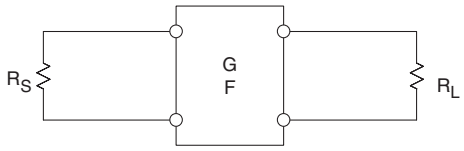
$$\text{Available signal power from source} = P_{as} = \frac{V_S^2}{4R_S}$$

$$\text{Available signal power at output} = P_{ao} = \frac{V_o^2}{4R_2}$$

$$\text{Available power gain} = G_a = \frac{P_{ao}}{P_{as}} = \frac{V_O^2 R_S}{V_S^2 R_2}$$

Figure 6-130: Available power gain of a two-port network

The gain and the noise of a two-port network can now be defined in terms of the available power gain, G, and the noise factor, F, as shown in Figure 6-131. The noise factor, F, is defined as the ratio of the total available output noise power to the available output noise power due to the source only. For a resistive source, the available noise power from the source is simply kTB, and the output noise power due to the source only is G · kTB.



G = Available Power Gain of Network

$$\text{F = Noise Factor} = \frac{\text{Total Available Output Noise Power}}{\text{Available Output Noise Power Due to Source Only}}$$

$$= \frac{\text{Total Available Output Noise Power}}{G \bullet kTB}$$

$$\text{NF = Noise Figure} = 10 \log_{10} F$$

Figure 6-131: Definition of noise factor and noise figure for a two-port noisy network.

Note that the noise factor, F, is expressed as a ratio, and the noise figure, NF, is simply the ratio F expressed in dB. An ideal noiseless two-port network therefore has noise factor F = 1, and a noise figure NF = 0 dB.

These same definitions can be used to calculate the NF of an op amp circuit; however, it is much easier to work in terms of the square of voltage noise spectral density and current noise spectral density, rather than

power or power spectral density (see Figure 6-132). Also, unmatched conditions are easier to deal with using this approach. *The noise factor F for an op amp is simply the ratio of the square of the total output noise spectral density to the square of the output noise spectral density due to the source only.* The noise figure NF = 10 • logF.

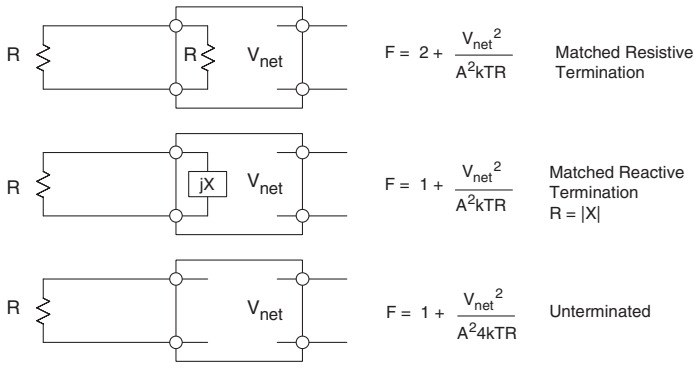
- With op amps, it is easier to work with voltage and current noise spectral density, rather than power or power spectral density.
- Unmatched conditions are more easily dealt with using voltage noise spectral density analysis.
- Voltage noise spectral densities add using root-sum-squares (RSS).
- A 1000Ωresistor has a voltage noise spectral density of 4nV/$\sqrt{\text{Hz}}$ @ 25°C (300K). (This is good to remember!)
- The basic definition of Noise Fact or and Noise Figure in terms of voltage noise spectral density becomes:

$$\text{Noise Factor} = F = \frac{(\text{Total Output Voltage Noise Spectral Density})^2}{(\text{Output Voltage Noise Spectral Density Due to Source Only})^2}$$

$$\text{Noise Figure} = NF = 10 \log_{10} F$$

Figure 6-132: Noise figure for op amps

In RF or IF gain blocks, the input impedance is defined. However, when using an op amp in the noninverting mode as a gain block, the input impedance is high (relative to transmission line impedances), and there are several options regarding the input termination which affect the noise figure. These options have been generalized to cover any two-port network with optional input terminations in Figure 6-133.



V_{net} = Voltage noise density of network excluding source and load terminations
A = Open circuit voltage gain of network

Figure 6-133: Noise factor for resistive, reactive, and unterminated conditions

Assume that the open-circuit voltage gain of the network is A and that the total output noise spectral density (excluding that due to the source resistance and the input termination) is equal to V_{net}.

The top diagram of Figure 6-133 shows the traditional matched case where the input is resistively terminated to match the source impedance. In this case, the input termination resistor not only attenuates the voltage noise of the source by a factor of 2, but also contributes noise due to its own thermal resistance.

The middle diagram of this figure shows the case of a reactive matched termination. Reactive terminations are often used where the bandwidth is limited but centered on a high frequency carrier. In this case, the source voltage noise is attenuated by a factor of 2, but the reactive termination adds no additional noise of its own to the total output noise.

The bottom diagram in Figure 6-133 shows the case of an unmatched, unterminated input. In this case, the voltage noise of the source is not attenuated, and there is obviously no additional noise due to the input termination because there is no input termination. Although this situation is not likely in a system using RF/IF gain blocks that generally require impedance matching at all interfaces, it is a possibility when using an op amp as the gain block, since the noninverting configuration input impedance is relatively high.

If we assume that the noise of the network, V_{net}, is very small relative to the source noise, then it is obvious that the input termination resistor adds 3 dB to the overall noise figure as well as reduces the overall voltage gain by a factor of 2. This is compared to the lowest noise case where there is no input termination. In fact, the lowest possible noise figure for a noiseless network with only an input resistive matched termination is 3 dB. Lower noise figures can only be obtained by using matched reactive terminations.

On the other hand, if the noise of the network, V_{net}, is very large with respect to the source noise, adding the resistive termination increases the overall noise figure by 6 dB compared to the unmatched unterminated case.

Summarizing, it is interesting to note that using large source resistances will decrease the noise figure but increase overall circuit noise. This illustrates the important fact that *noise figures can be compared only if they are specified at the same impedance level*. In Figure 6-134 these effects of amplifier input terminations on overall circuit noise and noise figure are summarized.

- For a low noise network, adding the matching input termination resistor makes the noise figure 3dB worse. The voltage gain is also reduced by a factor of 2.
- For a high noise network, adding the matching termination resistor makes the noise figure 6dB worse.
- Reactive matched terminations are often used at fixed IF/RF frequencies in LNAs, mixers, etc.
- Using large source and termination resistors decreases noise figure but increases overall circuit noise.
- Noise figures should only be compared at the same impedance level.

Figure 6-134: Effects of input termination on noise figure

Op amp noise has two components: low frequency noise whose spectral density is inversely proportional to the square root of the frequency, and white noise at medium and high frequencies. The low frequency noise is known as 1/f noise (the noise *power* obeys a 1/f law—the noise voltage or noise current is proportional to $1/\sqrt{f}$). The frequency at which the 1/f noise spectral density equals the white noise is known as the "1/f Corner Frequency." This is an important figure of merit for op amps, with low values indicating better performance. Values of the 1/f corner frequency vary from a few Hz for the most modern low noise low frequency amplifiers, to several hundreds, or even thousands of Hz for some high-speed op amps.

In most applications of high speed op amps, the total output RMS noise is generally of interest. Because of the high bandwidths, the chief contributor to the output RMS noise is the white noise, and that of the 1/f noise is negligible.

In order to better understand the effects of noise in high speed op amps, we use the classical noise model shown in Figure 6-135. This diagram identifies all possible white noise sources, including the external noise in the source and the feedback resistors.

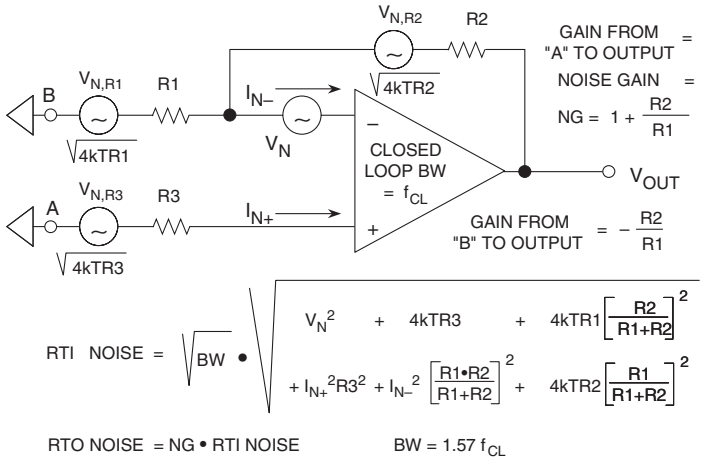


Figure 6-135: Calculating total op amp circuit noise

The equation in the figure allows for calculation of the total output RMS noise over the closed-loop bandwidth of the amplifier. This formula works quite well when the frequency response of the op amp is relatively flat. If there are more than a few dB of high frequency peaking, however, the actual noise will be greater than the predicted because the contribution over the last octave before the 3 dB cutoff frequency will dominate.

In most applications, the op amp feedback network is designed so that the bandwidth is relatively flat, and the formula provides a good estimate. Note that BW in the equation is the equivalent *noise bandwidth,* which, for a single-pole system, is obtained by multiplying the closed-loop 3 dB bandwidth by 1.57.

Figure 6-136 is a table that indicates how the individual noise contributors of Figure 6-135 are referred to the output. After calculating the individual noise spectral densities in this table, they can be squared, added, and then the square root of the sum of the squares yields the RSS value of the output noise spectral density, since all the sources are uncorrelated. This value is multiplied by the square root of the noise bandwidth (noise bandwidth = closed-loop 3 dB bandwidth multiplied by a correction factor of 1.57) to obtain the final value for the output RMS noise.

Typical high speed op amps have bandwidths greater than 150 MHz or so, and bipolar input stages have input voltage noises ranging from about 2 to $20\ nV/\sqrt{Hz}$. To put voltage noise in perspective, let's look at the Johnson noise spectral density of a resistor:

$$v_n = \sqrt{4kTR \times BW}$$

where *k* is Boltzmann's constant, *T* is the absolute temperature, *R* is the resistor value, and *BW* is the equivalent noise bandwidth of interest. (The equivalent noise bandwidth of a single-pole system is 1.57 times the 3 dB frequency). Using the formula, a 100 Ω resistor has a noise density of $1.3\ nV/\sqrt{Hz}$, and a 1000 Ω resistor about $4\ nV/\sqrt{Hz}$ (values are at room temperature: 27°C, or 300K).

NOISE SOURCE EXPRESSED AS A VOLTAGE	MULTIPLY BY THIS FACTOR TO REFER TO THE OP AMP OUTPUT
Johnson Noise in R3: $\sqrt{(4kTR3)}$	Noise Gain = 1 + R2/R1
Noninverting Input Current Noise Flowing in R3: $I_{n+}R3$	Noise Gain = 1 + R2/R1
Input Voltage Noise: V_n	Noise Gain = 1 + R2/R1
Johnson Noise in R1: $\sqrt{(4kTR1)}$	–R2/R1 (Gain from input of R1, "B," to Output)
Johnson Noise in R2: $\sqrt{(4kTR2)}$	1
Inverting Input Current Noise Flowing in R2: $I_{n-}R2$	1

Figure 6-136: Referring all noise sources to the output

The base-emitter in a bipolar transistor has an equivalent noise voltage source that is due to the "shot noise" of the collector current flowing in the transistor's (noiseless) incremental emitter resistance, r_e. The current noise is proportional to the square root of the collector current, Ic. The emitter resistance, on the other hand, is inversely proportional to the collector current, so *the shot-noise voltage is inversely proportional to the square root of the collector current*.

Voltage noise in FET input op amps tends to be larger than for bipolar ones, but current noise is extremely low (generally only a few tens of $\mathrm{fA}/\sqrt{\mathrm{Hz}}$) because of the low input bias currents. However, FET inputs are not generally required for op amp applications requiring bandwidths greater than 100 MHz.

Op amps also have input current noise on each input. For high speed FET input op amps, the gate currents are so low that input current noise is almost always negligible (measured in $\mathrm{fA}/\sqrt{\mathrm{Hz}}$).

For a voltage feedback (VFB) op amp, the inverting and noninverting input current noise are typically equal, and almost always uncorrelated. Typical values for wideband VFB op amps range from $0.5\ \mathrm{pA}/\sqrt{\mathrm{Hz}}$ to $5\ \mathrm{pA}/\sqrt{\mathrm{Hz}}$. The input current noise of a bipolar input stage is increased when input bias-current cancellation generators are added, because their current noise is not correlated, and therefore adds (in an RSS manner) to the intrinsic current noise of the bipolar stage.

The input voltage noise in current feedback (CFB) op amps tends to be lower than for VFB op amps having the same approximate bandwidth. This is because the input stage in a CFB op amp is usually operated at a higher current, thereby reducing the emitter resistance and hence the voltage noise. Typical values for CFB op amps range from about 1 to $5\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$.

The input current noise of CFB op amps tends to be larger than for VFB op amps because of the generally higher bias current levels. The inverting and noninverting current noise of a CFB is usually different because of the unique input architecture, and are specified separately. In most cases, the inverting input current noise is the larger of the two. Typical input current noise for CFB op amps ranges from 5 to $40\ \mathrm{pA}/\sqrt{\mathrm{Hz}}$.

The general principle of noise calculation is that uncorrelated noise sources add in a root-sum-squares manner, which means that if a noise source has a contribution to the output noise of a system which is less than

20% of the amplitude of the noise from other noise source in the system, then its contribution to the total system noise will be less than 2% of the total, and that noise source can almost invariably be ignored—in many cases, noise sources smaller than 33% of the largest can be ignored. This can simplify the calculations using the formula, assuming the correct decisions are made regarding the sources to be included and those to be neglected.

The sources which dominate the output noise are highly dependent on the closed-loop gain of the op amp. Notice that for high values of closed loop gain, the op amp voltage noise will tend be the chief contributor to the output noise. At low gains, the effects of the input current noise must also be considered, and may dominate, especially in the case of a CFB op amp.

Feedforward/feedback resistors in high speed op amp circuits may range from less than 100 Ω to more than 1 kΩ, so it is difficult to generalize about their contribution to the total output noise without knowing the specific values and the closed loop gain. The best way to make the calculations is to write a simple computer program that performs the calculations automatically and includes all noise sources (see Reference 1 for one example). In most high speed applications, the source impedance noise can be neglected for source impedances of 100 Ω or less.

Figure 6-137 shows an example calculation of total output noise for the AD8011 (300 MHz, 1 mA) CFB op amp. All six possible sources are included in the calculation. The appropriate multiplying factors which reflect the sources to the output are also shown on the diagram. For G = 2, the close-loop bandwidth of the AD8011 is 180 MHz. The correction factor of 1.57 in the final calculation converts this single-pole bandwidth into the circuit's equivalent noise bandwidth.

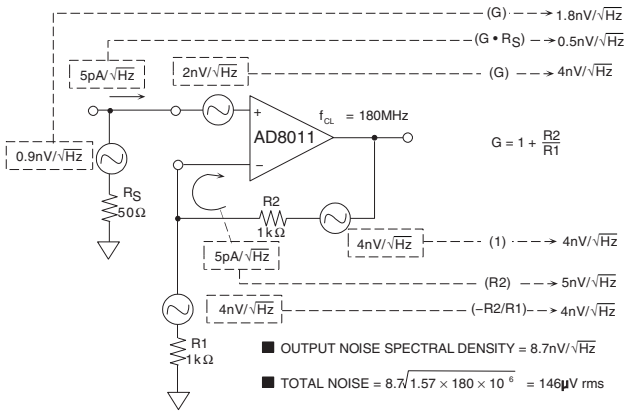


Figure 6-137: AD8011 output noise analysis

Now that the total output noise has been calculated, the issue of noise figure can be addressed. Figure 6-138 shows two cases for the AD8011 circuit: the top diagram corresponds to an unterminated input condition, and the bottom diagram corresponds to a terminated input condition.

For the unterminated case (top), the total output noise from the previous diagram (i.e., Figure 6-137) was $8.7\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$. Note this includes the noise of the 50 Ω source. The output noise due only to the source is simply the noise gain multiplied by the noise of the source, or $G\sqrt{(4kTR_S)} = 1.8\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$. The noise figure is simply NF = 20 log(8.7/1.8) = 13.7 dB. For the terminated case (bottom), the total output noise is still approximately $8.7\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$. Note that the input noise current (I_{n+}) now actually flows through 25 Ω

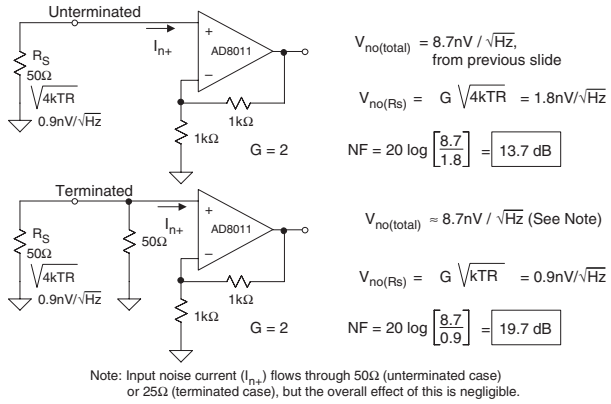


Figure 6-138: AD8011 noise figure for unterminated and terminated input conditions

rather than 50 Ω for the unterminated case, but the overall effect of this difference on the total output noise calculation is negligible.

The noise of the source, however, is now $\sqrt{(kTR)}$ due to the 50 Ω divider network, and reflected output, it becomes $G\sqrt{(kTR)} = 0.9\ nV/\sqrt{Hz}$. The noise figure is calculated as NF = 20 log(8.7/0.9) = 19.7 dB. Notice that the terminated case yields a noise figure that is approximately 6 dB worse than the unterminated case.

Finally, it should be noted that noise figure is actually a function of frequency. Figure 6-139 shows the noise figure of the AD8350 measured with a spot noise meter, as a function of frequency over the bandwidth 10 MHz to 1 GHz. The top curve is the noise figure, and the bottom curve is the closed-loop gain flatness.

In most cases, the approximations such as those used in the example of Figures 6-135 through 6-137 will give sufficient accuracy, provided the closed-loop bandwidth is relatively flat. However, using the actual spot noise figure may be desirable in high frequency narrowband applications involving specific carrier frequencies.

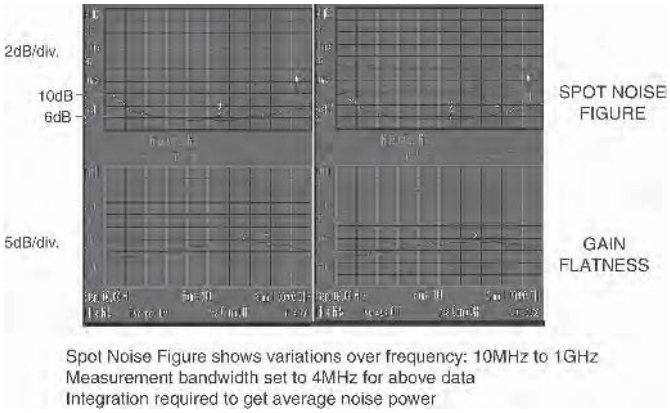


Figure 6-139: AD8350 spot noise figure and gain versus frequency from 10 MHz to 1 GHz

Variable Gain Amplifiers (VGAs) in Automatic Gain Control (AGC)

Wideband, low distortion variable gain amplifiers find wide applications in communications systems. One example is automatic gain control (AGC) in radio receivers. Typically, the received energy exhibits a large dynamic range due to the variability of the propagation path, requiring dynamic range compression in the receiver. In this case, the wanted information is in the modulation envelope (whatever the modulation mode), not in the absolute magnitude of the carrier. For example, a 1 MHz carrier modulated at 1 kHz to a 30% modulation depth would convey the same information, whether the received carrier level is at 0 dBm or –120 dBm. Some type of automatic gain control (AGC) in the receiver is generally utilized to restore the carrier amplitude to some normalized reference level, in the presence of large input fluctuations. AGC circuits are dynamic-range compressors which respond to some signal metric (often mean amplitude) acquired over an interval corresponding to many periods of the carrier.

Consequently, they require time to adjust to variations in received signal level. The time required to respond to a sudden increase in signal level can be reduced by using peak detection methods, but with some loss of robustness, since transient noise peaks can now activate the AGC detection circuits. Nonlinear filtering and the concept of "delayed AGC" can be useful in optimizing an AGC system. Many trade-offs are found in practice; Figure 6-140 shows a basic AGC system.

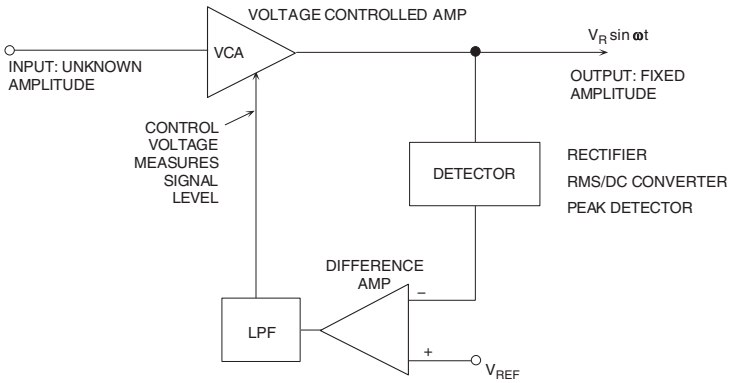


Figure 6-140: A typical automatic gain control (AGC) system

It is interesting to note that an AGC loop actually has *two* outputs. The more obvious output is of course the amplitude-stabilized signal. The less obvious output is the control voltage to the VCA. In reality, this voltage is a measure of the average amplitude of the input signal. If the system is precisely scaled, the control voltage may be used as a measure of the input signal, which is sometimes also known as a *received signal strength indicator* (RSSI).

This latter point, given a suitably precise VCA gain control law, allows implementation of a receiving system that is calibrated for incoming signal level.

Voltage Controlled Amplifiers (VCAs)

An analog multiplier can be used as a variable-gain amplifier, as shown in Figure 6-141 below. The control voltage is applied to one input, and the signal to the other. In this configuration, the gain is directly proportional to the control voltage.

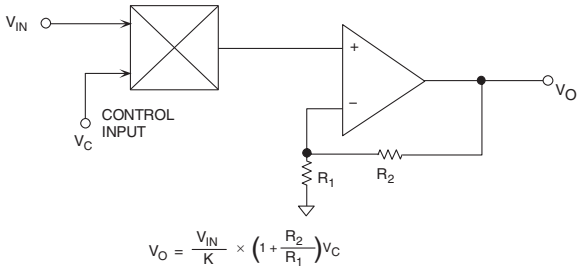


Figure 6-141: Using a multiplier as a voltage-controlled amplifier (VCA)

Most VCAs made with analog multipliers have gain that is *linear in volts* with respect to the control voltage, and they tend to be noisy. There is a demand, however, for a VCA that combines a wide gain range with constant bandwidth and phase, low noise with large signal-handling capabilities, and low distortion with low power consumption, while providing accurate, stable, *linear-in-dB* gain. The AD600, AD602, AD603, AD604, AD605, and AD8367 achieve these demanding and conflicting objectives with a unique and elegant solution—the X-AMP® (for *exponential amplifier* see Reference 2).

The concept is simple: a fixed-gain amplifier follows a passive, broadband attenuator, with special means to alter voltage-controlled attenuation, as in Figure 6-142.

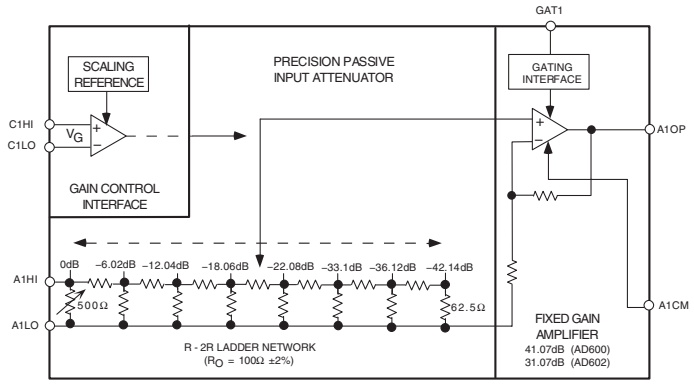


Figure 6-142: Single channel of the dual 30 MHz AD600/AD602 X-AMP

The AD600/AD602 amplifier stage is optimized for low input noise, and negative feedback is used to accurately define its moderately high gain (30 dB–40 dB) and minimize distortion. Since amplifier gain is fixed, so also are its ac and transient response characteristics, including distortion and group delay. As its gain is high, the input is never driven beyond a few millivolts, always operating within a small signal response range.

The attenuator network is a 7-section (8-tap) R-2R ladder. The ratio between adjacent taps is exactly 2, or 6.02 dB, providing the basis for precise linear-in-dB behavior, while overall attenuation is 42.14 dB. As will be shown, the amplifier's input can be connected to any one of these taps, or even *interpolated* between them, with only a small deviation error of about ±0.2 dB. Overall gain can be varied from the fixed (maximum) gain, to a value 42.14 dB less. In the AD600, the fixed gain is 41.07 dB (voltage gain of 113); using this choice, the full gain range is –1.07 dB to +41.07 dB. The gain is related to control voltage by the relationship $G_{dB} = 32\ V_G + 20$ where V_G is in volts. For the AD602, the fixed gain is 31.07 dB (voltage gain of 35.8), and the gain is given by $G_{dB} = 32\ V_G + 10$.

The gain at $V_G = 0$ is laser trimmed to an absolute accuracy of ±0.2 dB. The gain scaling is determined by an on-chip bandgap reference (shared by both channels), laser trimmed for high accuracy and low temperature coefficient. Figure 6-143 shows the gain versus the differential control voltage for both the AD600 and the AD602. Deviation from an ideal control law is only a fraction of a dB over a large part of the dynamic range.

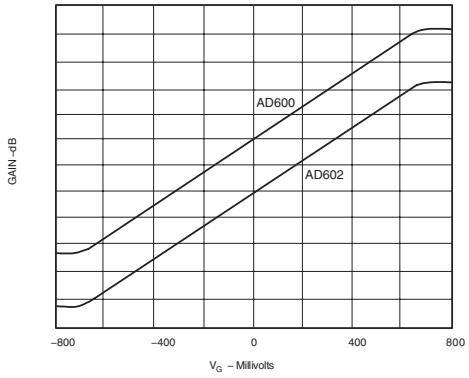


Figure 6-143: Gain of the AD600/AD602 as a function of control voltage

In order to understand the operation of the X-AMP, consider the simplified diagram shown in Figure 6-144. Note that each of the eight taps is connected to an input of one of eight bipolar differential pairs, used as current-controlled transconductance (g_m) stages; the other input of all these g_m stages is connected to the amplifier's gain-determining feedback network, R_{F1}/R_{F2}. When emitter bias current I_E is directed to one of the eight transistor pairs (not shown here), it becomes the complete amplifier input stage.

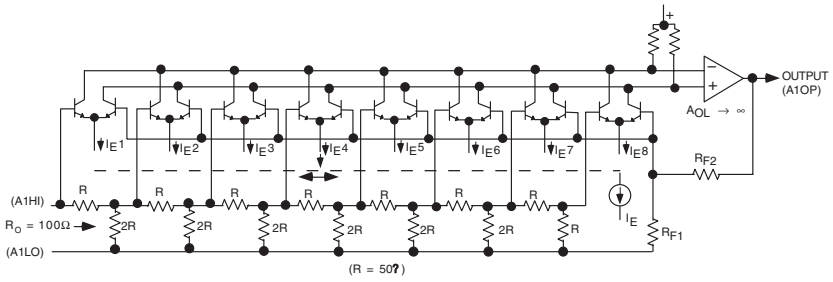


Figure 6-144: Continuous interpolation between taps using current-controlled g_m stages in the X-AMP

When I_E is connected to the left-most pair, the signal input is connected directly to the amplifier, giving maximum gain. The distortion is very low, even at high frequencies, due to the careful open-loop design, aided by the negative feedback. If I_E were to be abruptly switched to the second pair, the overall gain would drop by exactly 6.02 dB, and the distortion would remain low, because only one g_m stage remains active.

In reality, the bias current is *gradually* transferred from the first pair to the second. When I_E is equally divided between two g_m stages, both are active, and the situation arises where we have an op amp with two input stages fighting for control of the loop, one getting the full signal, and the other getting a signal exactly half as large.

Analysis shows that the effective gain is reduced, not by 3 dB, as one might first expect, but rather by 20 log1.5, or 3.52 dB. This error, when divided equally over the whole range, would amount to a gain ripple of ±0.25 dB; however, the interpolation circuit actually generates a Gaussian distribution of bias currents, and a significant fraction of I_E always flows in adjacent stages. This smoothes the gain function and actually lowers the ripple. As I_E moves further to the right, the overall gain progressively drops.

The key features of the X-AMP product family are summarized in Figure 6-145. Note the other members of the family beyond the described AD600/AD602.

	BANDWIDTH	DISTORTION	NOISE	INPUT Z	SUPPLY
AD600/602	35MHz	–60dBc @ 10MHz	1.4nV/√Hz	100Ω	±5V
AD603	90MHz	–60dBc @ 10MHz	1.3nV/√Hz	100Ω	±5V
AD604	40MHz	–43dBc @ 10MHz	0.8nV/√Hz	300kΩ	±5V
AD605	40MHz	–51dBc @ 10MHz	1.8nV/√Hz	200Ω	+5V
AD8367	500MHz	IP3 = +31.5dBm @140MHz	NF = 7.8dB @140MHz	200Ω	+2.7 to +5V

Figure 6-145: X-AMP family key specifications

The total input-referred noise of the AD600/AD602 X-AMP is ($1.4\ nV/\sqrt{Hz}$ at 25°C); only slightly more than the thermal noise of a 100 Ω resistor ($1.29\ nV/\sqrt{Hz}$ at 25°C). The input-referred noise is constant regardless of the attenuator setting, therefore the output noise is always constant and independent of gain.

For the AD600, the amplifier gain is 113 and the output noise spectral density is therefore $1.4\ nV/\sqrt{Hz} \times 113$, or $158\ nV/\sqrt{Hz}$. Referred to its maximum output of 2 V rms, the signal-to-noise ratio would be 82 dB in a 1 MHz bandwidth. The corresponding signal-to-noise ratio of the AD602 is 10 dB greater, or 92 dB.

Digitally Controlled Variable Gain Amplifiers for CATV Upstream Data Line Drivers

Cable modems offer much higher data rates than standard dial-up connections and have become very popular. In addition to receiving data (*downstream*), the cable modem also transmits data (*upstream*). This requires a low distortion digitally controlled variable gain amplifier capable of driving the 75 Ω coaxial cable at a nominal level of 1 V rms (+11.2 dBm, or 60 dBmV). The AD8323 is a member of a family of CATV upstream line drivers suitable for this application. The AD8323 gain is controlled by an 8-bit serial word that determines the desired gain over a 53.5 dB range, resulting in gain changes of 0.7526 dB/LSB. The AD8323 block diagram is shown Figure 6-146.

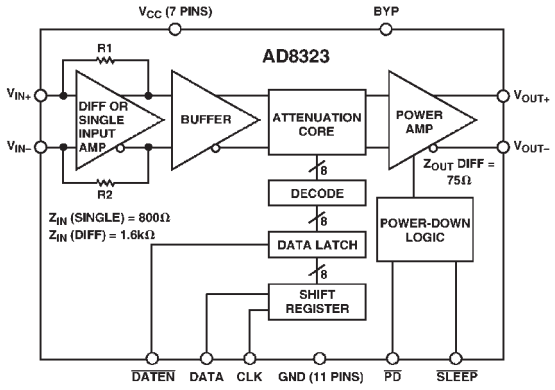


Figure 6-146: AD8323 CATV digitally controlled variable gain amplifier

The AD8323 has a variable attenuator core where the attenuation is digitally controlled from 0 dB to –53.5 dB. The input buffer has a gain of approximately + 27.5 dB; therefore, the resulting overall gain range is from –26 dB to +27.5 dB. The AD8323 is composed of four analog functions in the power-up mode. The input amplifier (preamp) can be used either single-ended or differentially. The preamp stage drives a vernier stage that provides the fine tune gain adjustment. The 0.7526 dB/LSB resolution is implemented in this stage and provides a total of approximately 5.25 dB of attenuation. After the vernier stage, a DAC provides the bulk of the AD8323's attenuation (8 bits, or 48 dB).

The signals in the preamp and vernier gain blocks are differential to improve the PSRR and linearity. A differential current is fed from the DAC to the output stage, which amplifies these currents to the appropriate levels necessary to drive the 75 Ω load.

A key performance and cost advantage of the AD8323 results from the ability to maintain a constant dynamic output impedance of 75 Ω during power-up/power-down conditions. The output stage uses negative feedback to implement a differential 75 Ω dynamic output impedance. This eliminates the need for an external 75 Ω termination, resulting in twice the effective output voltage when compared to a standard op amp.

These features allow the AD8323 to operate on a single 5 V supply and still deliver the required output power. Distortion performance of –56 dBc is achieved with an output level up to 1 V rms (+11.2 dBm, or 60 dBmV) at a 21 MHz bandwidth.

The key specifications for the AD8323 are shown in Figure 6-147.

- Supports cable modem DOCSIS (Data Over Cable Service) standard for upstream path transmission
- Gain/attenuation programmable in 0.7526dB steps over a 53.5dB range:
  –26dB to +27.5dB
- 3-wire SPI digital interface
- Bandwidth: > 100MHz (all gains)
- Low distortion @ 1V RMS (+11.2dBm, +60dBmV) output into 75Ω
  – –56dBc SFDR @ 21MHz
  – –55dBc SFDR @ 42MHz
- Single 5V supply (133mA)
- Power-down mode (35mA), sleep mode (4mA)
- 75Ω dynamic output impedance in power-up or power-down modes

Figure 6-147: AD8323 CATV line driver key specifications

xDSL Upstream Data Line Drivers

Various versions of DSL are now used to provide fast internet connections. The upstream data path requires the transmission of +13 dBm discrete multitone (DMT) signals occupying a bandwidth between approximately 144 kHz and 500 kHz. The DMT signal can have a crest factor as high as 5.3, requiring the line driver to provide peak power of +27.5 dBm, which translates into 7.5 V peak voltage on the 100 Ω telephone line.

DMT modulation appears in the frequency domain as power contained in several individual frequency subbands, sometimes referred to as tones or bins, each of which is uniformly separated in frequency. A quadrature amplitude modulated (QAM) signal occurs at the center of each subband or tone. Difficulties will exist when decoding these subbands if a signal from one subband is corrupted by the signal from other subbands, regardless of whether the corruption comes from an adjacent subband or harmonics of other subbands.

Conventional methods of expressing the output signal integrity of line drivers, such as single-tone harmonic distortion or THD, two-tone intermodulation distortion (IMD), and third order intercept (IP3), become significantly less meaningful when amplifiers are required to process DMT and other heavily modulated waveforms.

A typical ADSL upstream DMT signal can contain as many as 27 carriers (subbands or tones) of QAM signals (as shown in Figure 6-148). Multitone power ratio (MTTR) is the relative difference between the measured power in a typical subband (at one tone or carrier) versus the power at another subband specifically

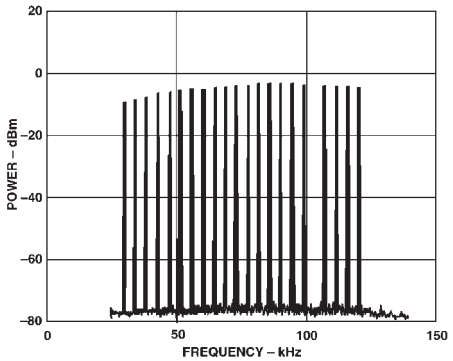


Figure 6-148: Discrete multitone (DMT) signal in the frequency domain

selected to contain no QAM data. In other words, a selected subband (or tone) remains open and void of intentional power (without a QAM signal), yielding an empty frequency bin. MTPR, sometimes referred to as the "empty bin test," is typically expressed in dBc and is a key specification for all types of DSL systems.

Another important specification for an xDSL line driver is *out-of-band* SFDR. Spurs produced by distortion of the DMT upstream data can fall in the downstream frequency regions and distort voiceband and downstream data.

Figure 6-149 shows an xDSL line driver application circuit based on the AD8018 line driver (one member of a family of Analog Devices' DSL line drivers). The peak DMT signal can be 7.5 V on the 100 Ω telephone line.

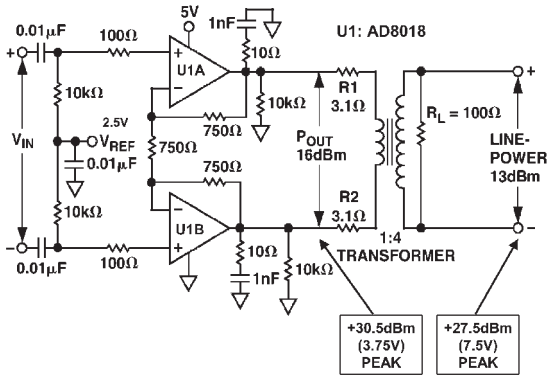


Figure 6-149: AD8018 xDSL upstream data line driver application

Assuming maximum low distortion output swing available from the AD8018 line driver on a single 5 V supply is 4 V, taking into account the power lost due to the two 3.1 Ω back-termination resistors, a transformer with a 1:4 or greater step-up is needed.

The AD8018 is therefore coupled to the phone line through a step-up transformer with a 1:4 turns ratio. R1 and R2 are back-termination or line-matching resistors, each 3.1 Ω. The total differential load presented to the AD8018 output is 12.5 Ω, including the termination resistors. Even under these conditions, the AD8018 provides low distortion signals to within 0.5 V or the power rails.

The transformer circuit presents a complex impedance to the AD8018 output, and therefore for stability, a series R-C network should be connected between each amplifier's output and ground. The recommended values are 10 Ω for the resistor and 1 nF for the capacitor to create a low impedance path to ground at frequencies above 16 MHz. The 10 kΩ output resistors connected to ground are added to improve common-mode stability.

For the AD8018 circuit of Figure 6-149, the out-of-band SFDR versus upstream line power is shown in Figure 6-150 for various supply voltages.

Some key AD8018 features and specifications are summarized in Figure 6-151.

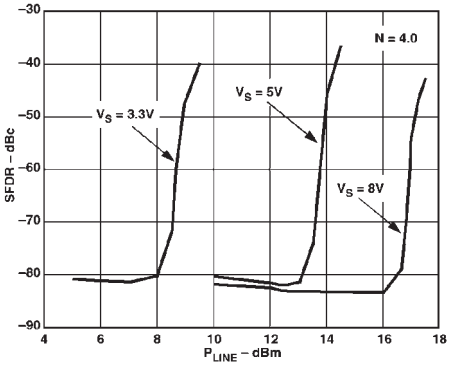


Figure 6-150: Out-of-band SFDR versus upstream line power, 144 kHz to 500 kHz

- Dual current feedback amplifiers
- Bandwidth: 130MHz (–3dB)
- Slew rate: 300V/µs
- Rail-to-rail output stage (swings within 0.5V of rails for R_L = 5Ω)
  - +16dBm into 12.5Ωload
  - +30.5dBm peak power (3.75V) with +5V supply
- MTPR: –70dBc (25kHz to 138kHz)
- Maintains –82dBc out-of-band SFDR, 144kHz to 500kHz, for output power = +16dBm, R_L = 12.5Ω
- Input voltage noise: 4.5nV/√Hz @100kHz
- Low supply current: 9mA/amplifier (full power mode)
- Standby mode (4.5mA/amplifier)
- Shutdown mode (0.3mA/amplifier)

Figure 6-151: AD8018 xDSL line driver key specifications

References: Communications Amplifiers

1. Bob Clarke, "Find Op Amp Noise with Spreadsheet," **Electronic Design**, December 13, 1990, or Analog Devices AN253.
2. Barrie Gilbert, "A Low Noise Wideband Variable-Gain Amplifier Using an Interpolated Ladder Attenuator," **IEEE ISSCC Technical Digest**, 1991, pp. 280, 281, 330.

SECTION 6-5

Amplifier Ideas

Walt Jung, Walt Kester

This section of the chapter features miscellaneous op amp applications, within a format of *amplifier ideas*. They range broadly across the spectrum, illustrating many innovative op amp uses that don't otherwise fit categories. Some of the concepts have been inspired by publication elsewhere. In such cases, an appropriate original reference is given.

High Efficiency Line Driver

Conventional video line drivers use a series or *back-termination* resistor, selected to match the transmission line characteristic impedance. Although simple, this scheme is inherently inefficient, as both load and series termination resistors drop the same voltage. This isn't usually a problem with 1 V p-p video signals operating on high voltage supplies, such as ±12 V or ±15 V. However, with lower voltage supplies, particularly 5 V or less, driver headroom is definitely an issue. For such conditions, a conventional driver may simply not be able to accommodate a signal of twice V_{OUT} without distortion.

Figure 6-152 illustrates a solution to this driver efficiency problem. In this line driver (adapted from a circuit by Victor Koren, see Reference 1), a Howland type of feedback configuration is used. This allows the series termination resistor R5 to be appreciably smaller, thus dropping less voltage and improving stage efficiency. Both positive and negative loop feedback paths are used around the op amp, R3 and R4, plus R1 and R2. An AD817 is chosen for its video characteristics, and line driving capability. The circuit also works with many other op amps, provided they have sufficient output drive.

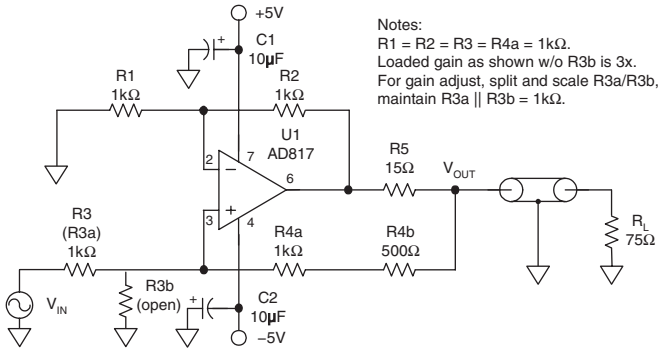


Figure 6-152: A high efficiency video line driver

In this example, a 75 Ω line is being driven, and R5 is set to 15 Ω. With the scaling chosen, this produces 1/5 the voltage drop of a more conventional 75 Ω resistor. For every volt of V_{OUT}, the amplifier needs only to produce 20% more, i.e., 1.2 V per V of V_{OUT}. This allows the design to operate easily on 5 V or even lower supplies, and still provide undistorted 1 V p-p video signals at V_{OUT}. The ± feedback paths produce the proper synthesized source impedance when the R1–R5 resistors are properly selected.

Given the desired output impedance R_O, R5 is related by a scaling factor, so that $R5 < R_O$. A direct design approach is to simply set R5 at some fraction of R_O, which then leads to a R1 through R4 resistor set that will provide the proper R_O. In this example design, R5 is set at 1/5 R_O as noted earlier, or 15 Ω.

As per the notes of the figure, a major simplifying design step is to make four of the feedback resistors equal, namely R1 through R3 and R4a. It also helps further to make these a common, readily available value. This should be a value moderately higher than the target load impedance. In this case, a 1 kΩ base value is chosen.

This defines the R4 value (R4a + R4b) as:

$$R4 = \left(R5 \times R1 + R_O \times R2\right) / \left(R_O - R5\right) \qquad \text{Eq. 6-31}$$

R4b is then simply R4-R4a. The design is further simplified with all of the noted resistors part of a single common array, *including* R4b (which is made from two parallel 1 kΩ resistors in this case). Note that R4b won't necessarily be so easily achieved in other design examples. Nevertheless, it is desirable for as many of the R1 through R4 resistors as possible be part of a common array, matched to 1% or better.

Gain of the stage just as shown is about 3× with the output loaded. If gain must be adjusted, there is a specific procedure to be followed. This is a necessary condition for proper stage function (for any gain), and is needed to maintain the synthesized R_O. For example, if a unity (1×) overall gain is desired, R3 can be changed to two resistors, i.e., R3a = 3 kΩ, R3b = 1.5 kΩ. Note that this reduces the drive to the op amp, but it also maintains the same 1 kΩ Thevenin impedance for R3 (where R3 is the resistance looking back to the input from R4a). Similarly, equal value 2 kΩ resistors could be used, which provides a net loaded stage gain of 1.5×. Of course, for arbitrary gains, a common array may not be possible, and ordinary 1% metal film types can also be used.

Also related to the above, the driving source at V_{IN} must be a very low impedance with respect to 1 kΩ, again to maintain the synthesized impedance relations. This is best achieved by use of an R3 driving source direct from an op amp output. Alternately, if the V_{IN} driving impedance is both fixed and known, it can be subtracted from R3.

A more general caveat (which applies to all Howland circuits) is that the design environment must maintain this source driving impedance *for all conditions*, as the circuit itself is *not* open source stable. For example, if R3 is opened, the positive feedback can override the negative feedback via R1 and R2, and the circuit could latch up.

Finally, although this design illustrates a driver oriented to a video standard of 75 Ω with 1 V p-p signals, there is no reason why the same design principles cannot be applied to other impedances and/or signal levels.

A Simple Wide Bandwidth Noise Generator

While most electronic designs seek noise minimization, there are occasions where a known quantity and/or quality of spectrally flat (white) noise is desirable. One such example is a dither source for enhanced dynamic resolution A/D conversion. For such applications, it is useful to be able to predict the output of a noise generator. It turns out that a carefully chosen decompensated op amp set up to amplify its own input noise is very useful as a wideband noise generator (see Reference 2).

Figure 6-153 illustrates this technique, which simply employs the op amp U1 as a fixed gain stage, amplifying its input noise by the stage factor G, where G = 1 + (R1/R2). This process is made easier by some simplifying assumptions, described next.

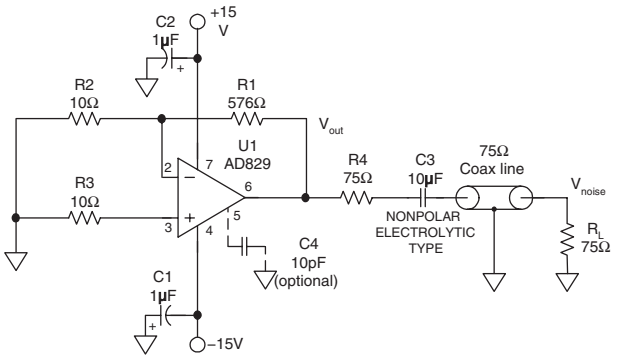


Figure 6-153: A simple wideband noise generator

By purposely selecting R2 and R3 values of 10 Ω or less, their Johnson noise contribution is forced to be less than the voltage noise of the amplifier. Similarly, the amplifier's current noise components in R2-R3, when converted to voltage noise, are also negligible. Thus the dominant circuit noise is reduced to the input voltage noise of U1.

To scale the amplifier noise to a given level of V_{noise} across R_L, select a stage gain which produces a noise density at V_{OUT} which is 2G times the typical U1 noise of $1.7\,nV/\sqrt{Hz}$. This will produce a V_{OUT} twice V_{noise}. For example, for a V_{noise} of $50\,nV/\sqrt{Hz}$, using a fixed R2 value of 10 Ω, the required R_1 is:

$$R1 = 10 \times \left(\left(\left(2 \times V_{NOISE}\right)/1.7\right) - 1\right) \qquad \text{Eq. 6-32}$$

Where V_{noise} is in $nV/\sqrt{Hz}$, and the 1.7 is the U1 voltage noise ($nV/\sqrt{Hz}$). This computes to 576 Ω (nearest standard value) for a wideband $50\ nV/\sqrt{Hz}$. Alternately, an audio range noise source of $1000\ nV/\sqrt{Hz}$ with several hundred kHz of bandwidth is achieved with R1 = 11.8 kΩ, and C3 = 100 µF. By choosing a bipolar-input, voltage feedback U1 device, with a single effective gain stage, a major performance point is achieved. Such an amplifier has a flat, frequency-independent input voltage noise response (i.e., a white noise characteristic). Many of the ADI high speed amplifiers use this topology within a folded cascode architecture.

In contrast to this, multiple stage, pole-zero compensated amplifiers such as the OP27 (and other similar architectures) can have peaks in the output noise response. This is due to the frequency compensation method used, and the associated gain distributions in the signal path. When picking U1, look for a noise characterization plot that shows flat input-referred voltage noise over several decades.

For the AD829 device used, input voltage noise is flat from below 100 Hz to more than 10 MHz, as is noted in Figure 6-154. Within the actual circuit, the upper bandwidth limit will be gain/compensation dependent, which can be controlled as described next.

The output is coupled through a nonpolar capacitor, C3, which removes any amplified dc offset at V_{out}. The C3 value should be large enough to pass the lowest noise frequencies of interest. As shown the response of this network is –3 dB at about 100 Hz, but C3 can be

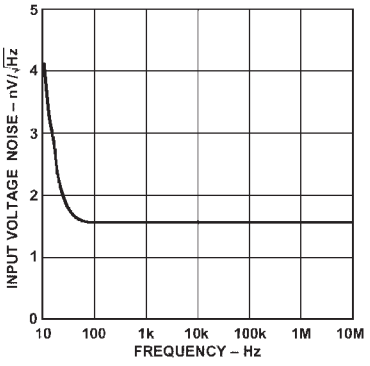


Figure 6-154: AD829 input voltage noise spectral density

changed for other low frequency limits. Source termination resistance R4 allows standard 75 Ω cables to be driven, providing distribution to a remote 75 Ω load, R_L.

In general, this noise generator's utility is greatest with a decompensated (or externally compensated) op amp, to take advantage of the maximum bandwidth possible. For the AD829, bandwidth is highest with lowest Pin 5 capacitance (i.e., no PCB Pin 5 pad, or Pin 5 cutoff). Conversely, C4 can be used to reduce bandwidth, if desired. With minimum Pin 5 capacitance, the AD829 gain bandwidth can be above 500 MHz, allowing extended response. In any case, the stage's effective –3 dB bandwidth varies inversely proportional to stage gain G. Some noise variations can be expected from IC sample-sample, so an R1 trim method can be used to set a output calibration level. Alternately, if ultrawide bandwidth noise isn't required, another op amp to consider is the AD817.

A final note—bipolar input amplifiers such as the AD829 typically use PTAT biasing for the input's differential stage tail current. Since equivalent input noise varies as the square root of this tail current, this can make noise output vary somewhat with temperature. The net effect causes noise to change less than 1 dB for a 50°C temperature change.

Single-Supply Half- and Full-Wave Rectifier

There are a number of ways to construct half- and full-wave rectifiers using combinations of op amps and diodes, but the circuit shown in Figure 6-155 requires only a dual op amp, two resistors, and operates on a single supply (see Reference 3).

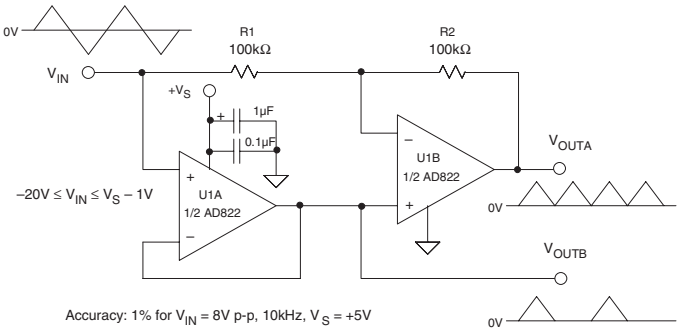


Figure 6-155: Single-supply half- and full-wave rectifier uses no diodes

The circuit will work with any single-supply op amp whose inputs can withstand being pulled below ground. The AD820 (single) or AD822 (dual) op amps have N-channel JFET inputs, which allow the input voltage to go to 20 V below the negative supply.

The output stage of these op amps is a complementary bipolar common emitter rail-to-rail stage with an output resistance of approximately 40 Ω when sourcing current and 20 Ω when sinking current. As a result of this stage, the outputs can go within a few millivolts of the supply rails under light loading.

When the input signal is above ground, unity-gain follower U1A and the loop of the amplifier U1B bootstrap R1. This bootstrapping forces the inputs of U1B to be equal. Thus, no current flows in R1 or R2, and the output V_{OUTA} tracks the input. Conversely, when the input is negative, the output of U1A is forced to zero (saturated). The noninverting input of U1B sees the ground-level output of U1A, and during this phase operates as a unity-gain inverter, rectifying the negative portion of the input V_{IN}.

The net output at V_{OUTA} is therefore a full-wave rectified version of VIN. In addition, a half-wave rectified version is obtained at the output of U1A (V_{OUTB}) if desired.

The circuit operates with a single power supply of 3 V to 20 V. The circuit will maintain an accuracy of better than 1% over a 10 kHz bandwidth for inputs of 8 V p-p on a +5 V supply. The input should not go more than 20 V below the negative supply, or closer than 1 V to the positive supply. Inputs of ±18 V can be rectified using a single +20 V supply.

Paralleled Amplifiers Drive Loads Quietly

Paralleling op amps is a method to increase load drive while keeping output impedance low, and also to reduce noise voltage. Figure 6-156A shows a classic stacked-amplifier circuit. This configuration halves the input voltage noise of a single op amp, and quadruples load drive. However, it does have several weaknesses.

First, it is necessary to *individually* set the correct gain for each amplifier. Second, series resistors must be added to each output, to ensure equal load current distribution among the op amps. Third, the input range can become limited at high gains because of the inherent offset of any of the amplifiers.

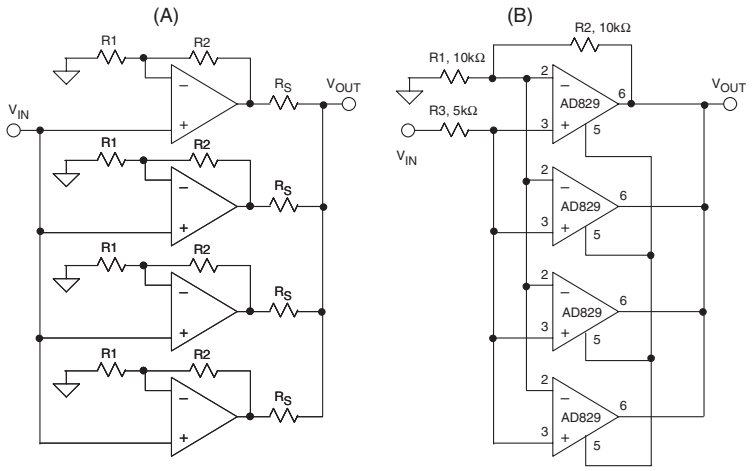


Figure 6-156: Paralleled amplifiers drive loads quietly

The circuit shown in Figure 6-156B also has half the noise voltage of an individual amplifier, and it also quadruples the load drive. But in so doing, it reduces the component count from twelve resistors to three (see Reference 4). In addition, the circuit has a gain-bandwidth product of about 750 MHz. Although the topology of Figure 6-156B is generally applicable to all externally compensated amplifiers (i.e., those with a pinned-out high impedance node before the output driver stage—such as the AD844 and AD846), the AD829 op amp is particularly well suited to video and other broadband applications.

Note that in the B circuit, external R_S load sharing resistors aren't required, because the only voltage difference between the individual outputs is due to the slight offset mismatch between the AD829 complementary emitter follower output driver stages, and internal 15 Ω emitter resistors ensure equal output current distribution. The closed-loop gain has no effect on this small offset voltage.

The end result of the four paralleled output stages in Figure 6-156B is a composite amplifier with both greater load drive and lower noise, but using only the conventional feedback components. The circuit in B increases the drive current by a factor of four, similar to A, but with a vast difference in the parts count.

In order to understand how the circuit reduces noise, let the RTI voltage noise of the individual op amps be V_{N1}, V_{N2}, V_{N3}, and V_{N4}, and let the total noise voltage be V_N.

Because all the inputs are connected in parallel, as well as the high impedance nodes, then:

$$(V_N - V_{N1})gm + (V_N - V_{N2})gm + (V_N - V_{N3})gm + (V_N - V_{N4})gm = 0 \qquad \text{Eq. 6-33}$$

$$V_N = ¼(V_{NI} + V_{N2} + V_{N3} + V_{N4}). \qquad \text{Eq. 6-34}$$

But because the voltage noise of the amplifiers is uncorrelated, and the noise spectral density for each amplifier is the same:

$$V_N = ¼\sqrt{\left[4(V_{N1})^2\right]} \qquad \text{Eq. 6-35}$$

$$V_N = V_{N1} / 2 \qquad \text{Eq. 6-36}$$

This result also implies that all uncorrelated parameters such as input offset voltage, input offset voltage drift, CMRR, PSRR, and so forth, will also approach their true mean values, thus reducing effects arising from the variability of the devices.

The AD829 is flexible and can operate on supply voltages from ±5 V to ±15 V. It's uncompensated gain-bandwidth product is 750 MHz. Nominal output current for rated performance is 20 mA, so in the circuit shown, 80 mA is available to drive the load.

The input voltage noise of a single AD829 is $1.7\ \text{nV}/\sqrt{\text{Hz}}$, so the parallel circuit has an input voltage noise of approximately $0.85\ \text{nV}/\sqrt{\text{Hz}}$. In order to take advantage of this low voltage noise, however, the circuit must be driven from a relatively low source impedance, because the input current noise of a single AD829 is $1.5\ \text{pA}/\sqrt{\text{Hz}}$. In the parallel circuit, the input current noise is therefore $3\ \text{pA}/\sqrt{\text{Hz}}$.

Notice that in the AD829 circuit, R3 = R1||R2 for bias current cancellation. This works because the input bias currents of the AD829 are not internally compensated: they are approximately equal, and of the same sign. If amplifiers with internal bias current compensation or current feedback op amps are used, the input bias currents may not be equal or of the same sign, and R3 should be made equal to zero.

Power-Down Sequencing Circuit for Multiple Supply Applications

The operating time of battery operated portable equipment can be extended by using power-down techniques. Many new components offer a power-down feature to implement this function. However, there may be times when this feature is not offered and other means must be devised. The solution may also require proper power supply sequencing in multiple supply systems.

Figure 6-157 shows a single-supply op amp powered from 15 V driving an single-supply ADC powered from 5 V. In many cases, the same 5 V can supply the op amp and the ADC, and in that case, there is no sequencing problem. However, in some cases better system performance is obtained by driving the op amp with a higher supply voltage.

In the circuit, MOSFETs Q1 and Q2 switch the 5 V and the 15 V to the devices in the proper sequence. On power-up, the voltage to the ADC must be supplied first; and on power-down, the voltage to the ADC must be removed last. This is to ensure that the V_{IN} input to the ADC is never more than 0.3 V above the V_{DD} positive supply or more than 0.3 V below the negative supply, thereby preventing damage and possible latch-up.

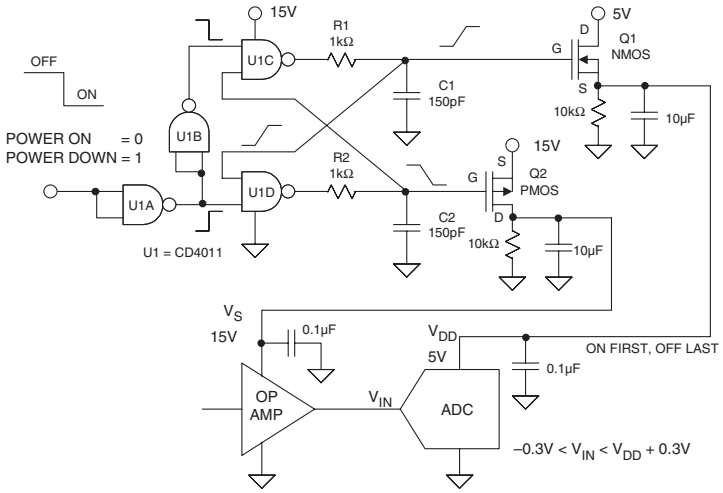


Figure 6-157: Power-down sequencing circuit for multiple supply applications

The MOSFETs, Q1 and Q2 switch the 5 V and the 15 V to the ADC and the op amp, respectively, in a sequence controlled by two cross-coupled CD4011 CMOS NAND gates (U1C and U1D). The gates are powered from the 15 V supply so that sufficient gate drive voltage is available to turn Q1 and Q2 on and off.

To initiate the power-on mode, a logic 0 is applied to the input of U1A, forcing its output high. This forces the output of U1B low, which causes U1C's output to go high. The R1-C1 time constant delays the application of the 15 V to the gate of Q1 which ultimately turns Q1 on with 5 V at its source. The delayed output of U1C is also applied to an input of U1D which forces its output low. U1D's output is delayed by the R2-C2 time constant, and ultimately forces the gate of Q2 to zero, which applies 15 V to the drain of Q2, and to the op amp V_S supply.

To initiate the power-down mode, a logic 1 is applied to the input of U1A which forces its output to zero, and the output of U1D is forced high, ultimately turning off Q2, the 15 V supply. The delayed output of U1D is applied to an input of U1C, the output of U1C goes low, and ultimately the gate of Q1 is forced to zero, turning off the 5 V to the V_{DD} input of the ADC.

It is important to note that when system power is applied to the overall circuit, the 5 V should come up either before, or simultaneously with, the 15 V. Similarly, when system power is removed, the 15 V should be removed first or simultaneously with the 5 V.

This circuit is based on a modification of the one described in Reference 5, where the desired sequencing is the reverse of the one described here. The reverse sequence (15 V turned on before 5 V, and 5 V turned off before 15 V) can be easily achieved by replacing the CD4011 NAND gates with CD4001 NOR gates, reversing the "sense" of the power-on/power-down control input, and swapping the gate drive signals to Q1 and Q2.

Programmable Pulse Generator Using the AD8037 Clamping Amplifier

The AD8036 (G ≥ 1 stable) and AD8037 (G ≥ 2 stable) clamp amplifier outputs can be set accurately to well controlled flat levels determined by the clamping voltages. This, along with wide bandwidth and high slew rate suits them well for numerous applications.

A basic description of the AD8036/AD8037 operation can be found in the Video Applications section of this chapter. Figure 6-158 is a diagram of a programmable level pulse generator (see Reference 6).

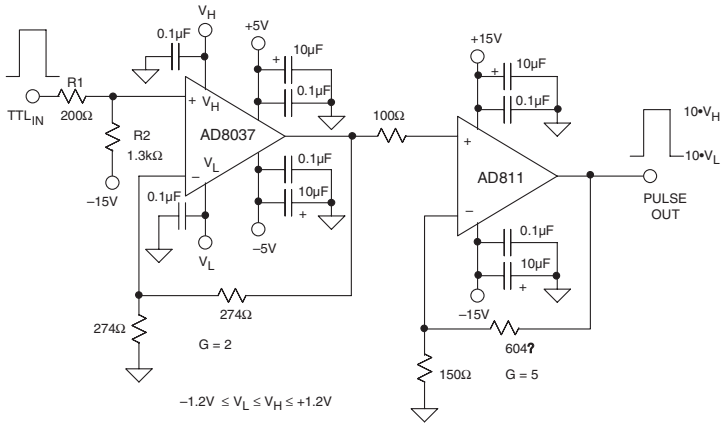


Figure 6-158: Programmable pulse generator using AD8037 clamping amplifier

The circuit accepts a TTL timing signal for its input and generates pulses at the output up to 24 V p-p with 2500 V/µs slew rate. The output levels can be programmed to anywhere in the range between –12 V to +12 V.

The circuit uses an AD8037 operating at a gain of two with an AD811 to boost the output to the ±12 V range. The AD811 was chosen for its ability to operate with ±15 V supplies and its high slew rate. R1 and R2 level shift the TTL input signal level approximately 2 V negative, making it symmetrical above and below ground. This ensures that both the high and low logic levels will be clamped by the AD8037. For well controlled signal levels in the output pulse, the high and low output levels result from the clamping action of the AD8037 and aren't controlled by either the high/low logic levels passing through a linear amplifier. For good output rise/fall times, logic with high edge speed should be used.

The high logic levels are clamped at two times the voltage at V_H, while the low logic levels are clamped at two times the voltage at V_L. The output of the AD8037 is amplified by the AD811 operating at a gain of 5. The overall gain of 10 will cause the high output level to be 10 times the voltage at V_H, and the low output level 10 times the voltage at V_L. For this gain, the clamping levels for a ±12 V output pulse are V_H = +1.2 V and V_L = −1.2 V.

Full-Wave Rectifier Using the AD8037 Clamping Amplifier

The clamping inputs can be used as additional inputs to the AD8036/AD8037. As such, they have an input bandwidth comparable to the amplifier inputs and lend themselves to some unique functions when they are driven dynamically.

Figure 6-159 is a schematic for a full-wave rectifier, also called an absolute value generator (Reference 6). It works well up to 20 MHz and can operate at significantly higher frequencies with some performance degradation. The distortion performance is significantly better than diode-based full-wave rectifiers, especially at high frequencies.

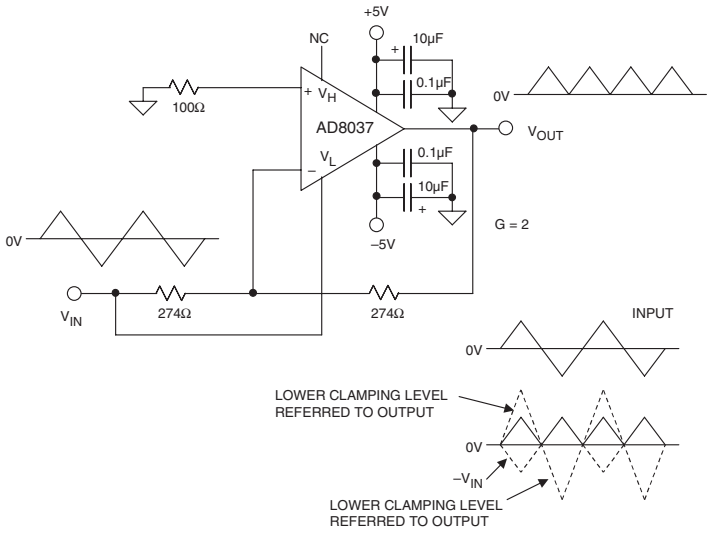


Figure 6-159: Full-wave rectifier using the AD8037 clamping amplifier

The AD8037 is configured as an inverting amplifier with a gain of unity. The V_{IN} input drives the inverting amplifier and also directly drives V_L, the lower level clamping input. The high level clamping input, V_H, is left floating and plays no role in the circuit.

When the input is negative, the amplifier acts as a unity-gain inverter and outputs a positive signal at the same amplitude as the input, with opposite polarity. V_L is driven negative by V_{IN}, so it performs no clamping action, because the positive output signal is always higher than the negative level driving V_L.

When the input is positive, the output result is the sum of two separate effects. First, the inverting amplifier multiplies the V_{IN} input by –1, because of the unity-gain inverting configuration. This effectively produces an offset at the output, but with a dynamic level that is equal to –1 times the input. Second, although the positive input is grounded (through 100 Ω), the output is clamped at two times the voltage applied to V_L (a positive, dynamic voltage in this case). The factor of two is because the 2× amplifier noise gain.

The sum of these two actions results in an output that is equal to unity times the input signal for positive input signals, as shown in Figure 6-159. Thus, for either positive or negative input signals, the output is unity times the absolute value of the input signal. The circuit can be easily configured to produce the negative absolute value of the input by applying the input to V_H rather than V_L.

The circuit can get to within about 40 mV of ground during the time when the input crosses zero. This voltage is fixed over a wide frequency range, and is a result of the switching between the conventional op amp input and the clamp input. However, because there are no diodes to rapidly switch from forward to reverse bias, the performance far exceeds diode-based full-wave rectifiers. Signals up to 20 MHz can be rectified with minimal distortion.

If desired, the 40 mV offset can be removed by adding an offset to the circuit, with little additional complexity. A 27.4 kΩ input resistor to the inverting input will have a gain of 0.01, while changing the gain of the circuit by only 1%. A plus or minus 4 V dc level (depending on the polarity of the rectifier) fed into this resistor will then compensate for the offset.

Full-wave rectifiers are useful in many applications including AM signal detection, high frequency ac voltmeters, and various arithmetic operations.

AD8037 Clamping Amplifier Amplitude Modulator

The AD8037 can also be configured as an amplitude modulator as shown in Figure 6-160 (Reference 6). The positive input of the AD8037 is driven with a square wave of sufficient amplitude to produce clamping action at both the high and low levels set by V_H and V_L. This is the higher frequency carrier signal.

The modulation signal is applied to both the input of a unity gain inverting amplifier and to V_L, the lower clamping input. V_H is biased at 0.5 V for the example to be discussed but can assume other values.

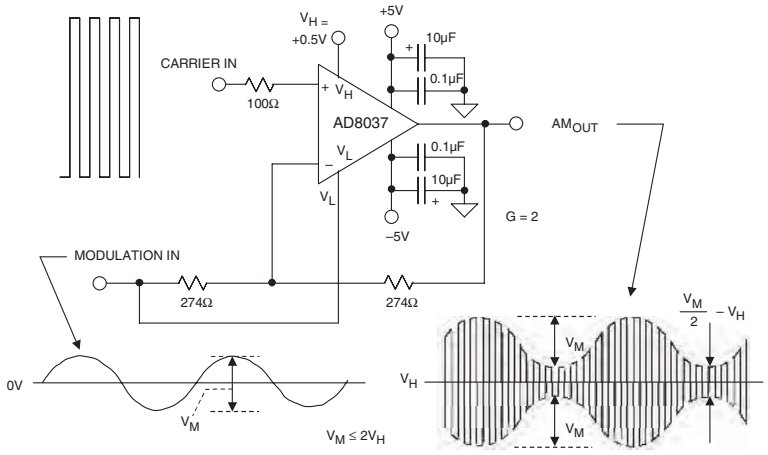


Figure 6-160: AD8037 clamping amplifier amplitude modulator

To understand the circuit operation, it is helpful to first consider a simpler circuit. If both V_H and V_L are dc-biased at +0.5 V and −0.5 V, respectively, and the carrier and modulation inputs driven as above, the output would be a 2 V p-p square wave at the carrier frequency riding on a waveform at the modulating frequency.

The inverting input (modulation signal) is creating a varying offset to the 2 V p-p square wave at the output. Both the high and low levels clamp at twice the input levels on the clamps because the noise gain of the circuit is two.

When V_L is driven by the modulation signal instead of being held at dc level, a more complicated situation results. The resulting waveform is composed of an upper envelope and a lower envelope with the carrier square wave in between. The upper and lower envelopes are 180° out of phase as in a typical AM waveform.

The upper envelope is produced by the upper clamp level being offset by the waveform applied to the inverting input. This offset is the opposite polarity of the input waveform because of the inverting configuration.

The lower envelope is produced by the sum of two effects. First, it is offset by the waveform applied to the inverting input as in the case of the simpler circuit above. The polarity of this offset is in the same direction as the upper envelope.

Second, the output is driven in the opposite direction of the offset at twice the offset voltage by the modulation signal being applied to V_L. This results from the noise gain being equal to two, and since there is no inversion in this connection, it is opposite in polarity from the offset.

The result at the output for the lower envelope is the sum of these two effects, which produces the lower envelope of an AM waveform. The depth of modulation can be modified by changing the amplitude of the modulation signal. This changes the amplitude of the upper and lower envelope waveforms.

The modulation depth can also be changed by changing the dc bias applied to V_H. In this case, the amplitudes of the upper and lower envelope waveforms stay constant, but the spacing between them changes. This alters the ratio of the envelope amplitude to the amplitude of the overall waveform.

For V_H = +0.5 V, 100% modulation occurs when the peak-to-peak amplitude of the modulation input V_M = 1 V. The AM output is always offset by V_H for a bipolar modulation input. In general, for a peak-to-peak modulation amplitude of V_M, the two output modulated envelopes are separated by an amount equal to $V_M/2 - V_H$.

Sync Inserter Using the AD8037 Clamping Amplifier

Video signals typically combine an active video region with both horizontal and vertical blanking intervals during their respective retrace times. A sync signal is required during the blanking intervals in some systems. In RGB systems, the sync is usually inserted on the Green signal. In composite video systems, it is inserted during blanking on the single-channel composite signal, or on the luminance (or Y) signal in an S-video system. Further details on video signals can be found in the Video Applications section of this chapter.

The AD8037 input clamping amplifier can be used to make a video sync inserter that does not require accuracy in the amplitude or shape of the sync pulse (see Reference 7). The circuit shown in Figure 6-161 uses the AD8037 to create the proper amplitude sync insertion, and the dc levels of the sync pulse do not affect the active video level. The circuit is also noninverting with a gain-of-two, which allows for driving a back-terminated cable with no loss of amplitude.

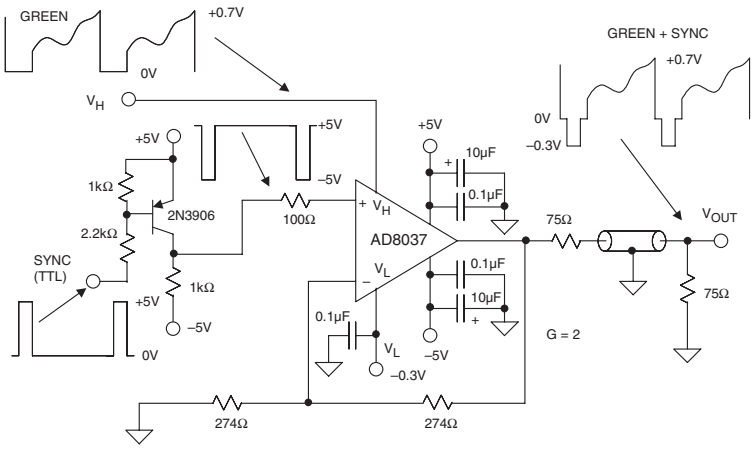


Figure 6-161: Sync inserter using the AD8037 clamping amplifier

The Green video signal is applied to the VH input of the AD8037. This signal has a blanking level of 0 V and an approximate full-scale value of 0.7 V. The TTL-level sync pulse is applied to the base of the 2N3906 transistor. The signal at the collector of the 2N3906 are inverted sync pulses with an amplitude of 10 V p-p which are applied to the noninverting input of the AD8037.

The amplitude of the signal into the noninverting input of the AD8037 is 5 V during the active video portion, and since this is greater than the maximum positive Green signal excursion of 0.7 V on the V_H input, the Green signal is passed through to the output of the AD8037 with a gain of +2.

During the blanking interval, the sync signal into the noninverting input of the AD8037 goes to −5 V, and the output of the AD8037 is clamped to a value which is two times the dc level on the V_L input. Nominally, the sync should be −0.3 V referenced to a 0 V blanking level, and this level is applied to V_L from a voltage reference, or a simple divider.

The high and low levels of the sync pulse generated by the 2N3906 can be relatively loosely defined. The value of the high-level sync input to the noninverting input of the AD8037 must be higher than the active video signal; the value of the low level sync input must be lower than the dc voltage on the V_L input. The rising and falling edges of the sync pulse input determine the timing of the inserted sync, but the dc level at the V_L input of the AD8037 will always determine the sync amplitude.

The 2N3906 PNP transistor serves as a level translator and simply provides an appropriate drive signal from a TTL source of positive-going sync. The sync input to the noninverting input of the AD8037 neither influences the dc level of the output video nor determines the amplitude of the inserted sync.

AD8037 Clamped Amplifier As Piecewise Linear Amplifier

Piecewise linear amplifiers are often implemented using diodes in the feedback loop of an op amp. When the diodes become forward biased, they switch in resistors that alter the closed-loop gain of the amplifier.

This approach has three disadvantages. First, the diode's forward voltage drop (even with Schottky diodes) reduces accuracy and speed during the switching region. Second, diode stray capacitance can limit bandwidth. Third, the 2 mV/ºC drift of the diode's forward bias voltage introduces errors in the transfer function. The circuit shown in Figure 6-162 avoids these problems by using the fast and accurate clamping function of the AD8037 to set the breakpoints (see Reference 8).

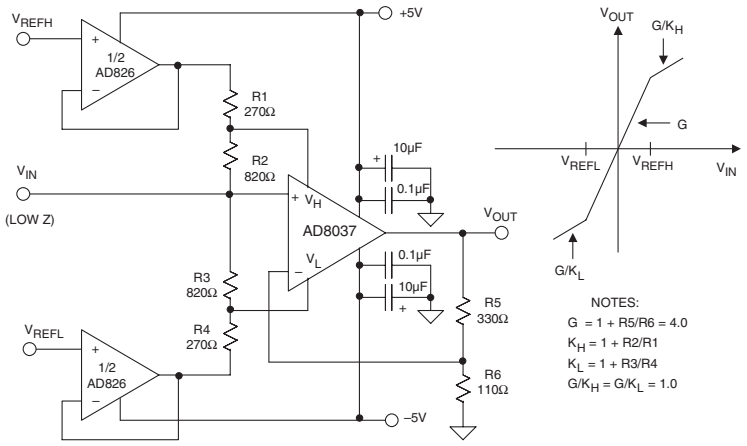


Figure 6-162: Piecewise linear amplifier uses AD8037 clamping amplifier rather than diodes

If the V_{IN} signal applied to the noninverting input of the AD8037 lies between the clamp voltages (set by V_{REFH} and V_{REFL}), the AD8037 works as a standard op amp with a gain = G = 1 + R5/R6. If the input signal is greater than the upper clamp voltage, V_H, the amplifier disconnects the input signal, and V_H becomes the noninverting signal input. Likewise, if the signal at the noninverting input of the AD8037 is below the lower clamp voltage, V_L, the amplifier also disconnects the signal input, and V_L becomes the noninverting signal input.

Figure 6-162 also graphically illustrates the operation of the circuit. When V_{IN} is between V_{REFH} and V_{REFL}, the circuit is a standard noninverting op amp with a gain G = 1 + R5/R6. When V_{IN} is greater than V_{REFH}, V_H becomes the noninverting input to the amplifier.

The transfer function from V_{IN} to V_{OUT} comprises two parts under this condition. From V_{IN} to V_H, the signal is attenuated by a factor K_H = 1 + R2/R1. From V_H to V_{OUT}, the gain remains G = 1 + R5/R6. This leads to an overall gain of G/K_H in this region. The circuit behaves similarly when V_{IN} is below V_{REFL}. The gain in this condition is G/K_L, where K_L = 1 + R3/R4.

Careful layout ensures adherence to the desired nonlinear transfer function over a 5 MHz bandwidth. The stability of the breakpoints is determined by the tracking of the resistor temperature coefficients, the 10 µV/ºC offset voltage drift of the AD8037, and the temperature stability of the reference voltages.

The reference voltages can be generated using precision voltage references or DACs. To maintain accuracy, the reference voltages should be buffered with a fast op amp, such as the dual AD826, to provide a low source impedance throughout the input signal bandwidth.

The analog input voltage, V_{IN}, should also be driven from a low impedance source, such as an op amp, to prevent errors due to the loading effect of the R1-R2-R3-R4 network.

Using the AD830 Active Feedback Amplifier as an Integrator

The active feedback amplifier topology used in the AD830/AD8130 can be used to produce a precision voltage-to-current converter which, in turn, makes possible the creation of grounded-capacitor integrators (see Reference 9).

The design discussed here uses the AD830 to deliver a bipolar output current at high impedance (see Figure 6-163). Using R = 1 kΩ, the output current is simply equal to V_{IN}/R, or 1 mA per volt of input. The maximum output current is limited to ±30 mA by the output drive capability of the AD830.

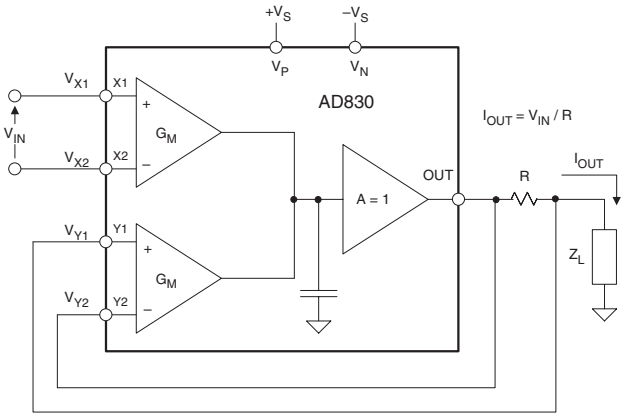


Figure 6-163: Constant current source using the AD830 active feedback amplifier

The output resistance is determined by the CMR performance of the AD830. A CMR of 60 dB yields an effective output resistance of 1000 × R. The output impedance at any frequency can be determined by consulting the CMR data provided in the data sheet. The compliance range on the output is ± (V_S – 2 V) reduced or increased by V_{IN}.

Figure 6-164A shows a standard op amp integrator circuit using the AD825, and Figure 6-164B shows the improved AD830 grounded-capacitor circuit. The dc operating point for testing purposes is determined by R1 in the AD825 op amp circuit, and by R1 and C1 in the AD830 circuit. R2 and C2 determine the integrator time constant in both circuits.

If the op amp in Figure 6-164A is assumed to be ideal, i.e., zero output impedance, and infinite input impedance, then the only difference between the two circuit topologies is the finite input resistance of the op amp based integrator as set by R2.

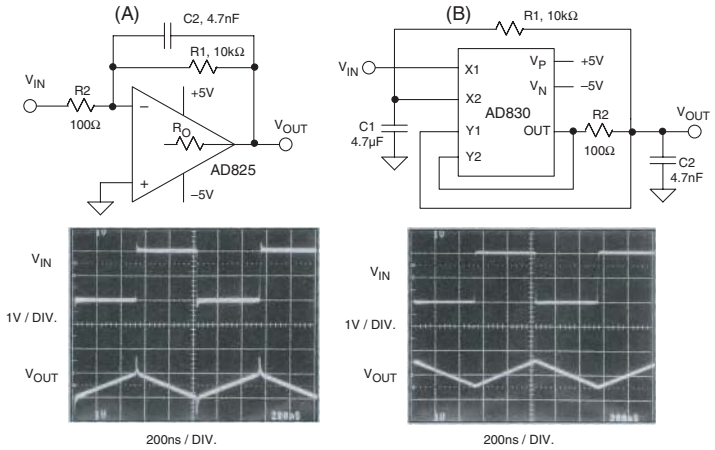


Figure 6-164: Traditional op amp integrator versus grounded capacitor integrator

However, in a real op amp, the output resistance is finite and increases with signal frequency as the open-loop gain decreases. This causes the "ground" at the output of the op amp to degrade at high frequencies. The result is a relatively large spike on the output voltage waveform whenever the input switches.

This can be explained as follows. Assume the input V_{IN} switches between $-V_A$ and $+V_A$. When the input is at $-V_A$ long enough for the op amp to settle, the current in resistor R2 is $-V_A$/R2 and the output increases due to C2 being charged by the op amp. As V_{IN} suddenly switches to $+V_A$, the voltage across C2 cannot change instantaneously, and neither can the op amp's output because it behaves itself as an integrator. This implies that the change in input voltage will be impressed upon the voltage divider formed by the R_O of the op amp and R2. This change in voltage at V_{OUT} will also be coupled by C2 to the summing node at the inverting input of the op amp.

If V_{IN} is generated by a source with finite source resistance, this voltage spike will also appear at the input. Only after the amplifier settles will the external components again define the integrator time constant and the circuit function as desired.

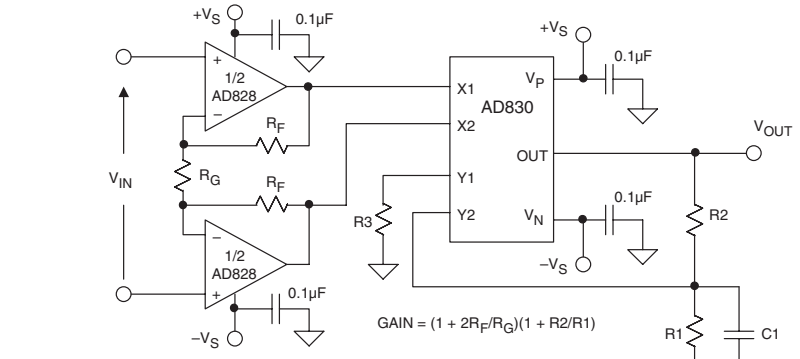
It can be seen by comparing the waveforms of (A) and (B) that no spike develops in the output waveform produced by the grounded capacitor integrator using the AD830. This is because the integrating capacitor

is connected to a true ground. In addition, the input is completely isolated from the output. Therefore, if an aberration did occur, it would not be coupled back to the driving source.

Various active filter topologies can be realized from this fundamental integrator building block. For example, two such sections can implement a biquad. An example of a simple all-pass filter using the AD830 is described in Reference 10.

Instrumentation Amplifier with 290MHz Gain-Bandwidth

The circuit shown in Figure 6-165 combines a dual AD828 op amp with the AD830 active feedback difference amplifier to form a high frequency instrumentation amplifier (see Reference 11). The circuit's performance for ±5 V supplies for gains of 10 and 50 are shown in the figure, along with appropriate component values.



NOTE: V_S = ±5V

GAIN	R_F	R_G	R1	R2	R3	C1
10	1050Ω	1050Ω	348Ω	348Ω	169Ω	60pF
50	1150Ω	255Ω	127Ω	510Ω	100Ω	300pF

GAIN	3dB BW	SLEW RATE	0.1% SETTLING TIME	CMR@1MHz	V_N@10kHz	I_N@10kHz	V_{OS}	I_S
10	14.2MHz	200V/µs	80ns	64dB	15nV/√Hz	1.5pA/√Hz	0.6mV	27.5mA
50	5.8MHz	60V/µs	200ns	64dB	15nV/√Hz	1.5pA/√Hz	0.6mV	27.5mA

Figure 6-165: Instrumentation amplifier with 290 MHz gain bandwidth

The circuit can be configured for different gains, and will operate on supplies ranging from ±4 V to ±16.5 V.

The gain is proportioned between the AD828 stage and the AD830 stage, such that the closed-loop bandwidths of both stages are approximately equal. Under these conditions, a gain bandwidth of 290 MHz is obtained.

The input AD828 stage dominates the effective referred-to-input (RTI) input voltage noise and offset voltage. Capacitor C1 causes gain peaking in the AD830 which compensates for the AD828 input stage roll-off. The optimum value for C1 must be determined experimentally in a prototype or by a careful SPICE evaluation.

Note that R3 is made equal to the parallel combination of R1 and R2 to provide first-order input bias current cancellation at the Y1-Y2 input of the AD830.

Programmable Gain Amplifier with Arbitrary Attenuation Step Size

The R/2R ladder is a popular resistor topology often used to implement a current or voltage 6 dB step attenuator. However, if the resistors are appropriately scaled, the network can be modified to provide any desired attenuation step.

A programmable gain amplifier (PGA) can be made with a attenuating ladder network followed by CMOS multiplexer and a fixed gain amplifier, as in Figure 6-166. This circuit has several advantages (see Reference 12).

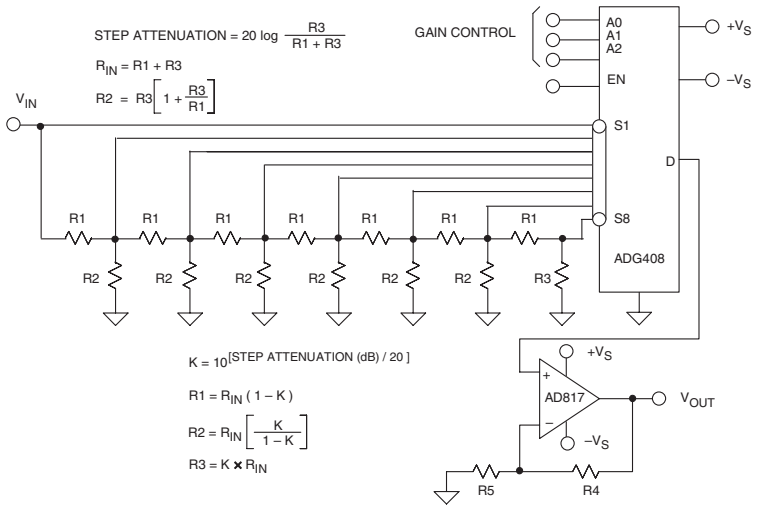


Figure 6-166: Programmable gain amplifier with arbitrary attenuation step size

First, as stated previously, the attenuation step size doesn't have to be 6 dB. Manipulating the resistor ratios, as described below, can easily change it. Second, the bandwidth of the circuit is always the same, regardless of the attenuation, due to the fact that the op amp buffer operates at a fixed gain. Third, the circuit is flexible, because practically any CMOS multiplexer and op amp can be used. The bandwidth of the circuit is determined primarily by the output op amp. Switching time between gain settings is determined by the multiplexer switching time and the op amp settling time.

The resistor ladder as shown uses three different resistor values: R1, R2, and R3. The step attenuation in dB is given by

$$\text{Step Attenuation}\,(\text{dB}) = 20\log\left[\text{R3}/(\text{R1}+\text{R3})\right] \qquad \text{Eq. 6-37}$$

Also, the following relationships apply:

$$\text{R}_{\text{IN}} = \text{R1}+\text{R3} \qquad \text{Eq. 6-38}$$

$$\text{R2} = \text{R3}\left[1+\text{R3}/\text{R1}\right] \qquad \text{Eq. 6-39}$$

If R1 = R3, then R2 = 2 × R1. In this case, the R-2R network provides 6 dB step attenuation.

To determine the resistor values for a specific step attenuation and input resistance, use the formulas as follows:

$$K = 10^{\left[\text{Step Attenuation (dB)}/20\right]} \quad \text{Eq. 6-40}$$

where the step attenuation is entered as a negative number.

Then, the following equations complete the design:

$$R1 = R_{IN}\left(1 - K\right) \quad \text{Eq. 6-41}$$

$$R2 = R_{IN} \times K/\left(1 - K\right) \quad \text{Eq. 6-42}$$

$$R3 = K \times R_{IN} \quad \text{Eq. 6-43}$$

For example, to implement a resistor ladder with a −1.5 dB step attenuation and a 500 Ω input impedance: K = 0.8414, R1 = 79.3 Ω, R2 = 2653 Ω, and R3 = 420.7 Ω using the above equations.

The gain of the op amp is equal to 1 + R4/R5. The overall gain of the PGA is equal to the op amp gain minus the attenuation setting.

Finally, it is interesting to note that the AD60x-series of X-Amps discussed in the previous "Communications Amplifiers" section of this chapter uses the same basic approach described above. In the AD60x X-Amp series however, attenuation is continuously variable, because an interpolation circuit rather than a multiplexer is used to connect the individual taps of the network to the op amp input.

A Wideband In Amp

Some op amps with provisions for external offset trim can be used in unusually creative ways. In fact, if the two offset null inputs are considered as an additional differential signal input pair, this point becomes more clear. Although designed principally for adjustment of device V_{OS}, the null inputs can often be used for additional signals. An example is the wideband in amp of Gerstenhaber and Gianino (see Reference 13). In the circuit of Figure 6-167, the op amp used is the AD817. Designed for low distortion video circuits, it has a relatively high resistance between the input differential pair emitters, R_E, approximately 1 kΩ. It also has internal, large-value 8 kΩ resistors in series with the V_{OS} nulling terminals at Pins 1 and 8, labeled here as R_1.

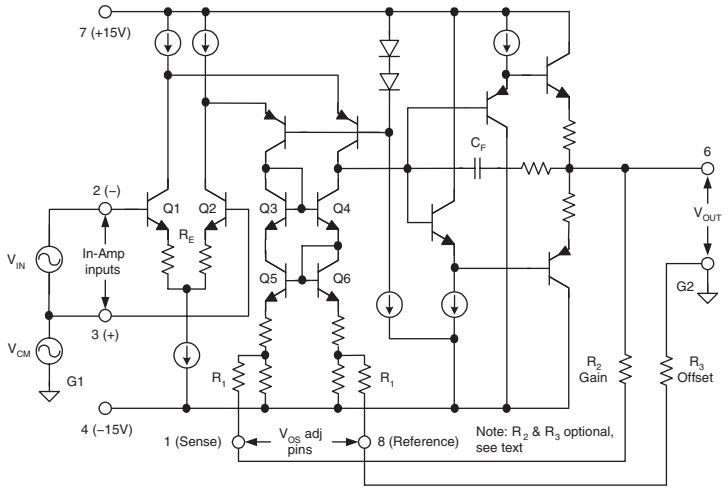


Figure 6-167: An AD817 wideband in amp configuration

Functioning here as an in amp, the AD817 is operated unconventionally. No feedback is used to inverting input Pin 2. Instead, the V_{IN} differential signal is applied between Pins 2 and 3, as noted. Typically there is also an associated CM noise, V_{CM}. Note that there must be a return path between the input ground G1 and output ground G2, to allow bias current flow (as with standard in amps). The input differential pair stage Q1 and Q2 produces an output signal current, driving quad-connected current mirror stage Q3, Q4, Q5, Q6. At the bottom of the current mirror is the balancing resistor network, functioning here as a signal current input. The connection from Pin 1 to the amplifier output closes a negative feedback loop, to the output at Pin 6. A balancing reference input is applied to Pin 8, either ground (as shown) or a variable offset voltage. Differential gain of the circuit, G, is:

$$G = V_{OUT}/V_{IN} = R_1/R_E \qquad \text{Eq. 6-44}$$

For the values noted, gain is about 8×, and bandwidth is 5 MHz. CMR is excellent, measuring more than 80 dB at 1 MHz. Optional trim resistors R_2 and R_3 are used to adjust gain via R_2, or, alternately, offset via R_3. For best CMR, the values should be the same.

Negative Resistance Buffer

There is often a requirement for driving a lower load impedance than a given op amp may be capable of meeting. This can be particularly true for precision op amps in general and, more specifically, with rail-rail output types. The latter class of op amps typically can have an output impedance on the order of several kΩ, which can limit load drive and lower open loop gain when driving low impedances. A straightforward way of addressing this problem is a unity gain buffer, which will work in almost all cases. But ordinary op amps can also be used for the buffer function. An interesting method is to use a second op amp as a negative resistance generator, to synthesize a negative resistance whose value is set equal to the load resistance. When this is carefully done the load disappears, as a parallel connection of R_L and $-R_L$ is infinite. Figure 6-168 illustrates this technique, in both basic and practical forms.

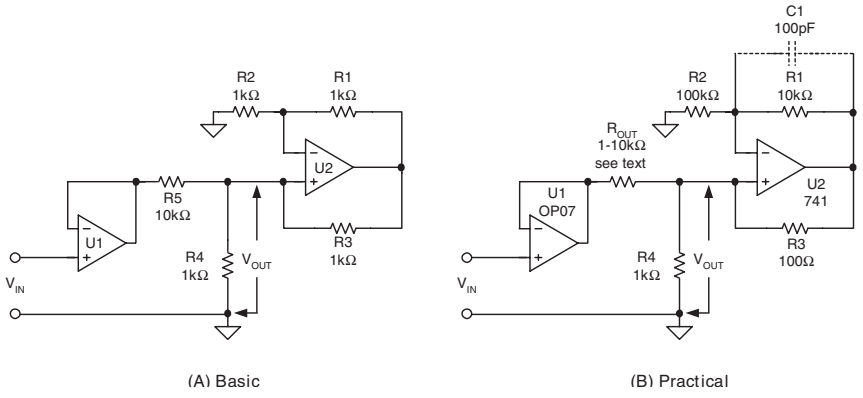


Figure 6-168: Negative resistance buffer circuits

A basic form of the circuit is shown in Figure 6-168A to illustrate the concept. Here op amp U1 is intended to drive load resistor R4, but would normally be prevented from doing so with high precision by the output resistance represented by R5. But, due to the connection of the U2 stage the voltage V_{OUT} is amplified by a factor of 1 + R1/R2. This amplified voltage is fed back to the V_{OUT} node by R3. With the R1–R4 values

scaled as shown, this produces a negative resistance of –R4 at the V_{OUT} node. Thus the driving amplifier U1 does not see the real resistance R4 loading, which can be confirmed by examining the (small) current in R5. If operation is not apparent, the circuit can be analyzed by viewing it as a balanced bridge, with ratios of R1/R2 matching R3/R4.

But the Figure 6-168A circuit isn't very efficient, as twice the load voltage must be developed for operation, and double the load current flows in U2. The same principles are employed in the more practical Figure 6-168B version, with the R1–R4 values rescaled to reduce power and to gain headroom in U2, *while maintaining the same ratios*. In a real circuit there is likely no need for R5, and U1 can drive the load directly. It does so taking full advantage of the precision characteristics of the U1 type. U2 can be almost any ordinary op amp capable of the load current required.

Cross-Coupled In Amps Provide Increased CMR

A primary in amp benefit is the ability to reject CM signals in the process of amplifying a low-level differential signal. While most in amps perform well below about 100 Hz, their CM rejection degrades rapidly with frequency. The circuit in Figure 6-169 is a composite in amp with much increased CMR vis-à-vis more conventional hookups (see Reference 15). It consists of three in amps, with unity-gain connected U1 and U2 cross-coupled at their inputs. In amp U3 amplifies the difference between V_{O1} and V_{O2}, while rejecting CM signals. The in amps are AD623s, but the scheme works with other devices.

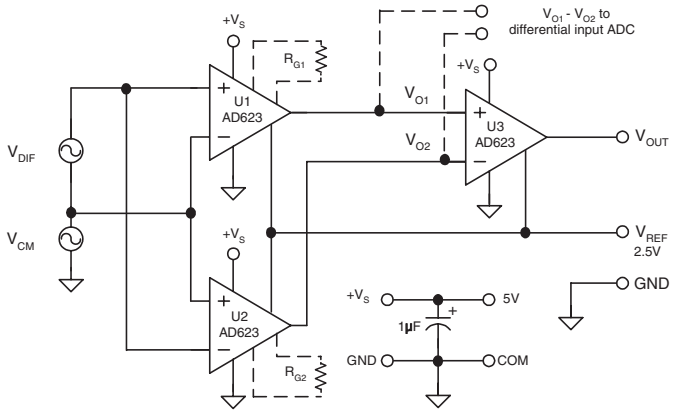


Figure 6-169: Two cross-coupled and similar in amp devices followed by a third provides much increased CMR with frequency

Because of the fact that U1 and U2 have CM responses that are correlated (by the nature of their design), their output CM errors due to V_{CM} will be similar. For U3, this CM error appears as a CM signal, and is rejected further. Meanwhile, the desired differential signal, equal to 2 V_{DIF} appears as $V_{O1} – V_{O2}$, and is amplified by U3 at unity gain. Overall gain is 2× as shown, but can be raised by a gain factor programmable by R_{G1} and R_{G2}. Note that due to the fact that the U1 and U2 CM errors correlate, their matching isn't necessary.

A big advantage of this scheme is the extended frequency range over which the composite in amp has good CMR. For example, at the gain of 2 as shown, CMR as measured at either V_{O1} or V_{O2} will be on the order of 60 dB or more at 10 kHz. At V_{OUT} however (the output of U3), the CMR is increased to about 85 dB, or more than 20 dB. The low frequency CMR corner of the composite in amp is about 6 kHz, as opposed to about 500 Hz as measured at either V_{O1} or V_{O2}. At higher gains, for example a gain of 100 (as set by R_{G1} and

R_{G2} = 2.05 kΩ), CMR increases to more than 110 dB at low frequencies, and a corner frequency of about 2 kHz is noted, while 10 kHz CMR is more than 100 dB. For these measurements $+V_S$ was 5 V, and the V_{REF} applied to all devices was 2.5 V.

Although the example shown is single-supply, it is also useful with dual-supply in amps. Another possible mode is to use V_{O1} and V_{O2} to drive a differential input ADC, which eliminates a need for in amp U3. ADC scaling can be matched via R_G, and the V_{REF} used.

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SECTION 6-6

Composite Amplifiers

Walt Jung

The term "composite op amp" can mean a variety of things. In the most general sense of the word, any additional circuitry at either the input or the output of an op amp could make the combination of what is termed a composite amplifier. This can be a valuable thing, as often such enhancements allow new performance levels to be realized from the resultant amplifier.

Some straightforward op amp performance enhancements of this type of have already been treated elsewhere in this book. For example, within the "Buffer Amplifiers" section of this chapter, as well as some of the specialized buffers in the "Audio" section of this chapter are found what could be termed composite op amps. In these examples, a standard output stage buffering design step is to utilize a unity-gain buffer, running on the same supplies as the op amp being buffered. So long as this buffer has sufficient bandwidth, this is an easy and straightforward step—insert the buffer between the op amp and the load, connect the feedback around the op amp plus buffer, and that's it.

A very useful means of increasing op amp performance can be obtained by blending the performance advantages of two ICs, or a standard op amp IC and discrete transistors. Such a combination is known as a *composite amplifier.* In special situations, a well-designed composite amp can often outperform standard op amps. The reason this is true is that the composite amplifier can be optimized for a unique and specialized performance, a combination that may not be available (or practical) in a standard op amp.

However, whenever an input (or output) circuit is added to an op amp that provides additional voltage gain, then the open-loop gain/phase characteristics of the composite op amp may need to be examined for possible stability problems. Note that this applies even when a unity-gain stable op amp is used within the composite, because the additional voltage gain raises the net open-loop gain of the combination. This will be made clearer by some circuit examples that follow.

In this section composite op amp circuits are described which fall into these categories:

- Multiple Op Amp Composite Amplifiers
- Voltage-Boosted Output Composite Amplifiers
- Gain-Boosted Input Composite Amplifiers
- A Nostalgia Composite Op Amp

These sections follow, with one or more circuit examples of each type.

Multiple Op Amp Composite Amplifiers

The simplest composite amplifier form utilizes two (or more) op amps, merged into a single equivalent composite. This is usually done for reasons of offset control, although in some instances it may be for increased gain capability, more output swing, and so forth.

Two-Op-Amp Composite Amplifier

The most flexible composite amplifier version combines two op amps in such a way that both signal inputs are still accessible to an application. A good example of this is the circuit shown in Figure 6-170 (see Reference 1).

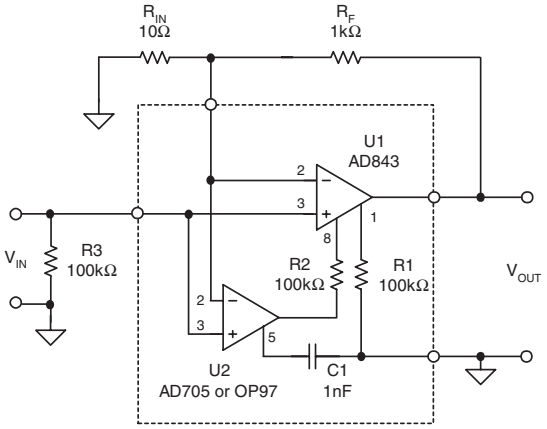

Figure 6-170: Low noise, low drift two-op-amp composite amplifier

In this circuit, U1 is a high speed FET input op amp, the AD843. While FET input devices are typically excellent for fast data acquisition applications, their offset and drift are often higher than the best bipolar op amps. By combining the fast AD843 with a low offset and low drift, super-β input device for U2, the best of both worlds is achieved. Offset and drift are reduced essentially to the maximum U2 specification levels—an offset of 60 μV, a drift of 0.6 μV/°C, and 100pA of bias current (for the OP97E). The composite op amp formed is the dotted box outline, and is applied as a 4-pin op amp.

Both the U1 and U2 op amps have inputs connected in parallel, and both amplify the signal. Device U1 drives the load and feedback loop directly. U2, however, drives the offset null input of U1, via a 100 kΩ resistor connected to Pin 8, R2. R1 provides a complementary resistance at the opposite offset input, Pin 1. C1 is used to over-compensate U2, at Pin 5. Note that the three just described pins are unique to the AD843, and either the AD705 or the OP97 devices. The U1/U2 signal inputs, output, and power supply pins are all standard, and the circuit operates on conventional ±15 V supplies.

The circuit as shown has a noninverting gain of 101×, as determined by R_F and R_{IN}. However, other applications are also possible, both inverting and noninverting in style. A detailed technical analysis of this circuit was presented in Reference 2.

Low Voltage Single-Supply to High Output Voltage Interface

There are numerous cases when an op amp designed for low (or single) supply voltage operation might need to be interfaced into a system operating on higher voltage and/or dual power supplies. An example would be the numerous low voltage chopper-stabilized op amps, which, without some means of easy interfacing, would simply not be available for use on high voltage supplies.

The circuit of Figure 6-171 shows how a low voltage, single-supply chopper-stabilized amplifier, the AD8551, can be used on a ±15 V supply system.

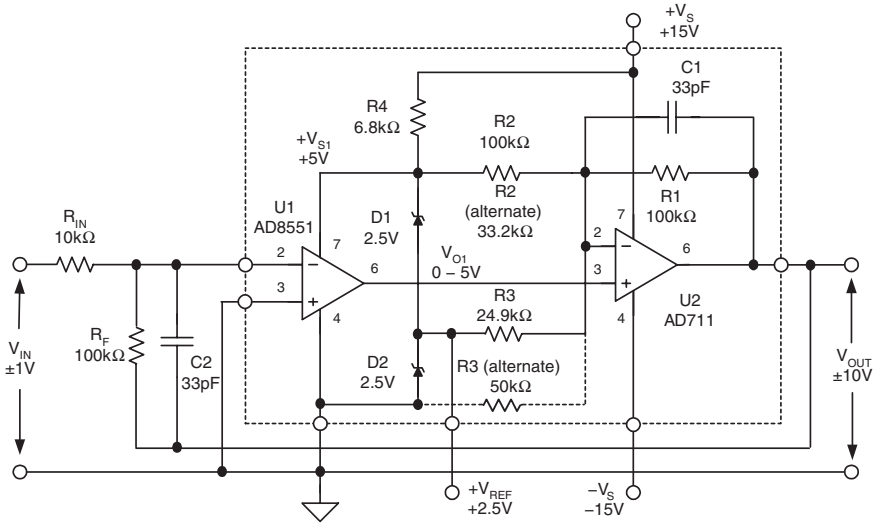

Figure 6-171: Chopper-stabilized 160 dB gain, low voltage single-supply to high output voltage composite amplifier

In this circuit, the U1 AD8551 operates as a precision input stage of the composite amplifier, working from a local 5 V supply generated from the main 15 V rail by reference diodes D1, D2. This satisfies the supply requirements for the U1 stage, with the R4 value selected to supply the required current.

To interface the 0 V to 5 V output swing of U1 to a ±10 V range, the U2 output stage operates as both a level shifter and a gain stage. A nominal gain of 6× is provided, with a dc offset providing the required level shifting. With the R1–R3 resistors and the 5 V supply used as a reference, the gain and level-shifting is accomplished. The gain of 6× translates back to a 0.833 V to 4.167 V positive output swing from U1, a range that even nonrail-rail output op amps can most likely accommodate.

A virtue of this circuit is that the output of U1 is not loaded, and thus it operates at its full characteristic gain. For the AD8551, this is typically 145dB. When the additional 15.6dB of the U2 stage is added, the net open-loop gain of the composite amplifier formed is more than 160 dB. Further, this high gain will be maintained for relatively lower impedance loads, by virtue of the fact that a standard emitter-follower type output stage is used within U2. So, the dc accuracy of this composite amplifier will be very high, and will also be well-maintained over a wide range of loads due to the buffering of stage U2.

The voltage-offsetting network as shown uses two 2.5 V reference diodes, which provides a 2.5 V V_{REF} output from D2. This is usually a handy asset to have in any 5 V supply device system. Alternately, a single 5 V reference diode can be used, with the alternate values and connections for R2 and R3 substituted.

To compensate the system for the additional voltage gain of U2, two feedback capacitors are used, C1 and C2. *Note that for anything other than this exact circuit, one or both of these capacitors may require adjustment.* This is best done by applying a low-level square wave to the input such that the final output is on the order of 100 mV p-p or less, and verifying that the output step response is well damped, with minimal overshoot.

C1 ensures stability for stage U2, and C2 provides overall bandwidth control for the main feedback loop. In general, the U2 amplifier should have more bandwidth than the U1 stage. However, the relative dc accuracy of U2 is not at all critical. The AD711 is shown as one possible choice, but many other types can also be used. While not shown for simplicity, conventional supply bypassing of the composite amplifier should be used.

System-wise, this composite amplifier behaves as a ±15 V powered op amp with an input CM range equal to the specification of the U1 device in use. Overall loop feedback is provided as with any conventional feedback stage, i.e., by R_F, R_{IN} and C2. The circuit is applied by treating the parts within the dotted box as a single op amp, with the external components adjusted to suit a given application. An application caveat is that saturation of U1–U2 should be avoided, due to the longer overload recovery. This can be addressed with a 11 V–12 V back-back clamping network across the feedback impedance.

Although the example hookup shown is a gain-of-10 inverter, other inverting configurations such as integrators and also noninverting stages are possible. The caveat here is that the CM range of U1 must be observed. However this is likely no handicap; as such an amplifier is most likely to be used with very high gain and low CM input voltages. It could for example be used as a 5 V-powered bridge amplifier with a ±10 V output range.

There are of course any number of other op amp input and output devices that will work within this general setup. A more general-purpose low voltage part for U1 would be the AD8541. Offset voltage will be higher, and gain less, vis-à-vis the AD8551. For optimum dynamic range and linearity, the biasing of the U1 stage output is centered within the total U1 supply voltage V_{S1}, which can be different than 5 V if needed. This feature is provided by R1–R3. The absolute values of these resistors aren't critical, but they should be maintained as to their ratio. They can be part of a common 100 kΩ array for simplicity.

Voltage-Boosted Output Composite Amplifiers

A number of schemes are useful towards boosting the output swing of standard op amps. This can be either to achieve greater swing (i.e., closer to the rails), or, to develop swings greater than normally possible with standard ICs, i.e., ≈40 V swings. In both cases it may also be desirable to increase load drive to 100mA or more.

Voltage Boosted, Rail-Rail Output Driver

A common requirement in modern system is the rail-rail capable op amp. But all op amps aren't designed with rail-rail outputs, so this may not be possible in all instances. Of course, it makes good sense to utilize standard off-the-shelf rail-rail IC op amps, whenever they meet the application requirements. Nevertheless, it is possible to add an output stage to a standard op amp device that may itself not be rail-rail in function. By using common-emitter (or common-source) discrete transistors external to the op amp, a rail-rail capability is realized. An example designed in this fashion is Figure 6-172.

Within this circuit Q1 and Q2 are the complementary buffer transistors that provide the rail-rail output swing. The circuit works as follows: Q1 is driven by the voltage drop across R4, and diode-connected Q3. This voltage is developed from the positive rail supply terminal of U1, so the quiescent bias current of Q1 will be related to the quiescent current of U1. Similarly, Q2 is driven from R3 and Q4, via the negative rail terminal of U1. The Q1–Q3 and Q2–Q4 pairs make up current mirrors, developing a quiescent bias current that flows in Q1-Q2. The U1 quiescent current is about 400 μA, and with the resistance values shown, the Q1-Q2 bias current is about 10 mA.

The output stage added to the U1 op amp adds additional voltage gain, and a current gain boost of 25 times, essentially the ratio of R4/R9 and R3/R10. Thus for a 100 mA output from Q1-Q2, U1 only supplies 4 mA. The swing across R2 is relatively low, allowing operation on low voltage supplies of ±6 V, or up to ±15 V.

The simulation data of Figure 6-173 illustrates some salient characteristics of the composite op amp while driving a load of 85 Ω. The open loop gain of the circuit is shown by the topmost, or composite gain curve, which indicates a low frequency gain of over 130 dB, crossing unity gain at about 630 kHz. The intermediate curve is the OP97 op amp gain characteristics. The difference between this and the upper curve is the added

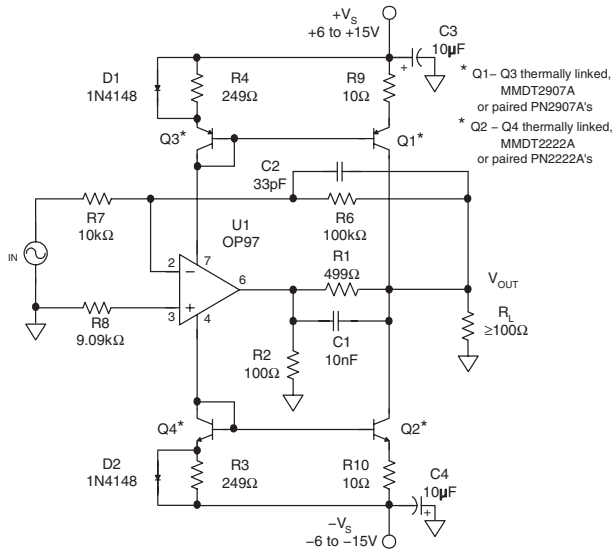

Figure 6-172: Voltage boosted rail-rail output composite op amp

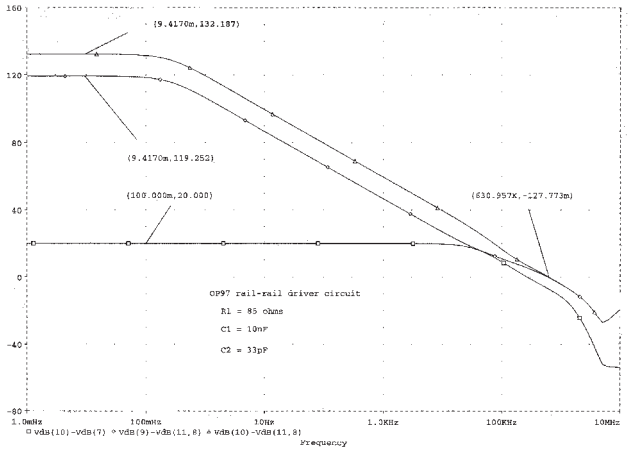

Figure 6-173: Gain (dB) versus frequency characteristics of Figure 6-172 composite op amp

gain, which is about 13 dB. The lowest curve indicates the closed-loop gain versus frequency characteristics of the composite op amp, which is 20 dB in this case, as set by R6 and R7 (as in a standard inverter).

There are a couple of critical points in setting up this circuit. Bandwidth can be controlled by C1 and C2. C1 reduces the added gain at high frequencies, which can be noticed from the composite gain curve, starting below 100 kHz. C2 reduces the closed-loop gain, starting about 50 kHz. For greater closed-loop gains, C2 may not be needed at all.

Bias control is achieved by the use of thermal coupling between the dual current mirror transistors. The easiest way to accomplish this is to use packaged dual types, either SOT-363 or SM-8 devices (see References

3 and 4). Alternately, TO92 equivalent PN2222A and PN2907A types can be used, with the two flat sides facing and clipped together.

The circuit as shown drives a 100Ω load to within 2 V of the rails, limited by the drop across R9 and R10. Current limiting is provided by a shunt silicon diode across R4 and R3, either with 1N4148 diodes, or diode-connected transistors. This limits peak output current to about ±60 mA. More output current is possible, by adding additional like devices in parallel to Q1 and Q2, with additional 10 Ω emitter resistors for each.

A point that should be noted about the booster circuit of Figure 6-172 is that *the biasing is dependent upon the quiescent current of the op amp*. Thus, this current must be stable within certain bounds, otherwise the idle current in Q1-Q2 could deviate—either too low (causing excess distortion), or too high, causing overheating. So, changing the U1 op amp isn't recommended, unless the biasing loop is re-analyzed for the new device.

Another point is that this type of circuit, which uses the power pins of the op amp for a signal path, *may not model at all in SPICE.* This is due to the fact that many op amp SPICE models do *not* model power supply currents so as to reflect output current—so be forewarned. However, the ADI OP97 model does happen to model these currents correctly, so the reader can easily replicate this circuit with the OP97 (as well as many other ADI models). Discussion of these models can be found in Chapter 7 of this book.

High Voltage Boosted Output Driver

With some subtle but key changes to the basic voltage-boosted composite amplifier of Figure 6-172, output swing can be extended even higher, more than double the standard ±10 V swing for ±15 V rails. A basic circuit that does this is shown in Figure 6-174.

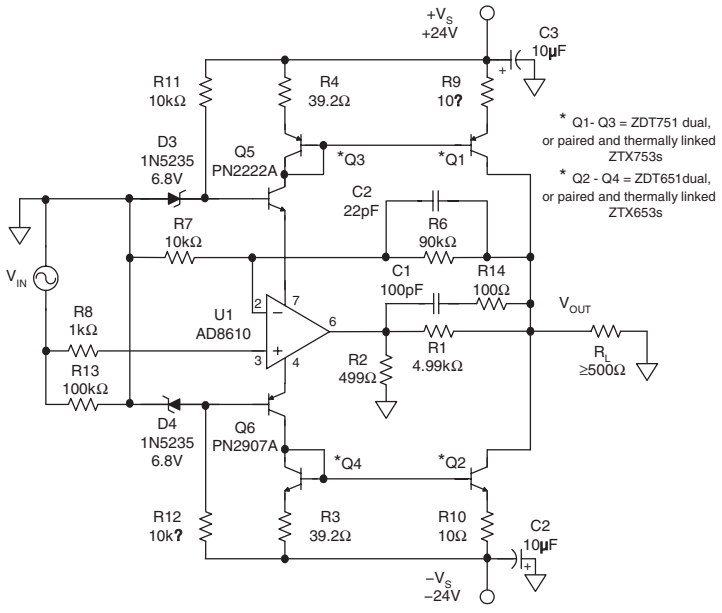

Figure 6-174: High voltage boosted rail-rail output composite op amp

This circuit can readily be recognized as being similar to the lower voltage counterpart of Figure 6-172. To achieve higher voltage capability, the U1 op amp is operated from a pair of combination level-shift/regulator transistors, Q5 and Q6. These are biased in turn from the D3 and D4 zener diodes at their bases, to ±6.8 V, respectively. The op amp rails are then simply ±6.2 V, while the main rails $+V_S$ and $-V_S$ can be virtually any potential, as will be ultimately limited by the Q1 and Q2 voltage/power ratings.

The op amp supply current passes through Q5 and Q6, driving the bases of Q1-Q2 as previously. To accommodate the higher ±24 V supplies, the standard 2222A and 2907A parts used in Figure 6-172 are replaced by higher voltage parts, the dual ZDT751 and ZDT651 (see Reference 4). Thermal matching is best maintained by using these dual types, but comparable TO92 pairs can also be used, for Q1-Q3, ZTX753s, and for Q2-Q4, ZTX653s (see References 5 and 6). In any case, a large area PCB land (i.e., 1–2 square inches) should be used to for the Q1-Q2 collectors for heat sinking purposes.

In this new circuit, an AD8610 op amp is used for U1, offering very low offset voltage, and higher speed. The quiescent current of the AD8610 is typically 2.5 mA. A 4/1 gain is used in this circuit, as established by R4/R9 and R3/R10. The idle current in Q1-Q2 is therefore about 10 mA, leading to a ≈240 mW dissipation each, on ±24 V supplies. This is low enough to not require a heat sink. However, the copper land area described above should be provided on the PCB around Q1-Q2 for heat sink purposes, tied electrically to their collectors. These measures, plus the active current limiting, help protect the output devices against shorts.

This circuit has a novel method of current limiting. As operated on ±6.2 V, the AD8610 will swing just over ±5 V. In driving R2 to this limit, ±10 mA of current will be delivered to the current mirrors, resulting in a maximum output current four times this, or ±40 mA. This is just about the dc safe-area limit of the Q1 and Q2 devices as used on ±24 V. For low impedance loads below 500 Ω, the maximum output voltage is a product of the 40mA limit and the load (for example 40 mA into 100 Ω yields 4 V peak). The maximum voltage swing into a 500 Ω load is then about ±20 V, again, as determined by the current limiting. Into higher impedance loads, the swing is proportionally greater, up until the point Q1-Q2 reach their saturation limits.

Although the circuit is quite versatile as shown, many other options are also possible. Other op amps can be used but, as noted before, the idle current should be taken into account. This is even more critical on higher voltage supplies, as it directly affects the power dissipated in Q1 and Q2.

For higher output currents from Q1-Q2, additional similar transistors can be paralleled, each with individual emitter resistors like R9 and R10. This will be practical for scaling up current by a factor of two to three times (assuming one additional package of the ZDT751 and ZDT651 types).

For ampere level current outputs, an additional current gain stage in the form of a complementary emitter follower can be added, driven from the Q1-Q2 collectors, with a 1:1 gain in the current mirror, and appropriate emitter follower biasing. With this step, the circuit will have been converted into a complete power amplifier. Details of this are left as an exercise for the reader. However, a good starting point might be the Alexander power amplifier topology (see Reference 7).

Gain-Boosted Input Composite Amplifiers

One of the most popular configurations used to enhance op amp performance is the gain-boosted input composite op amp. Here, a preamp gain stage is added ahead of a standard IC op amp, allowing greater open-loop gain, lower noise, and other performance enhancements. Another worthy improvement is the thermal isolation between the critical input stage, and the IC output stage that delivers the load current. The preamp can be a matched pair of bipolar transistors (NPN or PNP), or JFETs of either N or P types.

Prototype Bipolar Transistor Gain-Goosted Input Composite Amplifier

For illustration of the basics, a prototype example composite amplifier is the two-stage op amp of Figure 6-175. This circuit uses a matched NPN differential pair as a preamp stage ahead of U1, a standard AD711 type op amp. The preamp stage adds voltage gain to that of U1, making the overall gain higher, thus lowering gain-related errors.

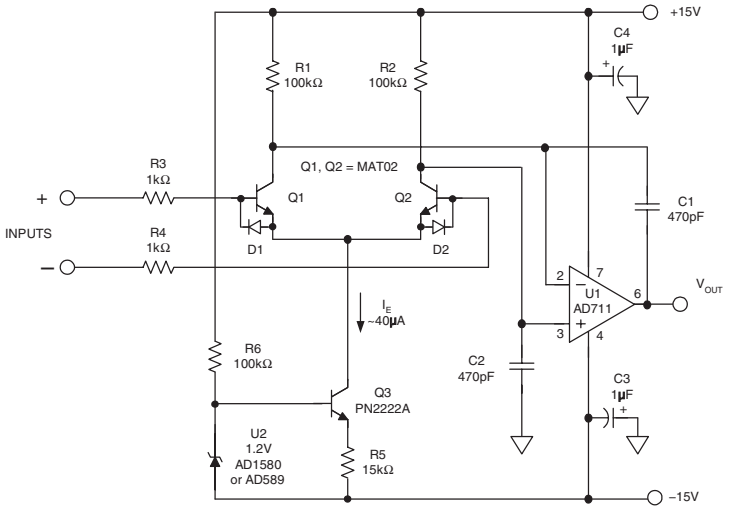

Figure 6-175: Bipolar transistor gain-boosted input composite op amp

Because of the added gain, the relative precision of the output op amp isn't very critical. It can be selected for sufficient output drive, slew rate and bandwidth. Within a given application the composite amplifier has overall feedback around both stages. Note—for this and following circuit examples, the op amp is *uncommitted* (i.e., external feedback).

In this example, a bipolar transistor differential pair, Q1-Q2 is loaded by a stable, matched load resistor pair, R1 and R2 (where R1 = R2 = R_L). The exact value of these resistors isn't overly critical, but they should match and track well. R1 and R2 are selected to drop 2 V–3 V at ½ I_E. For a 2 V drop, a suitable R_L is then:

$$R_L = \frac{4}{I_E} \qquad \text{Eq. 6-45}$$

Here, Q1 and Q2 operate at ≈20 µA each, so 100 kΩ values work for R1-R2. Note that in operation, *the second stage op amp must be capable of operating with input CM voltages of 2 V below the $+V_S$ rail*. This criterion is fine for many PFET input amplifiers such as the AD711, but others should be checked for CM input voltage compatibility. Note that similar preamp stages can also be built with PNP bipolars, or with JFETs, and some of these will be described later.

The dc or low frequency gain of the preamp stage, G1, can be quite high with bipolar transistors, since their g_m is high. G1 can be expressed as:

$$G1 = \frac{R_L I_E}{2V_T} \qquad \text{Eq. 6-46}$$

where V_T = KT/q (≈0.026 V at 27°C).

In this example, at 27°C, G1 is about 77 times (37.7 dB). Overall numeric gain is, of course, the product of the preamp gain and the U1 op amp gain. The minimum AD711 dc gain is 150,000, so the gain of the composite is more than 11.5 million (≥141 dB).

As the preamp stage provides additional gain, this extra gain must be phase controlled at high frequencies for unity-gain stability of the composite amplifier with applied feedback. In this circuit, compensation caps C1 and C2 provide this function with U1 connected as a differential integrator.

The unity gain frequency, Fu, can be expressed approximately as:

$$F_u \approx \frac{I_E}{4\pi C_C V_T} \qquad \text{Eq. 6-47}$$

where π is 3.14, C1 = C2 = C_C.

The performance of this composite op amp is illustrated in the gain and phase versus frequency simulation plot of Figure 6-176. The additional gain of the preamp raises the net dc gain to ≈149 dB, and the unity gain crossover frequency is shown to be ≈252 kHz, both of which generally agree with the estimated figures. The phase margin ϕ_m at 252 kHz is about 75 degrees, which is conservative. This op amp should be stable for all closed-loop gains down to unity (in fact, C1 and C2 could possibly be lowered).

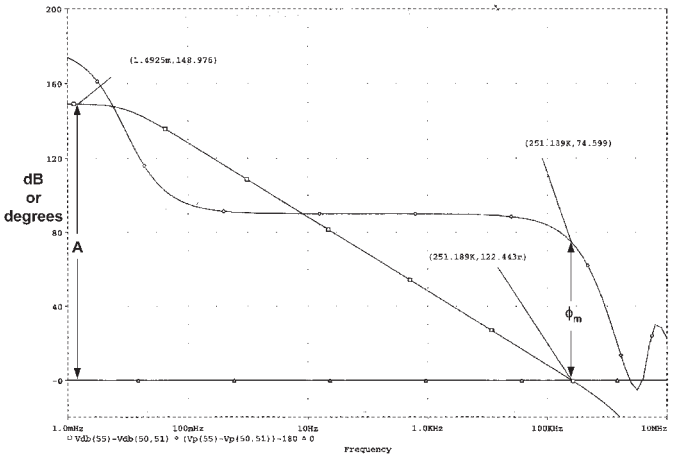

Figure 6-176: Gain/phase versus frequency for Figure 6-175 composite op amp

Slew rate of the composite op amp can be no higher than the specified SR of output stage U1. For cases where the effective SR is to be lower, it can be estimated as:

$$SR \approx \frac{I_E}{C_C} \qquad \text{Eq. 6-48}$$

Using Eqs. 6-47 and 6-48, the chosen values calculate a bandwidth of 260 kHz, and an SR of just under 0.1 V/µs. Actual bandwidths of 236 kHz–238 kHz were measured on 4 op amps for U1 (AD711, AD820, LM301A and LF356), while SR was +0.085 V/µs and –0.087 V/µs. As would be expected, the least bandwidth was measured with the lowest bandwidth U1 device, an LM301A. This demonstrates the relative insensitivity to U1 bandwidth.

With high gain input transistors, the bias current can be low. Generally, this will be:

$$I_B = \frac{I_E}{2H_{FE}} \qquad \text{Eq. 6-49}$$

Where I_B is the bias current of either Q1 or Q2, and H_{FE} is their dc gain. The MAT02 diodes protect against E-B reverse voltage, while the 1 kΩ resistors limit diode current.

Bias currents of 30 nA were measured with a MAT02 for Q1-Q2. Similar results can be obtained with high gain discrete transistors, such as 2N5210s. Offset voltage, however, is a different story. Monolithic duals such as the MAT02 will be far superior for offset voltage, with a V_{OS} specification of 50 µV. Nonmonolithic packaged duals will also function in this circuit, but with degradation of dc parameters versus a monolithic device such as the MAT02. As can be noted from the numbers quoted above, speed isn't a major asset of this amplifier. However, the dc performance is excellent, as noted, placing it in an OP177 class for gain.

The Q1-Q2 emitter current, I_E, can be established by a variety of means. The most general form is the U2, Q3, and R5 arrangement. This works for a wide range of inputs, and also offers relatively flat gain for a bipolar Q1-Q2 gain stage, since the PTAT current from Q3 compensates the temperature–related gain (Eq. 6-46). For those applications where the input of the amplifier is operating in an inverting mode, a more simple solution would be a resistor of 332 kΩ from the Q1-Q2 emitters to $-V_S$.

Of course, as a practical matter one wouldn't use the complex Figure 6-175 circuit, if an OP177 (or another standard device) could do the job more simply or inexpensively. Nevertheless, the above discussion illustrates how one can *tailor* a composite op amp's characteristics, to get exactly what is needed. The composite op amp circuit of Figure 6-175 could be used with a rail-rail output stage device for U1 (AD820), or with a very high current output stage (AD817, AD825), or any other performance niche not available from standard devices. Examples of these performance options follow.

Low Noise, Gain-Boosted Input Composite Amplifier

One of the more sound reasons for adding a preamp stage before a standard op amp is to lower the effective input noise, to a level lower than that of readily available IC devices. Figure 6-177 shows how this can be achieved within the same basic topology as described above for the Figure 6-175 prototype composite. As

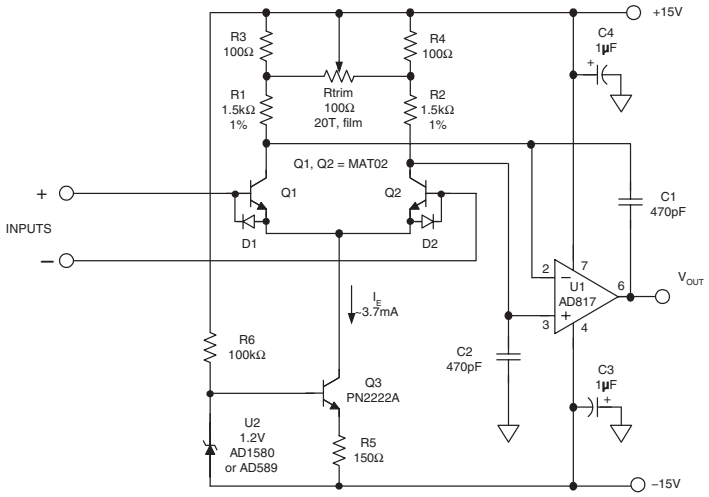

Figure 6-177: Low noise gain-boosted input composite op amp

will be noticed, this circuit is similar to the prototype, with the exception of the added offset trim network, a higher bias level for I_E, and a faster output op amp, U1. Rtrim nulls the offset for best dc accuracy in critical applications. If this isn't necessary, connect R1-R2 as in Figure 6-175.

By raising the current level of Q1-Q2 by roughly a factor of 100× compared to the prototype, the effective input noise of Q1-Q2 is dramatically lowered. At the operating current level of 3.7 mA, the MAT02 achieves an input voltage noise density $< 1\ \text{nV}/\sqrt{\text{Hz}}$ (see Reference 10). To eliminate their added noise, the series base resistors are dropped. Both bandwidth and SR are also improved in this circuit, since they are both proportional to I_E. The estimated bandwidth and SR for this circuit are 24 MHz and 7.9 V/µs, respectively. Measurements show about 21.2 MHz for bandwidth, and a SR close 7.6 V/µs. Both the actual bandwidth and SR are less than the AD817 specifications of 50 MHz and 350 V/µs. The circuit as shown is close to unity-gain stable, with 44° of phase margin at the unity gain frequency. Of course, very low noise amplifiers such as this will often be applied at some appreciably higher gain, for example 10, 100, or more. When this is the case, then C1 and C2 can be reduced, allowing greater bandwidth and SR.

An even lower noise op amp can be achieved simply by adding one or more low noise pairs parallel to Q1-Q2, and operating the combination at 6 mA of current. See References 11 and 12 for examples to achieve $0.5\ \text{nV}/\sqrt{\text{Hz}}$ or less noise.

JFET Transistor Gain-Boosted Input Composite Amplifier

The circuit of Figure 6-178 illustrates an alternative compensation method for composite op amps. This technique has the advantage of simplicity, but also the disadvantage of being conditionally stable. This technique goes back to the very earliest days of IC op amps, when discrete or monolithic matched FET pairs were used ahead of a standard IC op amp such as the 741, 709, and so forth. Further details are contained within References 13 and 14. The example here isn't offered as a practical example, inasmuch as so many superior IC FET op amps are available today. However, it does give insight into this type of compensation, which is applicable either to FET or bipolar input stages.

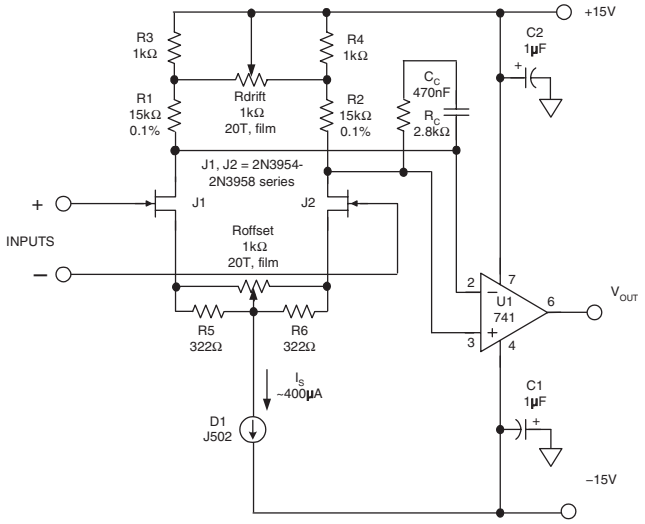

Figure 6-178: JFET transistor gain-boosted input composite amplifier

There are practical reasons why this type of FET input composite amplifier isn't used today. One is that to do it correctly involves many involved trims, another is that it requires a considerable number of parts. Dual FET devices don't come with sub-mV offsets, as do bipolars, so there is the need to trim out offset. Roffset does this, for J1-J2 V_{OS} up to 50 mV. For lowest drift, the drain currents should also be trimmed, via Rdrift.

N-channel JFET duals such as the 2N3954 and J401 series are specified for operation at a total I_S of 400 µA, or 200 µA/side. Their transconductance is much lower than a bipolar; for these conditions; it is typically ≈1400 µS. Therefore the gain of this preamp will typically be much lower than would a bipolar stage. With matched load resistors, gain is:

$$G1 = \frac{R_L \bullet g_{fs}}{2} \qquad \text{Eq. 6-50}$$

where g_{fs} is the specified JFET transconductance at $I_S/2$.

For the conditions shown, G1 works out to be 10.5 (20.4 dB). Note—if used, the Roffset network reduces gain somewhat, and Eq. 6-50 *doesn't* take this into account.

Compensation for this composite amplifier is via the RC network, R_C-C_C. This network reduces the gain of the preamp to unity above the zero frequency, which allows the aggregate open-loop response to then assume that of the U1 amplifier before the unity-gain crossover. It is chosen by setting R_C as:

$$R_C = \frac{4}{g_{fs}} \qquad \text{Eq. 6-51}$$

where g_{fs} is again the specified JFET transconductance at $I_S/2$.

In this case, R_C works out to be 2.8 kΩ. C_C is then chosen to provide a zero at some frequency that should be a very small fraction of the U1 op amp's unity gain frequency. The importance of this point will be made clearer by various open-loop response shapes.

It should be recalled that the classic open-loop response of an unconditionally stable op amp is a constant –6 dB/octave for gain, with an associated 90° phase shift. For such a device, any 1/β closed-loop response that intersects this open-loop response will be stable. For example, the 741 response (Δ), as so marked in Figure 6-179, is such a characteristic. But, as can also be noted from Figure 6-179, the gain/phase response of a composite op amp compensated as in Figure 6-178 just isn't a simple matter.

In the case of the added preamp stage and the R_C-C_C network compensation, the composite gain response (□) assumes *a multiple-slope response.* Associated with this gain response, note also that *the phase characteristic (*o*) varies radically with frequency*. In particular, the phase dip around 46 Hz signifies a frequency where a loop closure could be problematic, as the phase margin is only 40° at this point.

Faced with this type of open-loop gain/phase response, a designer needs to careful in crafting the closed-loop gain configuration. The first step is to decide what level of closed-loop gain is required by the application. Given that, an ideal 1/β curve can be drawn on a Bode diagram, to determine the rate-of-closure at the intersection. For optimum stability, it is desirable that this intersection occurs with a relative –6 dB/octave between the open-loop gain curve and an ideal 1/β curve. Note that if such a 1/β curve were drawn on Figure 6-179 at a 100 dB gain, it would intersect in a –12 dB/octave region. This is because C_C is 470 nF in this example, which places the phase dip at 46Hz, with a composite gain curve which, as noted, is dropping at a rate greater than 6dB/octave. So, with the proposed gain curve intersecting in this region, stability could be marginal.

On the other hand however, with the R_C-C_C "phase funnies" forced down to a low frequency that corresponds to very high closed-loop gains (i.e., ≈100 dB), the practical potential for instability is minimized.

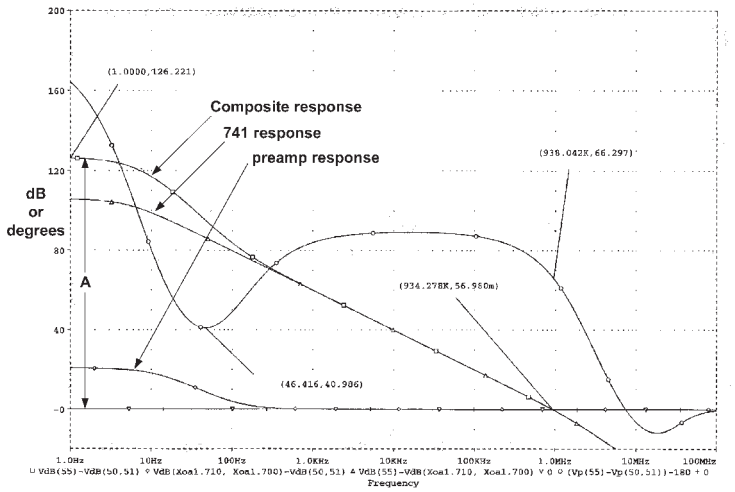

Figure 6-179: Gain/phase versus frequency for Figure 6-178 composite amplifier

Note also that it doesn't make good sense to build a 100 dB gain feedback amplifier based on limited open-loop gain such as Figure 6-179.

On the other hand, if C_C were smaller, this wouldn't necessarily be the case, because the associated phase dip would then move upward in frequency. This could wreak havoc with loop closures at more practical closed-loop gains. In contrast to this, with C_C sized as shown at 470 nF, the phase anomalies are confined to very low frequencies, yet the added dc gain of the preamp is still available. Loop closures at frequencies above ≈200 Hz (at closed-loop gains of 80 dB or less) see a high frequency composite response closely resembling the 741 (□ and Δ, respectively), and should thus be stable.

Watch out for the time domain response!

It should also be noted that there is a more subtle side effect related to the R_C-C_C method of compensation, as illustrated in Figure 6-178. Simply put, this is the fact that *the time domain response of the resulting composite amplifier will be marred, compared to that of a classic 6 dB/octave roll off* (see Reference 15).

So, wherever time domain response is critical, then the more conservative, unconditionally stable compensation method of Figure 6-175 should be used. A case in point using this method with a FET preamp is the next composite amplifier.

In summary, for the ac performance characteristics as a composite amplifier, the circuit of Figure 6-178 offers a gain raised higher that that of U1, or by about 20 dB (126 dB total) using the 741. At high frequencies, the overall gain bandwidth properties of this composite mimics the U1 amplifier, when the R_C-C_C time constant is relatively large.

Dc performance limitations

The dc input characteristics of this circuit will be those specified for the J1-J2 pair, with typical room temperature bias currents of 50 pA or less. Common-mode rejection will be limited by the J1-J2 specifications, and typically no more than about 80 dB, over a limited CM range. This could be improved by cascoding the J1-J2 pair, but again, given the availability of such FET-input IC amplifiers as the AD8610, this would be a questionable design for a precision FET amplifier. In Figure 6-178, the current source used for I_S is a simple

FET current limiter diode (see Reference 16). This offers simple, two-terminal operation, at a current level optimum for the J1-J2 pair.

Low Noise JFET Gain-Boosted Input Composite Amplifier

An alternative method of executing a JFET input gain-boosted composite is to operate the input differential pair into an output op amp stage that acts as a differential integrator (i.e., similar to the Figure 6-175 prototype, insofar as the compensation). The circuit of Figure 6-180 is such an example, one that is also optimized for low noise operation, medium speed, and higher output current.

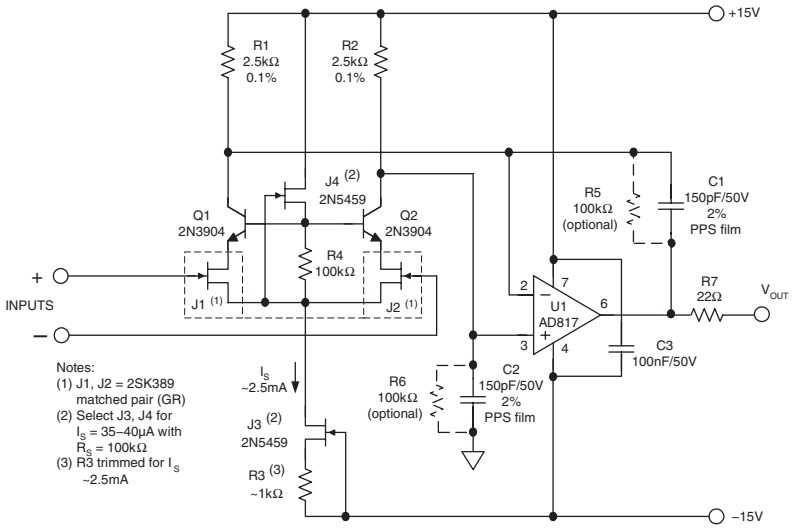

Figure 6-180: Low noise JFET gain-boosted input composite amplifier

The design uses a low noise JFET pair as the gain stage, the 2SK389 device (see Reference 17). Biased for drain currents of more than 2 mA, this device pair is capable of achieving an input voltage noise density of less than $1.5\ nV/\sqrt{Hz}$. The basic device is available in three I_{DSS} grades, GR (2.6–6.5 mA), BL (6–12 mA), and V (12–20 mA). The lowest noise will be found with use of the highest I_{DSS} parts, at the expense of course, of supply current. This design example can use any grade, by biasing J1-J2 for the GR parts (at an I_{DSS} of 2.5 mA). This still gives good noise performance for an FET-input amplifier (about $1.8\ nV/\sqrt{Hz}$), but at a still reasonable power supply drain.

A byproduct of the large geometry devices of this devices series is a relatively high capacitance. If this factor is not addressed, this large and nonlinear capacitance could cause distortion, for applications operating the circuit as a follower. To counteract this, the input stage of J1-J2 is cascoded, by the Q1-Q2 and J4 arrangement. This removes the major degradation of operation due to the J1-J2 capacitance, and it also stabilizes the dc operating points of J1-J2. From the output collectors of Q1-Q2 onward, the amplifier operates generally as the Figure 6-177 circuit previously described. An AD817 is used for U1, so as to take advantage of its wide bandwidth and high output current.

The unity-gain bandwidth of this circuit is about 15 MHz, but the open-loop gain is user selectable, by virtue of optional resistors R5 and R6. With these resistors connected, the composite amplifier open-loop

bandwidth is ≈10 kHz, and open-loop gain is about 63 dB. These attributes make it well-suited for audio applications, for example. Without R5 and R6, the open-loop gain is more like that of a conventional op amp, with a gain of more than 100 dB at low frequencies.

The open-loop response for R5 and R6 open is shown in Figure 6-181. In this simulation the load resistance was 600 Ω. As can be noted, the response is clean, without phase aberrations. Phase margin at the unity-gain crossover frequency is about 63°, and the low frequency gain is about 104 dB.

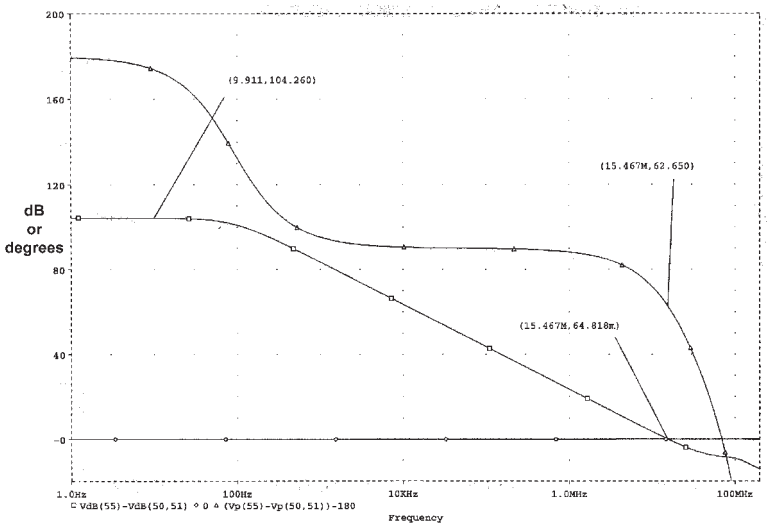

Figure 6-181: Gain/phase versus frequency for Figure 6-180 composite amplifier

Although this circuit does have some excellent ac characteristics, it should be noted that it is *not* a general-purpose op amp circuit. One reason for this is that the cascode input stage is a two-edged sword. While it reduces capacitance and improves distortion, it also limits the allowable CM input range. The positive swing headroom is limited by roughly the dc drop across R1 and R2, plus that of the cascode, or 3 V + 4.5 V. This means the most positive CM input should be less than about 5 V peak, or 3.5 V rms. This of course won't be a practical limitation for noninverting amplifiers with noise gains of 5× or more, or for low level preamps with high gains of 100× or 1000×.

As compensated in Figure 6-180, the composite op amp should be unity-gain stable. At closed-loop gains appreciably higher than about 5×, a reduction of C1-C2 can be considered, which will allow greater bandwidth and SR to be realized. Offset of the J1-J2 pair can be as high as 20 mV, so offset trim may be in order for dc-coupled applications. For lower noise, a high I_{DSS} grade for J1-J2 should be used, with I_S raised to 5 mA or more. R1-R2 will need to be lowered, and C1-C2 raised, in proportion.

"Nostalgia" Vacuum Tube Input/Output Composite Op Amp

In keeping with the theme of this book's History section, the final composite amplifier design for this section uses venerable vacuum tube devices, which formed the basis of the first ever op amps. Today however, designing a vacuum tube op amp has some advantages, vis-à-vis the early days—transistors didn't exist. Thus the nostalgia op amp shown in Figure 6-182 incorporates techniques of both today as well as yesteryear.

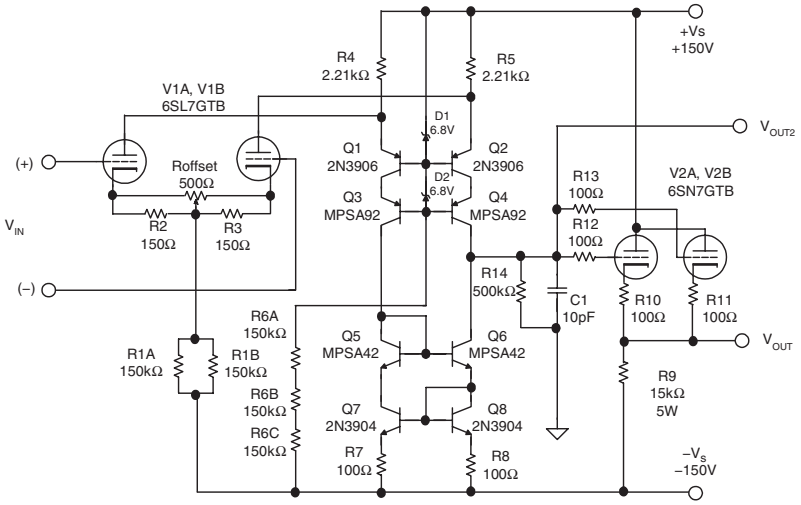

Figure 6-182: "Nostalgia" vacuum tube input/output composite op amp

Note that this particular circuit should be taken as a design exercise rather than a practical example. Yet, it was still a lot of fun to design using available SPICE models (see Reference 18). As such, it offers some insights not available to early op amp designers.

Here V1 is a dual triode input stage, using the high gain 6SL7 (or alternately, the close cousin 12AX7 miniature). It is operated here as a linear transconductance, long-tailed differential pair. Rather than using conventional plate loading, the output signal current from V1A–V1B is passed to a folded cascode stage Q1–Q4, which is loaded by a linear, high voltage current mirror, Q5–Q8. The transistors of the current mirror are also cascaded, both for higher output impedance as well as for required high voltage capability. A regulated 6.3 V heater supply for V1 is suggested, for highest stability.

Voltage gain of this one stage op amp is approximately equal to the V1A–V1B transconductance times the nodal impedance seen at V_{OUT2}. With R14 open, this impedance is very high, so gain can also be quite high (≈77 dB simulated). With R14 500 k, gain is about 53 dB. Open-loop bandwidth is established by the shunt capacitance at the high-Z node and R14, and measures about 7 MHz gain bandwidth in simulation. A 6SN7 dual cathode follower output stage for V2 allows up to 10 mA of load drive. Laboratory test results for this design are left as an exercise for the interested reader, and feedback is welcome.

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CHAPTER 7

Hardware and Housekeeping Techniques

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CHAPTER 7

Hardware and Housekeeping Techniques

Walt Kester, James Bryant, Walt Jung

This chapter, one of the longer of those within the book, deals with topics just as important as all of those basic circuits immediately surrounding the op amp, discussed earlier. The chapter deals with various and sundry circuit/system issues that fall under the guise of system *hardware and housekeeping techniques*. In this context, the hardware and housekeeping may be all those support items surrounding an op amp, excluding the op amp itself. This includes issues of passive components, printed circuit design, power supply systems, protection of op amp devices against overvoltage and thermal effects, EMI/RFI issues, and finally, simulation, breadboarding, and prototyping. Some of these topics aren't directly involved in the actual signal path of a design, but they are every bit as important as choosing the correct device and surrounding circuit values.

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SECTION 7-1

Passive Components

James Bryant, Walt Jung, Walt Kester

Introduction

When designing with op amps and other precision analog devices, it is critical that users avoid the pitfall of poor passive component choice. In fact, the wrong passive component can derail even the best op amp or data converter application. This section includes discussion of some basic traps of choosing passive components for op amp applications.

So, good money has been spent for a precision op amp or data converter, only to find that, when plugged into the board, the device doesn't meet spec. Perhaps the circuit suffers from drift, poor frequency response, and oscillations—or simply doesn't achieve expected accuracy. Well, before blaming the device, closely examine the passive components—including capacitors, resistors, potentiometers and, yes, even the printed circuit boards. In these areas, subtle effects of tolerance, temperature, parasitics, aging, and user assembly procedures can unwittingly sink a circuit. All too often these effects go unspecified (or underspecified) by passive component manufacturers.

In general, if using data converters having 12 bits or more of resolution, or op amps that cost more than a few dollars, pay very close attention to passive components. Consider the case of a 12-bit DAC, where ½ LSB corresponds to 0.012% of full scale, or only 122 ppm. A host of passive component phenomena can accumulate errors far exceeding this. But, buying the most expensive passive components won't necessarily solve the problems either. Often, a *correct* 25-cent capacitor yields a better-performing, more cost-effective design than a premium-grade part. With a few basics, understanding and analyzing passive components may prove rewarding, albeit not easy.

Capacitors

Most designers are generally familiar with the range of capacitors available. But the mechanisms by which both static and dynamic errors can occur in precision circuit designs using capacitors are sometimes easy to forget, because of the tremendous variety of types available. These include dielectrics of glass, aluminum foil, solid tantalum and tantalum foil, silver mica, ceramic, Teflon, and the film capacitors, including polyester, polycarbonate, polystyrene, and polypropylene types. In addition to the traditional leaded packages, many of these are now also offered in surface-mount styles.

Figure 7-1 is a workable model of a nonideal capacitor. The nominal capacitance, C, is shunted by a resistance R_P, which represents *insulation resistance* or leakage. A second resistance, R_S—*equivalent series resistance*, or ESR—appears in series with the capacitor and represents the resistance of the capacitor leads and plates.

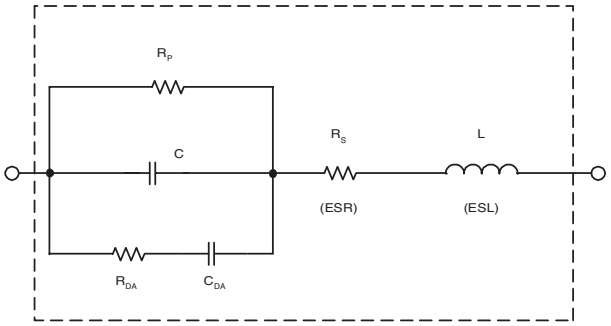


Figure 7-1: A nonideal capacitor equivalent circuit includes parasitic elements

Note that capacitor phenomena aren't that easy to separate out. The matching of phenomena and models is for convenience in explanation. Inductance, L—the *equivalent series inductance*, or ESL—models the inductance of the leads and plates. Finally, resistance R_{DA} and capacitance C_{DA} together form a simplified model of a phenomenon known as *dielectric absorption,* or DA. It can ruin fast and slow circuit dynamic performance. In a real capacitor, R_{DA} and C_{DA} extend to include multiple parallel sets. These parasitic RC elements can act to degrade timing circuits substantially, and the phenomenon is discussed further below.

Dielectric Absorption

Dielectric absorption, which is also known as "soakage" and sometimes as "dielectric hysteresis," is perhaps the least understood and potentially most damaging of various capacitor parasitic effects. Upon discharge, most capacitors are reluctant to give up all of their former charge, due to this memory consequence.

Figure 7-2 illustrates this effect. On the left of the diagram, after being charged to the source potential of V volts at time t_0, the capacitor is shorted by the switch S1 at time t_1, discharging it. At time t_2, the capacitor is then open-circuited; a residual voltage slowly builds up across its terminals and reaches a nearly constant value. This error voltage is due to DA, and is shown in the right figure, a time/voltage representation of the charge/discharge/recovery sequence. Note that the recovered voltage error is proportional to both the original charging voltage V, as well as the rated DA for the capacitor in use.

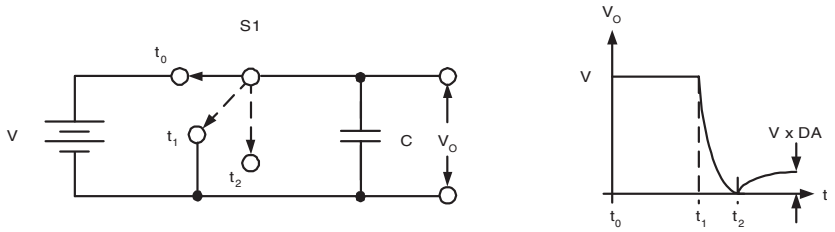


Figure 7-2: A residual open-circuit voltage after charge/discharge characterizes capacitor dielectric absorption

Standard techniques for specifying or measuring dielectric absorption are few and far between. Measured results are usually expressed as the percentage of the original charging voltage that reappears across the capacitor. Typically, the capacitor is charged for a long period, then shorted for a shorter established time. The capacitor is then allowed to recover for a specified period, and the residual voltage is then measured (see Reference 8 for details). While this explanation describes the basic phenomenon, it is important to note that real-world capacitors vary quite widely in their susceptibility to this error, with their rated DA ranging from well below to above 1%, the exact number being a function of the dielectric material used.

In practice, DA makes itself known in a variety of ways. Perhaps an integrator refuses to reset to zero, a voltage-to-frequency converter exhibits unexpected nonlinearity, or a sample-hold (SH) exhibits varying errors. This last manifestation can be particularly damaging in a data-acquisition system, where adjacent channels may be at voltages which differ by nearly full scale, as shown below.

Figure 7-3 illustrates the case of DA error in a simple SH. On the left, switches S1 and S2 represent an input multiplexer and SH switch, respectively. The multiplexer output voltage is V_X, and the sampled voltage held on C is V_Y, which is buffered by the op amp for presentation to an ADC. As can be noted by the timing diagram on the right, a DA error voltage, $\in$, appears in the hold mode, when the capacitor is effectively open circuit. This voltage is proportional to the difference of voltages V1 and V2, which, if at opposite extremes of the dynamic range, exacerbates the error. As a practical matter, the best solution for good performance in terms of DA in a SH is to use only the best capacitor.

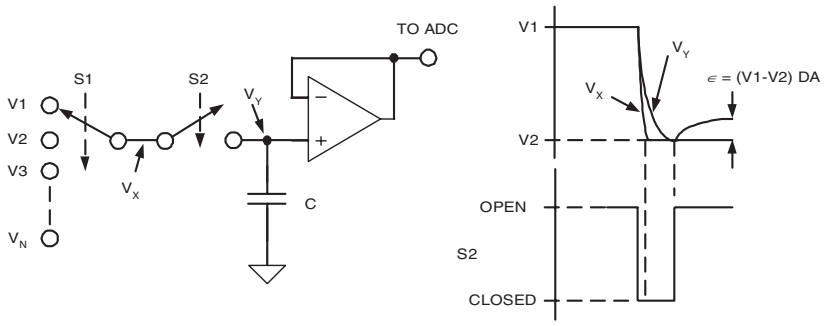


Figure 7-3: Dielectric absorption induces errors in SH applications

The DA phenomenon is a characteristic of the dielectric material itself, although inferior manufacturing processes or electrode materials can also affect it. DA is specified as a percentage of the charging voltage. It can range from a low of 0.02% for Teflon, polystyrene, and polypropylene capacitors, up to a high of 10% or more for some electrolytics. For some time frames, the DA of polystyrene can be as low as 0.002%.

Common high-K ceramics and polycarbonate capacitor types display typical DA on the order of 0.2%, it should be noted this corresponds to ½ LSB at only 8 bits. Silver mica, glass, and tantalum capacitors typically exhibit even larger DA, ranging from 1.0% to 5.0%, with those of polyester devices failing in the vicinity of 0.5%. As a rule, if the capacitor spec sheet doesn't specifically discuss DA *within your time frame and voltage range*, exercise caution. Another type with lower *specified* DA is likely a better choice.

DA can produce long tails in the transient response of fast-settling circuits, such as those found in high-pass active filters or ac amplifiers. In some devices used for such applications, Figure 7-1's R_{DA}-C_{DA} model of DA can have a time constant of milliseconds. Much longer time constants are also quite usual. In fact, several paralleled R_{DA}-C_{DA} circuit sections with a wide range of time constants can model some devices. In

fast-charge, fast-discharge applications, the behavior of the DA mechanism resembles "analog memory"; the capacitor in effect tries to remember its previous voltage.

The effects of DA can be compensated for in some designs if it is simple and easily characterized, and the user is willing to do custom tweaking. In an integrator, for instance, the output signal can be fed back through a suitable compensation network, tailored to cancel the circuit equivalent of the DA by placing a negative impedance effectively in parallel. Such compensation has been shown to improve SH circuit performance by factors of 10 or more (Reference 6).

Capacitor Parasitics and Dissipation Factor

In Figure 7-1, a capacitor's leakage resistance, R_P, the effective series resistance, R_S, and effective series inductance, L, act as parasitic elements, which can degrade an external circuit's performance. The effects of these elements are often lumped together and defined as a dissipation factor, or D_F.

A capacitor's leakage is the small current that flows through the dielectric when a voltage is applied. Although modeled as a simple insulation resistance (R_P) in parallel with the capacitor, the leakage actually is nonlinear with voltage. Manufacturers often specify leakage as a megohm-microfarad product, which describes the dielectric's self-discharge time constant, in seconds. It ranges from a low of 1 s or less for high-leakage capacitors, such as electrolytic devices, to the hundreds of seconds for ceramic capacitors. Glass devices exhibit self-discharge time-constants of 1,000 or more; but the best leakage performance is shown by Teflon and the film devices (polystyrene, polypropylene), with time constants exceeding 1,000,000 megohm-microfarads. For such a device, external leakage paths—created by surface contamination of the device's case or in the associated wiring or physical assembly—can overshadow the internal dielectric-related leakage.

Effective series inductance, ESL (Figure 7-1) arises from the inductance of the capacitor leads and plates which, particularly at the higher frequencies, can turn a capacitor's normally capacitive reactance into an inductive reactance. Its magnitude strongly depends on construction details within the capacitor. Tubular wrapped-foil devices display significantly more lead inductance than molded radial-lead configurations. Multilayer ceramic and film-type devices typically exhibit the lowest series inductance, while ordinary tantalum and aluminum electrolytics typically exhibit the highest. Consequently, standard electrolytic types, if used alone, usually prove insufficient for *high speed* local bypassing applications. Note however that there also are more specialized aluminum and tantalum electrolytics available, which may be suitable for higher speed uses. These are the types generally designed for use in switch-mode power supplies, which are covered more completely in a following section.

Manufacturers of capacitors often specify effective series impedance by means of impedance-versus-frequency plots. Not surprisingly, these curves show graphically a predominantly capacitive reactance at low frequencies, with rising impedance at higher frequencies because of the effect of series inductance.

Effective series resistance, ESR (resistor R_S of Figure 7-1), is made up of the resistance of the leads and plates. As noted, many manufacturers lump the effects of ESR, ESL, and leakage into a single parameter called *dissipation factor*, or DF. Dissipation factor measures the basic inefficiency of the capacitor. Manufacturers define it as the ratio of the energy lost to energy stored per cycle by the capacitor. The ratio of ESR to total capacitive reactance—at a specified frequency—approximates the dissipation factor, which turns out to be equivalent to the reciprocal of the figure of merit, Q. Stated as an approximation, $Q \approx 1/DF$ (with DF in numeric terms). For example, a DF of 0.1% is equivalent to a fraction of 0.001; thus the inverse in terms of Q would be 1000.

Dissipation factor often varies as a function of both temperature and frequency. Capacitors with mica and glass dielectrics generally have DF values from 0.03% to 1.0%. For ordinary ceramic devices, DF ranges from a low of 0.1% to as high as 2.5% at room temperature. And electrolytics usually exceed even this level. The film capacitors are the best as a group, with DFs of less than 0.1%. Stable-dielectric ceramics, notably the NP0 (also called COG) types, have DF specs comparable to films (more below).

Tolerance, Temperature, and Other Effects

In general, precision capacitors are expensive and—even then—not necessarily easy to buy. In fact, choice of capacitance is limited both by the range of available values and by tolerances. In terms of size, the better performing capacitors in the film families tend to be limited in practical terms to 10 μF or less (for dual reasons of size and expense). In terms of low value tolerance, ±1% is possible for NP0 ceramic and some film devices, but with possibly unacceptable delivery times. Many film capacitors can be made available with tolerances of less than ±1%, but on a special order basis only.

Most capacitors are sensitive to temperature variations. DF, DA, and capacitance value are all functions of temperature. For some capacitors, these parameters vary approximately linearly with temperature, in others they vary quite nonlinearly. Although it is usually not important for SH applications, an excessively large *temperature coefficient* (TC, measured in ppm/°C) can prove harmful to the performance of precision integrators, voltage-to-frequency converters, and oscillators. NP0 ceramic capacitors, with TCs as low as 30 ppm/°C, are the best for stability, with polystyrene and polypropylene next best, with TCs in the 100–200 ppm/°C range. On the other hand, when capacitance stability is important, one should stay away from types with TCs of more than a few hundred ppm/°C, or in fact any TC that is nonlinear.

A capacitor's maximum working temperature should also be considered, in light of the expected environment. Polystyrene capacitors, for instance, melt near 85°C, compared to Teflon's ability to survive temperatures up to 200°C.

Sensitivity of capacitance and DA to applied voltage, expressed as *voltage coefficient*, can also hurt capacitor performance within a circuit application. Although capacitor manufacturers don't always clearly specify voltage coefficients, the user should always consider the possible effects of such factors. For instance, when maximum voltages are applied, some high-K ceramic devices can experience a decrease in capacitance of 50% or more. This is an inherent distortion producer, making such types unsuitable for signal path filtering, for example, and better suited for supply bypassing. Interestingly, NP0 ceramics, the stable dielectric subset from the wide range of available ceramics, do offer good performance with respect to voltage coefficient.

Similarly, the capacitance, and dissipation factor of many types vary significantly with frequency, mainly as a result of a variation in dielectric constant. In this regard, the better dielectrics are polystyrene, polypropylene, and Teflon.

Assemble Critical Components Last

The designer's worries don't end with the design process. Some common printed circuit assembly techniques can prove ruinous to even the best designs. For instance, some commonly used cleaning solvents can infiltrate certain electrolytic capacitors—those with rubber end caps are particularly susceptible. Even worse, some of the film capacitors, polystyrene in particular, actually melt when contacted by some solvents. Rough handling of the leads can damage still other capacitors, creating random or even intermittent circuit problems. Etched-foil types are particularly delicate in this regard. To avoid these difficulties it may be advisable to mount especially critical components as the last step in the board assembly process—if possible.

Table 7-1
CAPACITOR COMPARISON CHART

TYPE	TYPICAL DA	ADVANTAGES	DISADVANTAGES
Polystyrene	0.001% to 0.02%	Inexpensive Low DA Good Stability (~120ppm/°C)	Damaged by Temperature >85°C Large High Inductance Vendors Limited
Polypropylene	0.001% to 0.02%	Inexpensive Low DA Stable (~200ppm/°C) Wide Range of Values	Damaged by Temperature >105°C Large High Inductance
Teflon	0.003% to 0.02%	Low DA Available Good Stability Operational Above 125°C Wide Range of Values	Expensive Large High Inductance
Polycarbonate	0.1%	Good Stability Low Cost Wide Temperature Range Wide Range of Values	Large DA Limits to 8-Bit Applications High Inductance
Polyester	0.3% to 0.5%	Moderate Stability Low Cost Wide Temperature Range Low Inductance (Stacked Film)	Large DA Limits to 8-Bit Applications High Inductance (Conventional)
NP0 Ceramic	<0.1%	Small Case Size Inexpensive, Many Vendors Good Stability (30ppm/°C) 1% Values Available Low Inductance (Chip)	DA Generally Low (May Not be Specified) Low Maximum Values (≤10nF)
Monolithic Ceramic (High K)	>0.2%	Low Inductance (Chip) Wide Range of Values	Poor Stability Poor DA High Voltage Coefficient
Mica	>0.003%	Low Loss at HF Low Inductance Good Stability 1% Values Available	Quite Large Low Maximum Values (≤10nF) Expensive
Aluminum Electrolytic	Very High	Large Values High Currents High Voltages Small Size	High Leakage Usually Polarized Poor Stability, Accuracy Inductive
Tantalum Electrolytic	Very High	Small Size Large Values Medium Inductance	High Leakage Usually Polarized Expensive Poor Stability, Accuracy

Table 7-1 summarizes selection criteria for various capacitor types, arranged roughly in order of decreasing DA performance. In a selection process, the general information of this table should be supplemented by consultation of current vendor's catalog information (see References at end of section).

Designers should also consider the natural failure mechanisms of capacitors. Metallized film devices, for instance, often self-heal. They initially fail due to conductive bridges that develop through small perforations in the dielectric film. But, the resulting fault currents can generate sufficient heat to destroy the bridge, thus returning the capacitor to normal operation (at a slightly lower capacitance). Of course, applications in high-impedance circuits may not develop sufficient current to clear the bridge, so the designer must be wary here.

Tantalum capacitors also exhibit a degree, of self-healing but, unlike film capacitors, the phenomenon depends on the temperature at the fault location rising slowly. Therefore, tantalum capacitors self-heal best in high impedance circuits which limit the surge in current through the capacitor's defect. Use caution therefore, when specifying tantalums for high-current applications.

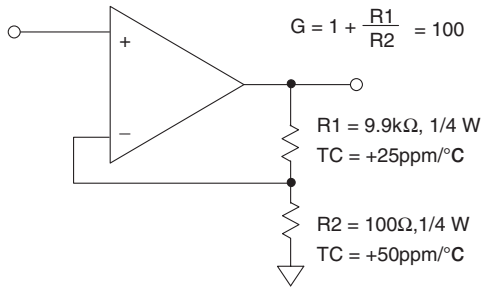
Electrolytic capacitor life often depends on the rate at which capacitor fluids seep through end caps. Epoxy end seals perform better than rubber seals, but an epoxy sealed capacitor can explode under severe reverse-voltage or overvoltage conditions. Finally, *all* polarized capacitors must be protected from exposure to voltages outside their specifications.

Resistors and Potentiometers

Designers have a broad range of resistor technologies to choose from, including carbon composition, carbon film, bulk metal, metal film, and both inductive and noninductive wire-wound types. As perhaps the most basic—and presumably most trouble-free—of components, resistors are often overlooked as error sources in high performance circuits.

An improperly selected resistor can subvert the accuracy of a 12-bit design by developing errors well in excess of 122 ppm (½ LSB).

Consider the simple circuit of Figure 7-4, showing a noninverting op amp where the 100× gain is set by R1 and R2. The TCs of these two resistors are a somewhat obvious source of error. Assume the op amp gain errors to be negligible, and that the resistors are perfectly matched to a 99/1 ratio at 25ºC. If, as noted, the resistor TCs differ by only 25 ppm/ºC, the gain of the amplifier changes by 250 ppm for a 10ºC temperature change. This is about a 1 LSB error in a 12-bit system, and a major disaster in a 16-bit system. Temperature changes, however, can limit the accuracy of the Figure 7-4 amplifier in several ways. In this circuit (as well as many op amp circuits with component-ratio defined gains), the *absolute* TC of the resistors is less



Temperature change of 10°C causes gain change of 250ppm

This is 1LSB in a 12-bit system and a disaster in a 16-bit system

Figure 7-4: Mismatched resistor TCs can induce temperature-related gain errors

important—*as long as they track one another in ratio*. But even so, some resistor types simply aren't suitable for precise work. For example, *carbon composition* units—with TCs of approximately 1,500 ppm/°C, won't work. Even if the TCs could be matched to an unlikely 1%, the resulting 15 ppm/°C differential still proves inadequate—an 8°C shift creates a 120 ppm error.

Many manufacturers offer metal film and bulk metal resistors, with absolute TCs ranging between ±1 and ±100 ppm/°C. Be aware, though; TCs can vary a great deal, particularly among discrete resistors from different batches. To avoid this problem, more expensive matched resistor pairs are offered by some manufacturers, with temperature coefficients that track one another to within 2 to 10 ppm/°C. Low priced thin-film networks have good relative performance and are widely used.

Suppose, as shown in Figure 7-5, R1 and R2 are ¼W resistors with identical 25 ppm/ºC TCs. Even when the TCs are identical, there can still be significant errors. When the signal input is zero, the resistors dissipate no heat. But, if it is 100 mV, there is 9.9 V across R1, which then dissipates 9.9 mW. It will experience a temperature rise of 1.24ºC (due to a 125ºC/W ¼W resistor thermal resistance). This 1.24ºC rise causes a resistance change of 31 ppm, and thus a corresponding gain change. But R2, with only 100mV across it, is only heated a negligible 0.0125ºC. The resulting 31 ppm net gain error represents a full-scale error of ½ LSB at 14 bits, and is a disaster for a 16-bit system.

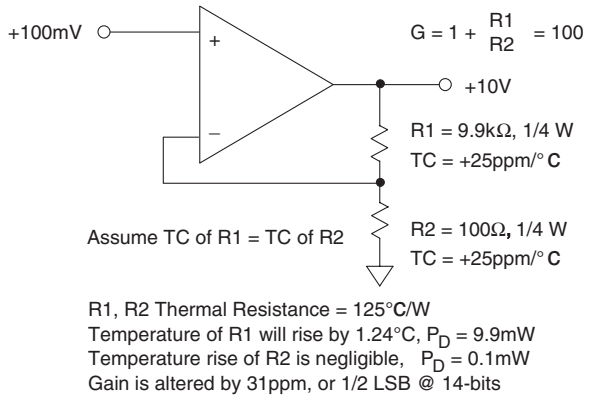


Figure 7-5: Uneven power dissipation between resistors with identical TCs can also introduce temperature-related gain errors

Even worse, the effects of this resistor self-heating also create easily calculable *nonlinearity errors*. In the Figure 7-5 example, with one-half the voltage input, the resulting self-heating error is only 15 ppm. In other words, the stage gain is not constant at ½ and full scale (nor is it so at other points), as long as uneven temperature shifts exist between the gain-determining resistors. This is by no means a worst-case example; physically smaller resistors would give worse results, due to higher associated thermal resistance.

These, and similar errors, are avoided by selecting critical resistors that are accurately matched for both value and TC, are well derated for power, and have tight thermal coupling between those resistors where matching is important. This is best achieved by using a resistor network on a single substrate—such a network may either be within an IC, or a separately packaged thin-film resistor network.

When the circuit resistances are very low (≤10 Ω), *interconnection stability* also becomes important. For example, while often overlooked as an error, the resistance TC of typical copper wire or printed circuit traces can add errors. The TC of copper is typically ~3,900 ppm/°C. Thus a precision 10 Ω, 10 ppm/°C

wirewound resistor with 0. 1 Ω of copper interconnect effectively becomes a 10.1 Ω resistor with a TC of nearly 50 ppm/°C.

One final consideration applies mainly to designs that see widely varying ambient temperatures: a phenomenon known as *temperature retrace* describes the change in resistance which occurs after a specified number of cycles of exposure to low and high ambients with constant internal dissipation. Temperature retrace can exceed 10 ppm/°C, even for some of the better thin-film components.

In summary, to design resistance-based circuits for minimum temperature-related errors, consider the points noted in Figure 7-6 (along with their cost).

- Closely match resistance TCs
- Use resistors with low absolute TCs
- Use resistors with low thermal resistance (higher power ratings, larger cases)
- Tightly couple matched resistors thermally (use standard common-substrate networks)
- For large ratios consider using stepped attenuators

Figure 7-6: A number of points are important towards minimizing temperature- related errors in resistors

Resistor Parasitics

Resistors can exhibit significant levels of parasitic inductance or capacitance, especially at high frequencies. Manufacturers often specify these parasitic effects as a reactance error, in % or ppm, based on the ratio of the difference between the impedance magnitude and the dc resistance, to the resistance, at one or more frequencies.

Wirewound resistors are especially susceptible to difficulties. Although resistor manufacturers offer wirewound components in either normal or noninductively wound form, even noninductively wound resistors create headaches for designers. These resistors still appear slightly inductive (of the order of 20 μH) for values below 10 kΩ. Above 10 kΩ the same style resistors actually exhibit 5 pF of shunt capacitance.

These parasitic effects can raise havoc in dynamic circuit applications. Of particular concern are applications using wirewound resistors with values both greater than 10 kΩ. Here it isn't uncommon to see peaking, or even oscillation. These effects become more evident at low kHz frequency ranges.

Even in low-frequency circuit applications, parasitic effects in wirewound resistors can create difficulties. Exponential settling to 1 ppm may take 20 time constants or more. The parasitic effects associated with wirewound resistors can significantly increase net circuit settling time to beyond the length of the basic time constants.

Unacceptable amounts of parasitic reactance are often found even in resistors that aren't wirewound. For instance, some metal-film types have significant interlead capacitance, which shows up at high frequencies. In contrast, when considering this end-end capacitance, carbon resistors do the best at high frequencies.

Thermoelectric Effects

Another more subtle problem with resistors is the *thermocouple effect*, also sometimes referred to as *thermal EMF*. Wherever there is a junction between two different metallic conductors, a thermoelectric voltage results. The thermocouple effect is widely used to measure temperature, as described in detail within Chapter 4. However, in any low level precision op amp circuit it is also a potential source of inaccuracy, since wherever two different conductors meet, a thermocouple is formed (whether we like it or not). In fact, in many cases, it can easily produce the dominant error within an otherwise precision circuit design.

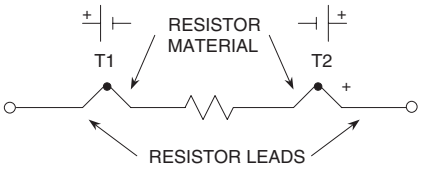
Parasitic thermocouples will cause errors when and if the various junctions forming the parasitic thermocouples are at different temperatures. With two junctions present on each side of the signal being processed within a circuit, by definition at least one thermocouple pair is formed. If the two junctions of this thermocouple pair are at different temperatures, there will be a net temperature dependent error voltage produced. Conversely, if the two junctions of a parasitic thermocouple pair are kept at an identical temperature, then the net error produced will be zero, as the voltages of the two thermocouples effectively will be canceled.

This is a critically important point, since in practice we cannot avoid connecting dissimilar metals together to build an electronic circuit. But, what we can do is carefully control temperature differentials across the circuit, so such that the undesired thermocouple errors cancel one another.

The effect of such parasitics is very hard to avoid. To understand this, consider a case of making connections *with copper wire only*. In this case, even a junction formed by different copper wire alloys can have a thermoelectric voltage that is a small fraction of 1 µV/ºC. And, taking things a step further, even such apparently benign components as resistors contain parasitic thermocouples, with potentially even stronger effects.

For example, consider the resistor model shown in Figure 7-7. The two connections between the resistor material and the leads form thermocouple junctions, T1 and T2. This thermocouple EMF can be as high as 400 µV/ºC for some carbon composition resistors, and as low as 0.05 µV/ºC for specially constructed resistors (see Reference 15). Ordinary metal film resistors (RN-types) are typically about 20 µV/ºC.

Note that these thermocouple effects are relatively unimportant for ac signals. Even for dc-only signals, they will nicely cancel one another if, as noted above, the entire resistor is at a uniform temperature. However, if there is significant power dissipation in a resistor, or if its orientation with respect to a heat source is nonsymmetrical, this can cause one of its ends to be warmer than the other, causing a net thermocouple



TYPICAL RESISTOR THERMOCOUPLE EMFs

- CARBON COMPOSITION ≈ 400 µV/ °C
- METAL FILM ≈ 20 µV/ °C
- EVENOHM OR MANGANIN WIREWOUND ≈ 2 µV/ °C
- RCD Components HP-Series ≈ 0.05 µV/ °C

Figure 7-7: Every resistor contains two thermocouples, formed between the leads and resistance element

error voltage. Using ordinary metal film resistors, an end-to-end temperature differential of 1ºC causes a thermocouple voltage of about 20 µV. This error level is quite significant compared to the offset voltage drift of a precision op amp like the OP177, and extremely significant when compared to chopper-stabilized op amps, with their drifts of <1 µV/°C.

Figure 7-8 shows how resistor orientation can make a difference in the net thermocouple voltage. In the left diagram, standing the resistor on end in order to conserve board space will invariably cause a temperature gradient across the resistor, especially if it is dissipating any significant power. In contrast, placing the resistor flat on the PC board as shown at the right will generally eliminate the gradient. An exception might occur, if there is end-to-end resistor airflow. For such cases, orienting the resistor axis perpendicular to the airflow will minimize this source of error, since this tends to force the resistor ends to the same temperature.

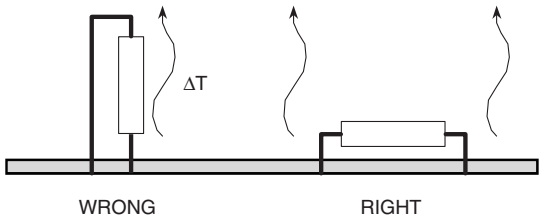


Figure 7-8: The effects of thermocouple EMFs generated by resistors can be minimized by orientation that normalizes the end temperatures

Note that this line of thinking should be extended to include orientation of resistors on a vertically mounted PC board. In such cases, natural convection air currents tend to flow upward across the board. Again, the resistor thermal axis should be perpendicular to convection, to minimize thermocouple effects. With tiny surface-mount resistors, the thermocouple effects can be less problematic, due to tighter thermal coupling between the resistor ends.

In general, designers should strive to avoid thermal gradients on or around critical circuit boards. Often this means thermally isolating components that dissipate significant amounts of power. Thermal turbulence created by large temperature gradients can also result in dynamic noise-like low frequency errors.

Voltage Sensitivity, Failure Mechanisms, and Aging

Resistors are also plagued by changes in value as a function of applied voltage. The deposited-oxide high megohm type components are especially sensitive, with voltage coefficients ranging from 1 ppm/V to more than 200 ppm/V. This is another reason to exercise caution in such precision applications as high-voltage dividers.

The normal failure mechanism of a resistor can also create circuit difficulties, if not carefully considered beforehand. For example, carbon-composition resistors fail safely, by turning into open circuits. Consequently, in some applications, these components can play a useful secondary role, as a fuse. Replacing such a resistor with a carbon-film type can possibly lead to trouble, since carbon-films can fail as short circuits. (Metal-film components usually fail as open circuits.)

All resistors tend to change slightly in value with age. Manufacturers specify long-term stability in terms of change—ppm/year. Values of 50 or 75 ppm/year are not uncommon among metal film resistors. For critical applications, metal-film devices should be burned in for at least one week at rated power. During burn-in, resistance values can shift by up to 100 or 200 ppm. Metal film resistors may need 4–5000 operational hours for full stabilization, especially if deprived of a burn-in period.

Resistor Excess Noise

Most designers have some familiarity with thermal, or Johnson, noise that occurs in resistors. But a less widely recognized secondary noise phenomenon is associated with resistors, and it is called *excess noise*. It can prove particularly troublesome in precision op amp and converter circuits, as it is evident only when current passes through a resistor.

To review briefly, thermal noise results from thermally induced random vibration of charge resistor carriers. Although the average current from the vibrations remains zero, instantaneous charge motions result in an instantaneous voltage across the terminals.

Excess noise on the other hand, occurs primarily when dc flows in a discontinuous medium—for example the conductive particles of a carbon composition resistor. The current flows unevenly through the compressed carbon granules, creating microscopic particle-to-particle "arcing." This phenomenon gives rise to a 1/f noise-power spectrum, in addition to the thermal noise spectrum. In other words, the excess spot noise voltage increases as the inverse square-root of frequency.

Excess noise often surprises the unwary designer. Resistor thermal noise and op amp input noise set the noise floor in typical op amp circuits. Only when voltages appear across input resistors and causes current to flow does the excess noise become a significant—and often dominant—factor. In general, carbon composition resistors generate the most excess noise. As the conductive medium becomes more uniform, excess noise becomes less significant. Carbon film resistors do better, with metal film, wirewound and bulk-metal-film resistors doing better yet.

Manufacturers specify excess noise in terms of a noise index—the number of microvolts of rms noise in the resistor in each decade of frequency per volt of dc drop across the resistor. The index can rise to 10 dB (3 microvolts per dc volt per decade of bandwidth) or more. Excess noise is most significant at low frequencies, while above 100 kHz thermal noise predominates.

Potentiometers

Trimming potentiometers (trimpots) can suffer from most of the phenomena that plague fixed resistors. In addition, users must also remain vigilant against some hazards unique to these components.

For instance, many trimpots aren't sealed, and can be severely damaged by board washing solvents, and even by excessive humidity. Vibration—or simply extensive use—can damage the resistive element and wiper terminations. Contact noise, TCs, parasitic effects, and limitations on adjustable range can all hamper trimpot circuit operation. Furthermore, the limited resolution of wirewound types and the hidden limits to resolution in cermet and plastic types (hysteresis, incompatible material TCs, slack) make obtaining and maintaining precise circuit settings anything but an "infinite resolution" process. Given this background, two rules are suggested for the potential trimpot user. Rule 1: Use infinite care and infinitesimal adjustment range to avoid infinite frustration when applying manual trimpots. Rule 2: *Consider the elimination of manual trimming potentiometers altogether, if possible.* A number of digitally addressable potentiometers (RDACs) are now available for direct application in similar circuit functions as classic trimpots (see Reference 17). There are also many low cost multi-channel voltage output DACs expressly designed for system voltage trimming.

Table 7-2 summarizes selection criteria for various fixed resistor types, both in discrete form and as part of networks. In a selection process, the general information of this table should be supplemented by consultation of current vendor's catalog information (see References at end of section).

Table 7-2
RESISTOR COMPARISON CHART

	TYPE	ADVANTAGES	DISADVANTAGES
DISCRETE	Carbon Composition	Lowest Cost High Power/Small Case Size Wide Range of Values	Poor Tolerance (5%) Poor Temperature Coefficient (1500 ppm/°C)
	Wirewound	Excellent Tolerance (0.01%) Excellent TC (1ppm/°C) High Power	Reactance is a Problem Large Case Size Most Expensive
	Metal Film	Good Tolerance (0.1%) Good TC (<1 to 100ppm/°C) Moderate Cost Wide Range of Values Low Voltage Coefficient	Must be Stabilized with Burn-In Low Power
	Bulk Metal or Metal Foil	Excellent Tolerance (to 0.005%) Excellent TC (to <1ppm/°C) Low Reactance Low Voltage Coefficient	Low Power Very Expensive
	High Megohm	Very High Values (10^8 to $10^{14}\Omega$) Only Choice for Some Circuits	High Voltage Coefficient (200ppm/V) Fragile Glass Case (Needs Special Handling) Expensive
NETWORKS	Thick Film	Low Cost High Power Laser-Trimmable Readily Available	Fair Matching (0.1%) Poor TC (>100ppm/°C) Poor Tracking TC (10ppm/°C)
	Thin Film	Good Matching (<0.01%) Good TC (<100ppm/°C) Good Tracking TC (2ppm/°C) Moderate Cost Laser-Trimmable Low Capacitance Suitable for Hybrid IC Substrate	Often Large Geometry Limited Values and Configurations

Inductance

Stray Inductance

All conductors are inductive, and at high frequencies, the inductance of even quite short pieces of wire or printed circuit traces may be important. The inductance of a straight wire of length L mm and circular cross-section with radius R mm in free space is given by the first equation shown in Figure 7-9.

The inductance of a strip conductor (an approximation to a PC track) of width W mm and thickness H mm in free space is also given by the second equation in Figure 7-9.

In real systems, these formulas both turn out to be approximate, but they do give some idea of the order of magnitude of inductance involved. They tell us that 1 cm of 0.5 mm o.d. wire has an inductance of 7.26 nH, and 1 cm of 0.25 mm PC track has an inductance of 9.59 nH. These figures are reasonably close to measured results.

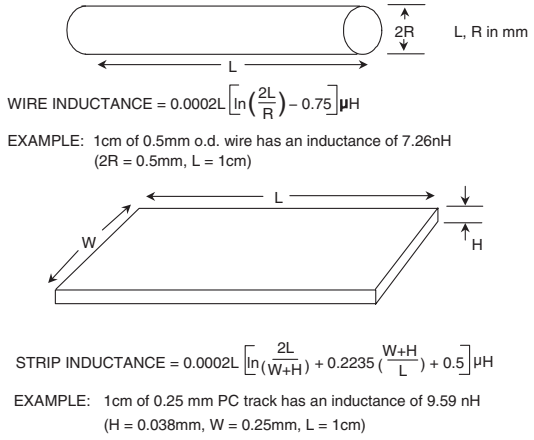


Figure 7-9: Wire and strip inductance calculations

At 10 MHz, an inductance of 7.26 nH has an impedance of 0.46 Ω, and so can give rise to 1% error in a 50 Ω system.

Mutual Inductance

Another consideration regarding inductance is the separation of outward and return currents. As we shall discuss in more detail later, Kirchoff's Law tells us that current flows in closed paths—there is always an outward and return path. The whole path forms a single-turn inductor.

This principle is illustrated by the contrasting signal trace routing arrangements of Figure 7-10. If the area enclosed within the turn is relatively large, as in the upper "nonideal" picture, the inductance (and hence the ac impedance) will also be large.

On the other hand, if the outward and return paths are closer together, as in the lower "improved" picture, the inductance will be much smaller.

Note that the nonideal signal routing case of Figure 7-10 has other drawbacks—the large area enclosed within the conductors produces extensive external magnetic fields, which may interact with other circuits,

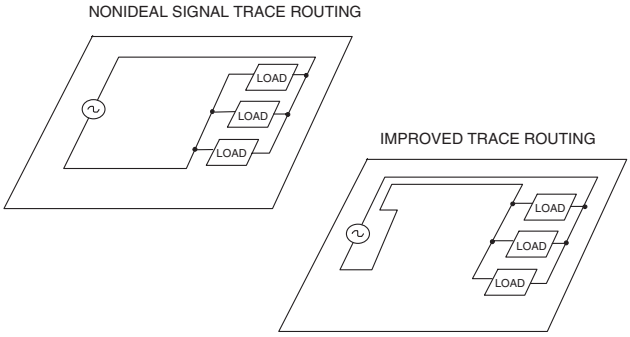
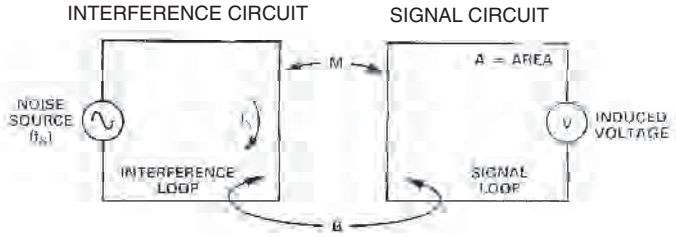


Figure 7-10: Nonideal and improved signal trace routing

causing unwanted coupling. Similarly, the large area is more vulnerable to interaction with external magnetic fields, which can induce unwanted signals in the loop.

The basic principle is illustrated in Figure 7-11, and is a common mechanism for the transfer of unwanted signals (noise) between two circuits.



M = MUTUAL INDUCTANCE
B = MAGNETIC REFLUX DENSITY
A = AREA OF SIGNAL LOOP
$\omega_N = 2\pi f_N$ = FREQUENCY OF NOISE SOURCE
V = INDUCED VOLTAGE = $\omega_N MIN = \omega AB$

Figure 7-11: Basic principles of inductive coupling

As with most other noise sources, as soon as we define the working principle, we can see ways of reducing the effect. In this case, reducing any or all of the terms in the equations in Figure 7-11 reduces the coupling. Reducing the frequency or amplitude of the current causing the interference may be impracticable, but it is frequently possible to reduce the mutual inductance between the interfering and interfered with circuits by reducing loop areas on one or both sides and, possibly, increasing the distance between them.

A layout solution is illustrated by Figure 7-12. Here two circuits, shown as Z1 and Z2, are minimized for coupling by keeping each of the loop areas as small as is practical.

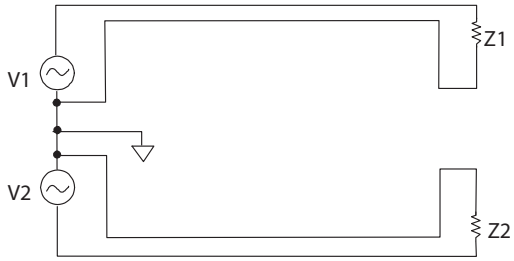


Figure 7-12: Proper signal routing and layout can reduce inductive coupling

As also illustrated in Figure 7-13, mutual inductance can be a problem in signals transmitted on cables. Mutual inductance is high in ribbon cables, especially when a single return is common to several signal circuits (top). Separate, dedicated signal and return lines for each signal circuit reduces the problem (middle). Using a cable with twisted pairs for each signal circuit as in the bottom picture is even better (but is more expensive and often unnecessary).

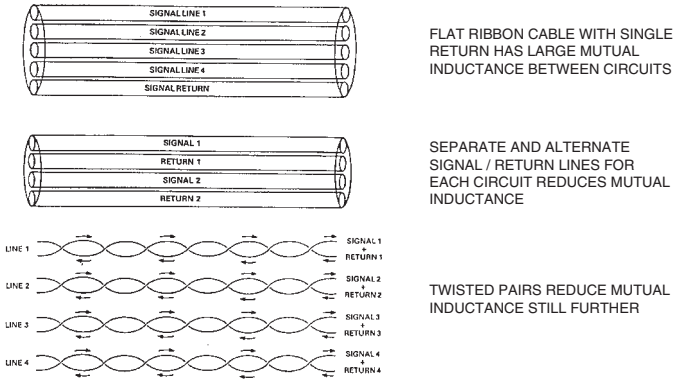


Figure 7-13: Mutual inductance and coupling within signal cabling

Shielding of magnetic fields to reduce mutual inductance is sometimes possible, but is by no means as easy as shielding an electric field with a Faraday shield (following section). HF magnetic fields are blocked by conductive material provided the skin depth in the conductor at the frequency to be screened is much less than the thickness of the conductor, and the screen has no holes (Faraday shields can tolerate small holes, magnetic screens cannot). LF and dc fields may be screened by a shield made of mu-metal sheet. Mu-metal is an alloy having very high permeability, but it is expensive, its magnetic properties are damaged by mechanical stress, and it will saturate if exposed to too high fields. Its use, therefore, should be avoided where possible.

Ringing

An inductor in series or parallel with a capacitor forms a resonant, or "tuned," circuit, whose key feature is that it shows marked change in impedance over a small range of frequency. Just how sharp the effect is depends on the relative Q of the tuned circuit. The effect is widely used to define the frequency response of narrow-band circuitry, but can also be a potential problem source.

If stray inductance and capacitance (which may or may not be stray) in a circuit should form a tuned circuit, that tuned circuit may be excited by signals in the circuit, and ring at its resonant frequency.

An example is shown in Figure 7-14, where the resonant circuit formed by an inductive power line and its decoupling capacitor may possibly be excited by fast pulse currents drawn by the powered IC.

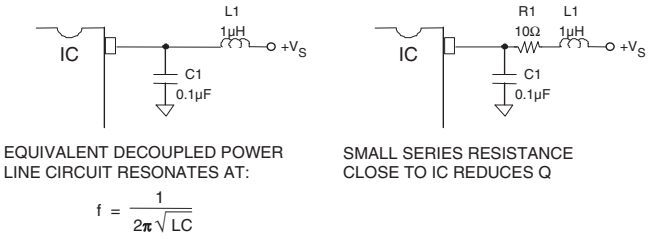


Figure 7-14: Resonant circuit formed by power line decoupling

While normal trace inductance and typical decoupling capacitances of 0.01 µF–0.1 µF will resonate well above a few MHz, an example 0.1 µF capacitor and 1 CH of inductance resonates at 500 kHz. Left unchecked, this could present a resonance problem, as shown in the left case. Should an undesired power line resonance be present, the effect may be minimized by lowering the Q of the inductance. This is most easily done by inserting a small resistance (~10 Ω) in the power line close to the IC, as shown in the right case.

Parasitic Effects in Inductors

Although inductance is one of the fundamental properties of an electronic circuit, inductors are far less common as components than are resistors and capacitors. As for precision components, they are even more rare. This is because they are harder to manufacture, less stable, and less physically robust than resistors and capacitors. It is relatively easy to manufacture stable precision inductors with inductances from nH to tens or hundreds of µH, but larger valued devices tend to be less stable, and large.

As we might expect in these circumstances, circuits are designed, where possible, to avoid the use of precision inductors. We find that stable precision inductors are relatively rarely used in precision analog circuitry, except in tuned circuits for high frequency narrow band applications. Of course, they are widely used in power filters, switching power supplies and other applications where lack of precision is unimportant (more on this in a following section).

The important features of inductors used in such applications are their current carrying and saturation characteristics, and their Q. If an inductor consists of a coil of wire with an air core, its inductance will essentially be unaffected by the current it is carrying. On the other hand, if it is wound on a core of a magnetic material (magnetic alloy or ferrite), its inductance will be nonlinear since, at high currents, the core will start to saturate. The effects of such saturation will reduce the efficiency of the circuitry employing the inductor and is liable to increase noise and harmonic generation.

As mentioned above, inductors and capacitors together form tuned circuits. Since all inductors will also have some stray capacity, all inductors will have a resonant frequency (which will normally be published on their data sheet), and should only be used as precision inductors at frequencies well below this.

Q or "Quality Factor"

The other characteristic of inductors is their Q (or "Quality Factor"), which is the ratio of the reactive impedance to the resistance, as indicated in Figure 7-15.

- $Q = 2\pi f\ L/R$
- The Q of an inductor or resonant circuit is a measure of the ratio of its reactance to its resistance.
- The resistance is the HF and NOT the DC value.
- The 3 dB bandwidth of a single tuned circuit is Fc/Q where Fc is the center frequency.

Figure 7-15: Inductor Q or quality factor

It is rarely possible to calculate the Q of an inductor from its dc resistance, since skin effect (and core losses if the inductor has a magnetic core) ensure that the Q of an inductor at high frequencies is always lower than that predicted from dc values.

Q is also a characteristic of tuned circuits (and of capacitors—but capacitors generally have such high Q values that it may be disregarded, in practice). The Q of a tuned circuit, which is generally very similar to the Q of its inductor (unless it is deliberately lowered by the use of an additional resistor), is a measure of its bandwidth around resonance. LC tuned circuits rarely have Q of much more than 100 (3 dB bandwidth of 1%), but ceramic resonators may have a Q of thousands, and quartz crystals tens of thousands.

Don't Overlook Anything

Remember, if a precision op amp or data-converter-based design does not meet specification, try not to overlook anything in trying to find the error sources. Analyze both active *and* passive components, trying to identify and challenge any assumptions or preconceived notions that may obscure to the facts. Take nothing for granted.

For example, when not tied down to prevent motion, cable conductors, moving within their surrounding dielectrics, can create significant static charge buildups that cause errors, especially when connected to high-impedance circuits. Rigid cables, or even costly low noise Teflon-insulated cables, are expensive alternative solutions.

As more and more high precision op amps become available, and system designs call for higher speed and increased accuracy, a thorough understanding of the error sources described in this section (as well those following) becomes more important.

Some additional discussions of passive components within a succeeding power supply filtering section complements this one. In addition, the very next section on PCB design issues also complements many points within this section. Similar comments apply to the section on EMI/RFI.

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SECTION 7-2

PCB Design Issues

James Bryant

Printed circuit boards (PCBs) are by far the most common method of assembling modern electronic circuits. Comprised of a sandwich of insulating layer (or layers) and one or more copper conductor patterns, they can introduce various forms of errors into a circuit, particularly if the circuit is operating at either high precision or high speed. PCBs then, act as "unseen" components, wherever they are used in precision circuit designs. Since designers don't always consider the PCB electrical characteristics as additional components of their circuit, overall performance can easily end up worse than predicted. This general topic, manifested in many forms, is the focus of this section.

PCB effects that are harmful to precision circuit performance include leakage resistances, spurious voltage drops in trace foils, vias, and ground planes, the influence of stray capacitance, dielectric absorption (DA), and the related "hook." In addition, the tendency of PCBs to absorb atmospheric moisture, *hygroscopicity,* means that changes in humidity often cause the contributions of some parasitic effects to vary from day to day.

In general, PCB effects can be divided into two broad categories—those that most noticeably affect the static or dc operation of the circuit, and those that most noticeably affect dynamic or ac circuit operation.

Another very broad area of PCB design is the topic of grounding. Grounding is a problem area in itself for all analog designs, and it can be said that implementing a PCB based circuit doesn't change that fact. Fortunately, certain principles of quality grounding, namely the use of ground planes, are intrinsic to the PCB environment. This factor is one of the more significant advantages to PCB-based analog designs, and appreciable discussion of this section is focused on this issue.

Some other aspects of grounding that must be managed include the control of spurious ground and signal return voltages that can degrade performance. These voltages can be due to external signal coupling, common currents, or simply excessive IR drops in ground conductors. Proper conductor routing and sizing, as well as differential signal handling and ground isolation techniques enables control of such parasitic voltages.

One final area of grounding to be discussed is grounding appropriate for a mixed-signal, analog/digital environment. Although this isn't the specific overall focus of the book, it is certainly true that interfacing with ADCs (or DACs) is a major task category of op amps, and thus it shouldn't be overlooked. Indeed, the single issue of quality grounding can drive the entire layout philosophy of a high performance mixed signal PCB design—as it well should.

Resistance of Conductors

Every engineer is familiar with resistors—little cylinders with wire or tab ends—although perhaps fewer are aware of their idiosyncrasies, as generally covered in section 7-1. But far too few engineers consider that all the wires and PCB traces with which their systems and circuits are assembled are also resistors. In higher precision systems, even these trace resistances and simple wire interconnections can have degrading effects. Copper is *not* a superconductor—and too many engineers appear to think it is.

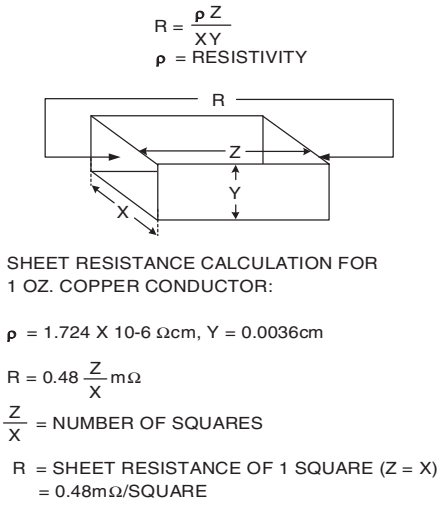


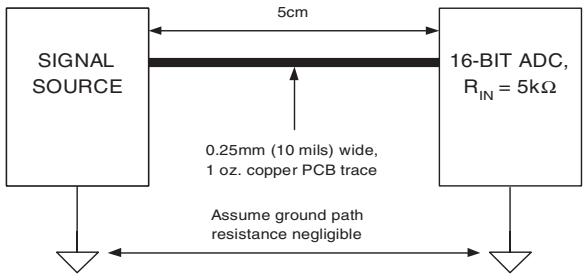
Figure 7-16: Calculation of sheet resistance and linear resistance for standard copper PCB conductors

Figure 7-16 illustrates a method of calculating the sheet resistance R of a copper square, given the length Z, the width X, and the thickness Y.

At 25°C the resistivity of pure copper is 1.724E-6 ohm cm. The thickness of standard 1 ounce PCB copper foil is 0.036 mm (0.0014"). Using the relations shown, the resistance of such a standard copper element is therefore 0.48 mΩ /square. One can readily calculate the resistance of a linear trace, by effectively "stacking" a series of such squares end-end, to make up the line's length. The line length is Z and the width is X, so the line resistance R is simply a product of Z/X and the resistance of a single square, as noted in the figure. For a given copper weight and trace width, a resistance/length calculation can be made. For example, the 0.25mm (10 mil) wide traces frequently used in PCB designs equates to a resistance/length of about 19 mΩ/cm (48 mΩ /inch), which is quite large. Moreover, the temperature coefficient of resistance for copper is about 0.4%/°C around room temperature. This is a factor that shouldn't be ignored, in particular within low impedance precision circuits, where the TC can shift the net impedance over temperature.

As shown in Figure 7-17, PCB trace resistance can be a serious error when conditions aren't favorable. Consider a 16-bit ADC with a 5 kΩ input resistance, driven through 5 cm of 0.25 mm wide 1 oz. PCB track between it and its signal source. The track resistance of nearly 0.1 Ω forms a divider with the 5 kΩ load, creating an error. The resulting voltage drop is a gain error of 0.1/5 k (~0.0019%), well over 1 LSB (0.0015% for 16 bits).

Figure 7-17: Ohm's law predicts >1 LSB of error due to drop in PCB conductor



So, when dealing with precision circuits, the point is made that even simple design items such as PCB trace resistance cannot be dealt with casually. There are various solutions that can address this issue, such as wider traces (which may take up excessive space), the use of heavier copper (which may be too expensive), or simply choosing a high impedance converter. But, the most important thing is to think it all through, avoiding any tendency to overlook items appearing innocuous on the surface.

Voltage Drop in Signal Leads—"Kelvin" Feedback

The gain error resulting from resistive voltage drop in PCB signal leads is important only with high precision and/or at high resolutions (Figure 7-17 example), or where large signal currents flow. Where load impedance is constant and resistive, adjusting overall system gain can compensate for the error. In other circumstances, it may often be removed by the use of "Kelvin" or "voltage sensing" feedback, as shown in Figure 7-18.

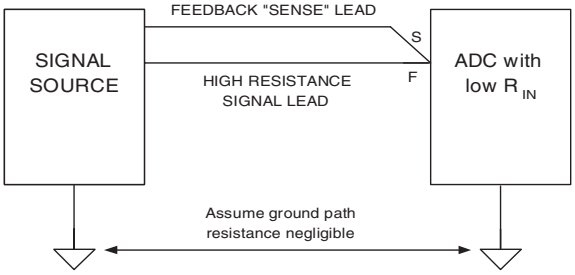


Figure 7-18: Use of a sense connection moves accuracy to the load point

In this modification to the case of Figure 7-17, a long resistive PCB trace is still used to drive the input of a high resolution ADC, with low input impedance. In this case, however, the voltage drop in the signal lead does *not* give rise to an error, as feedback is taken directly from the input pin of the ADC, and returned to the driving source. This scheme allows full accuracy to be achieved in the signal presented to the ADC, despite any voltage drop across the signal trace.

The use of separate force (F) and sense (S) connections at the load removes any errors resulting from voltage drops in the force lead but, of course, may be used only in systems where there is negative feedback. It is also impossible to use such an arrangement to drive two or more loads with equal accuracy, since feedback may only be taken from one point. Also, in this much-simplified system, errors in the common lead source/load path are ignored, the assumption being that ground path voltages are negligible. In many systems this may not necessarily be the case, and additional steps may be needed, as noted next.

Signal Return Currents

Kirchoff's Law tells us that at any point in a circuit the algebraic sum of the currents is zero. This tells us that all currents flow in circles and, particularly, that the return current must always be considered when analyzing a circuit, as is illustrated in Figure 7-19 (see References 7 and 8).

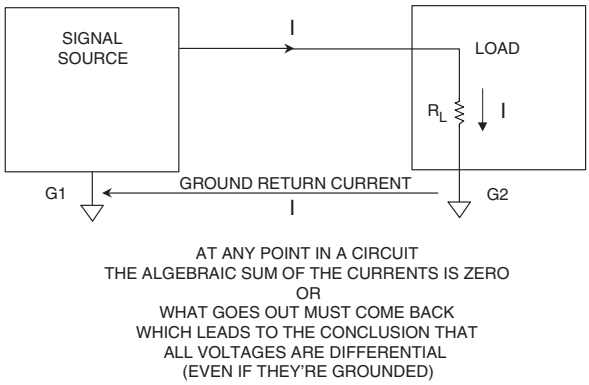


Figure 7-19: Kirchoff's law helps in analyzing voltage drops around a complete source/load coupled circuit

In dealing with grounding issues, common human tendencies provide some insight into how the correct thinking about the circuit can be helpful towards analysis. Most engineers readily consider the ground return current "I," *when they are considering a fully differential circuit*.

However, when considering the more usual circuit case, where a single-ended signal is referred to "ground," it is common to assume that all the points on the circuit diagram where ground symbols are found are at the same potential. Unfortunately, this happy circumstance just is not necessarily so.

This overly optimistic approach is illustrated in Figure 7-20, where, if it really should exist, "infinite ground conductivity" would lead to zero ground voltage difference between source ground G1 and load ground G2. Unfortunately this approach isn't a wise practice and, when dealing with high precision circuits, it can lead to disasters.

A more realistic approach to ground conductor integrity includes analysis of the impedance(s) involved, and careful attention to minimizing spurious noise voltages.

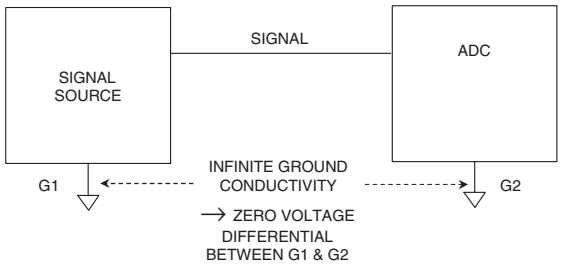


Figure 7-20: Unlike this optimistic diagram, it is unrealistic to assume infinite conductivity between source/load grounds in a real-world system

Ground Noise and Ground Loops

A more realistic model of a ground system is shown in Figure 7-21. The signal return current flows in the complex impedance existing between ground points G1 and G2 as shown, giving rise to a voltage drop ΔV in this path. But it is important to note that additional *external* currents, such as I_{EXT}, may also flow in this same path. It is critical to understand that such currents may generate uncorrelated noise voltages between G1 and G2 (dependent upon the current magnitude and relative ground impedance).

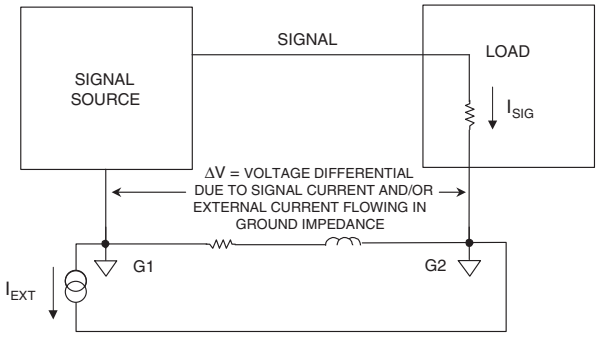


Figure 7-21: A more realistic source-to-load grounding system view includes consideration of the impedance between G1-G2, plus the effect of any nonsignal-related currents

Some portion of these undesired voltages may end up being seen at the signal's load end, and they can have the potential to corrupt the signal being transmitted.

It is evident, of course, that other currents can only flow in the ground impedance if there is a current path for them. In this case, severe problems can be caused by a high current circuit sharing an *unlooped* ground return with the signal source.

Figure 7-22 shows just such a common ground path, shared by the signal source and a high current circuit, which draws a large and varying current from its supply. This current flows in the common ground return, causing an error voltage ΔV to be developed.

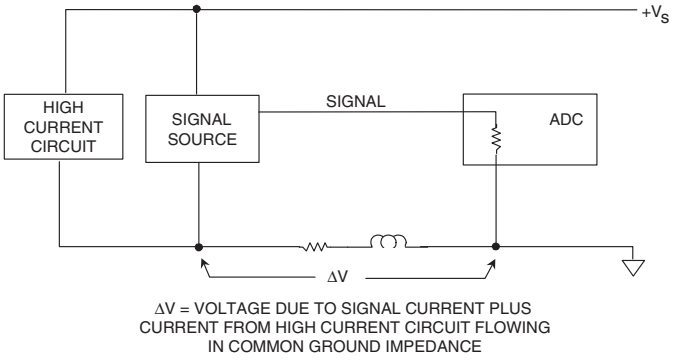


Figure 7-22: Any current flowing through a common ground impedance can cause errors

From Figure 7-23, it is also evident that if a ground network contains *loops,* or circular ground conductor patterns (with S1 closed), there is an even greater danger of it being vulnerable to EMFs induced by external magnetic fields. There is also a real danger of ground-current-related signals "escaping" from the high current areas, and causing noise in sensitive circuit regions elsewhere in the system.

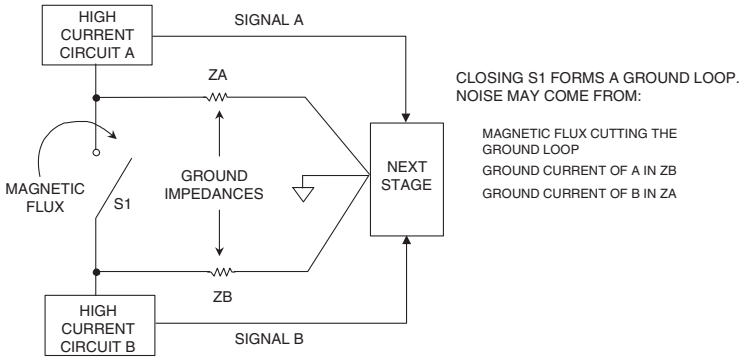


Figure 7-23: A ground loop

For these reasons ground loops are best avoided, by wiring all return paths within the circuit by separate paths back to a common point, i.e., the common ground point towards the mid-right of the diagram. This would be represented by the S1 open condition.

There are a number of possible ways of attacking the ground noise problem, apart from the presently impracticable one of using superconducting grounds. It is rare for any single method to be used to the exclusion of all others, and real systems generally contain a mixture. For descriptive purposes each approach is addressed separately.

Star Grounds

The "star" ground philosophy builds on the theory that there is one single ground point in a circuit to which all voltages are referred. This is known as the *star ground* point. It can be better understood by a visual analogy—the multiple conductors extending radially from the common schematic ground resemble a star. This can be appreciated by regarding Figure 7-23, considering many more ground returns from the common point. Note that the star point need not look like a star—it may be a point on a ground plane—but the key feature of the star ground system is that all voltages are measured with respect to a particular point in the ground network, not just to an undefined "ground" (i.e., wherever one can clip a probe). Figure 7-24 succinctly summarizes the philosophy.

- IF ALL SIGNAL VOLTAGES WITHIN A SYSTEM ARE MEASURED WITH RESPECT TO A SINGLE POINT, THAT POINT IS SAID TO BE THE SYSTEM STAR GROUND.

Figure 7-24: The star ground concept

This star grounding philosophy is reasonable theoretically, but can encounter practical difficulties. For example, if we design a star ground system, drawing out all signal paths to minimize signal interaction and the effects of high impedance signal or ground paths, we often find implementation problems. When the power

supplies are added to the circuit diagram, they either add unwanted ground paths or their supply currents flowing in the existing ground paths are sufficiently so large or noisy (or both), they can corrupt the signal transmission. This particular problem can often be avoided by having separate power supplies (and thus separate ground returns) for the various circuit portions. For example, separate analog and digital supplies with separate analog and digital grounds, joined at the star point, are common in mixed signal applications.

Separate Analog and Digital Grounds

As a fact of life, digital circuitry is noisy. Saturating logic draws large, fast current spikes from its supply during switching. However, logic stages, with hundreds of millivolts (or more) of noise immunity, usually have little need for high levels of supply decoupling. On the other hand, analog circuitry is quite vulnerable to noise on both power supply rails and grounds. So, it is very sensible to separate analog and digital circuitry, to prevent digital noise from corrupting analog performance. Such separation involves separation of both ground returns *and* power rails, which is inconvenient in a mixed-signal system. Nevertheless, if a mixed-signal system is to deliver full performance capability, it is often essential to have separate analog and digital grounds, and separate power supplies. The fact that some analog circuitry will "operate" (i.e., function) from a single 5 V supply does *not* mean that it may safely be operated from the same noisy 5 V supply as the microprocessor and dynamic RAM, the electric fan, and the solenoid jackhammer. What is required is that the analog portion *operate with full performance from such a low voltage supply*, not just be functional. This distinction will by necessity require quite careful attention to both the supply rails and the ground interfacing.

Figures 7-25 and 7-26 summarize some analog and digital power supply and grounding concepts which are useful to bear in mind as systems are designed.

Figure 7-25: Some power supply and ground noise concepts appropriate for mixed-signal systems

- DIGITAL CIRCUITRY IS *NOISY*
- ANALOG CIRCUITRY IS *QUIET*
- CIRCUIT NOISE FROM DIGITAL CIRCUITRY CARRIED BY POWER AND GROUND LEADS CAN CORRUPT PRECISION ANALOG CIRCUITRY
- IT IS ADVISABLE TO SEPARATE THE POWER AND GROUND OF THE DIGITAL AND ANALOG PARTS OF A SYSTEM
- ANALOG AND DIGITAL GROUNDS MUST BE JOINED AT ONE POINT

Figure 7-26: Treatment of analog and digital grounds with data converters of mixed-signal systems

- MONOLITHIC AND HYBRID ADCS FREQUENTLY HAVE SEPARATE *AGND* AND *DGND* PINS, WHICH MUST BE JOINED TOGETHER AT THE DEVICE.
- THIS ISN'T DONE TO BE DIFFICULT, BUT BECAUSE BONDWIRE VOLTAGE DROPS ARE TOO LARGE TO ALLOW INTERNAL CONNECTION.
- THE BEST SOLUTION TO THE GROUNDING PROBLEM ARISING FROM THIS REQUIREMENT IS TO CONNECT BOTH PINS TO SYSTEM "ANALOG GROUND."
- IT IS LIKELY THAT NEITHER THE DIGITAL NOISE SO INTRODUCED IN THE SYSTEM *AGND*, NOR THE SLIGHT LOSS OF DIGITAL NOISE IMMUNITY WILL SERIOUSLY AFFECT THE SYSTEM PERFORMANCE.

Note that analog and digital ground in a system must be joined at some point, to allow signals to be referred to a common potential. This star point, or analog/digital common point, is chosen so that it does not introduce digital currents into the ground of the analog part of the system—it is often convenient to make the connection at the power supplies.

Note also that many ADCs and DACs have separate *analog ground* (AGND) and *digital ground* (DGND) pins. On the device data sheets, users are often advised to connect these pins together at the package. This seems to conflict with the advice to connect analog and digital ground at the power supplies, and, in systems with more than one converter, with the advice to join the analog and digital ground at a single point.

There is, in fact, no conflict. The labels "analog ground" and "digital ground" on these pins refer to the parts of the converter to which the pins are connected, and not to the system grounds to which they must go. For example, with an ADC, generally these two pins should be joined together and to the *analog* ground of the system. It is not possible to join the two pins within the IC package, because the analog part of the converter cannot tolerate the voltage drop resulting from the digital current flowing in the bond wire to the chip. But they can be so tied, *externally*.

Figure 7-27 illustrates this concept of ground connections for an ADC. If these pins are connected in this way, the digital noise immunity of the converter is diminished somewhat by the amount of common-mode noise between the digital and analog system grounds. However, since digital noise immunity is of the order of hundreds or thousands of millivolts, this factor is unlikely to be important.

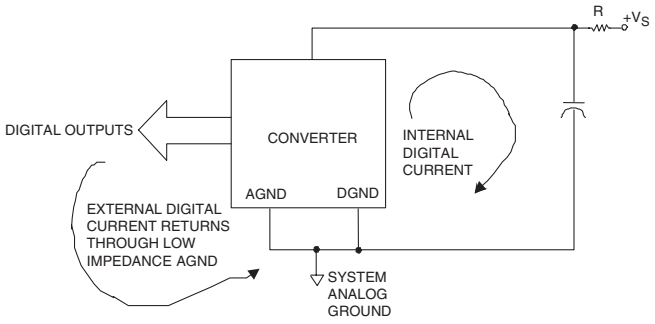


Figure 7-27: Analog (AGND) and digital ground (DGND) pins of a data converter should be returned to system analog ground

The analog noise immunity is diminished only by the external digital currents of the converter itself flowing in the analog ground. These currents should be kept quite small, and this can be minimized by ensuring that the converter outputs don't see heavy loads. A good solution towards this is to use a low input current buffer at the ADC output, such as a CMOS buffer-register IC.

If the logic supply to the converter is isolated with a small resistance and decoupled to analog ground with a local 0.1 μF capacitor, all the fast-edge digital currents of the converter will return to ground through the capacitor, and will not appear in the external ground circuit. If the analog ground impedance is maintained low, as it should be for adequate analog performance, additional noise due to the external digital ground current should rarely present a problem.

Ground Planes

Related to the star ground system discussed earlier is the use of a *ground plane*. To implement a ground plane, one side of a double-sided PCB (or one layer of a multilayer one) is made of continuous copper and used as ground. The theory behind this is that the large amount of metal will have as low a resistance as is possible. It will, because of the large flattened conductor pattern, also have as low an inductance as possible. It then offers the best possible conduction, in terms of minimizing spurious ground difference voltages across the conducting plane.

Note that ground plane concept can also be extended to include *voltage planes.* A voltage plane offers advantages similar to a ground plane, i.e., a very low impedance conductor, but is dedicated to one (or more) of the system supply voltages. Thus a system can have more than one voltage plane, as well as a ground plane.

It has been sometimes argued that ground planes shouldn't be used, as they are liable to introduce manufacture and assembly problems. Such an argument may have had limited validity some years ago when PCB adhesives were less well developed, wave-soldering less reliable, and solder resist techniques less well understood, but not today.

A summary of key points related to the construction and operation of ground planes is contained in Figure 7-28.

- ONE ENTIRE PCB SIDE (OR LAYER) IS A CONTINUOUS GROUNDED CONDUCTOR.
- THIS GIVES MINIMUM GROUND RESISTANCE AND INDUCTANCE, BUT ISN'T ALWAYS SUFFICIENT TO SOLVE ALL GROUNDING PROBLEMS.
- BREAKS IN GROUND PLANES CAN IMPROVE OR DEGRADE CIRCUIT PERFORMANCE — THERE IS NO GENERAL RULE.
- YEARS AGO GROUND PLANES WERE DIFFICULT TO FABRICATE. TODAY THEY AREN'T.
- MULTI-LAYER, GROUND AND VOLTAGE PLANE PCB DESIGNS ARE STANDARD

Figure 7-28: Characteristics of ground planes

While ground planes solve many ground impedance problems, it should still be understood they aren't a panacea. Even a continuous sheet of copper foil has residual resistance and inductance, and in some circumstances, these can be enough to prevent proper circuit function. Designers should be wary of injecting very high currents in a ground plane, as they can produce voltage drops that interfere with sensitive circuitry.

Skin Effect

At high frequencies, also consider *skin effect*, where inductive effects cause currents to flow only in the outer surface of conductors. Note that this is in contrast to the earlier discussions of this section on dc resistance of conductors.

The skin effect has the consequence of increasing the resistance of a conductor at high frequencies. Note also that this effect is separate from the increase in impedance due to the effects of the self-inductance of conductors as frequency is increased.

Skin effect is quite a complex phenomenon, and detailed calculations are beyond the scope of this discussion. However, a good approximation for copper is that the skin depth in centimeters is $6.61/\sqrt{f}$, (f in Hz).

A summary of the skin effect within a typical PCB conductor foil is shown in Figure 7-29. Note that this copper conductor cross-sectional view assumes looking into the *side* of the conducting trace.

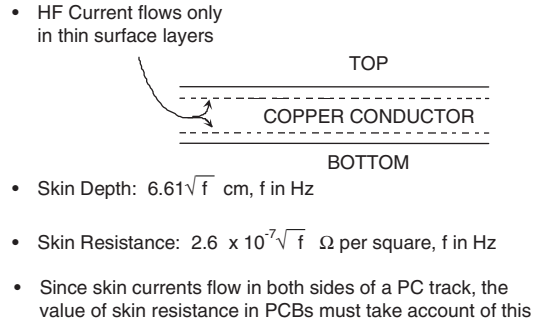


Figure 7-29: Skin depth in a PC conductor

Assuming that skin effects become important when the skin depth is less than 50% of the thickness of the conductor, this tells us that for a typical PC foil, we must be concerned about skin effects at frequencies above approximately 12 MHz.

Where skin effect is important, the resistance for copper is $2.6 \times 10^{-7} \sqrt{f}\ \Omega$ per square, (f in Hz). This formula is invalid if the skin thickness is greater than the conductor thickness (i.e., at dc or LF).

Figure 7-30 illustrates a case of a PCB conductor with current flow, as separated from the ground plane underneath.

In this diagram, note the (dotted) regions of HF current flow, as reduced by the skin effect. When calculating skin effect in PCBs, it is important to remember that current generally flows in both sides of the PC foil (this is not necessarily the case in microstrip lines, see below), so the resistance per square of PC foil may be half the above value.

Transmission Lines

We earlier considered the benefits of outward and return signal paths being close together so that inductance is minimized. As shown previously in Figure 7-30, when an HF signal flows in a PC track running over a ground plane, the arrangement functions as a *microstrip* transmission line, and the majority of the return current flows in the ground plane underneath the line.

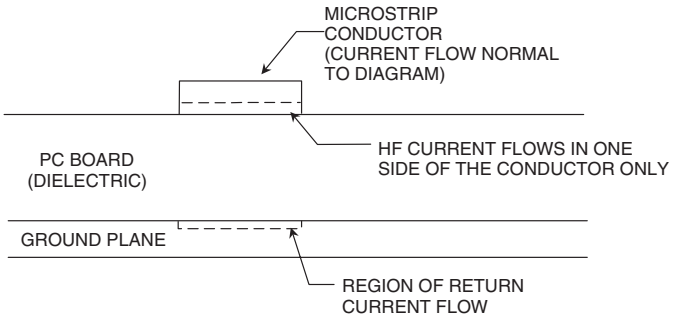


Figure 7-30: Skin effect with PC conductor and ground plane

Figure 7-31 shows the general parameters for a microstrip transmission line, given the conductor width, w, dielectric thickness, h, and the dielectric constant, E_r.

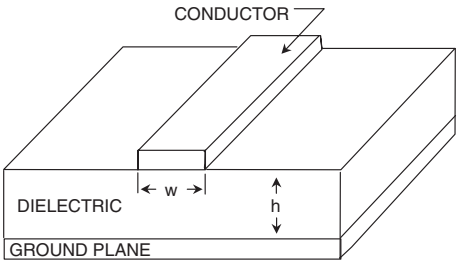


Figure 7-31: A PCB microstrip transmission line is an example of a controlled impedance conductor pair

The characteristic impedance of such a microstrip line will depend upon the width of the track and the thickness and dielectric constant of the PCB material. Designs of microstrip lines are covered in more detail within section six of this chapter.

For most dc and lower frequency applications, the characteristic impedance of PCB traces will be relatively unimportant. Even at frequencies where a track over a ground plane behaves as a transmission line, it is not necessary to worry about its characteristic impedance or proper termination if the free space wavelengths of the frequencies of interest are greater than ten times the length of the line.

However, at VHF and higher frequencies it is possible to use PCB tracks as microstrip lines within properly terminated transmission systems. Typically the microstrip will be designed to match standard coaxial cable impedances, such as 50 Ω, 75 Ω or 100 Ω, simplifying interfacing.

Note that if losses in such systems are to be minimized, the PCB material must be chosen for low high frequency losses. This usually means the use of Teflon or some other comparably low-loss PCB material. Often, though, the losses in short lines on cheap glass-fiber board are small enough to be quite acceptable.

Be Careful with Ground Plane Breaks

Wherever there is a break in the ground plane beneath a conductor, the ground plane return current must by necessity flow *around* the break. As a result, both the inductance and the vulnerability of the circuit to external fields are increased. This situation is diagrammed in Figure 7-32, where conductors A and B must cross one another.

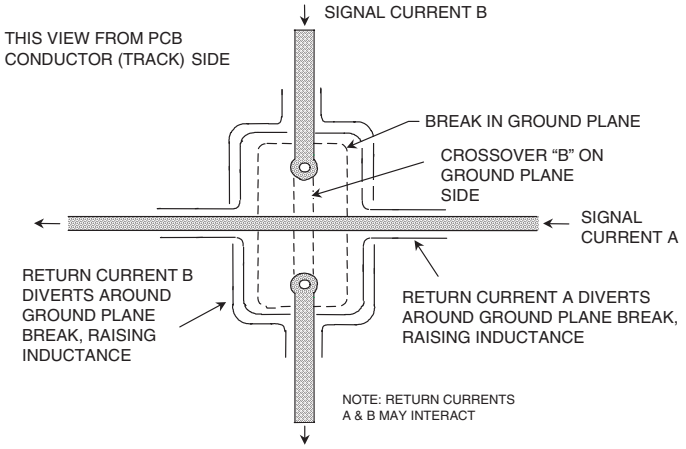


Figure 7-32: A ground plane break raises circuit inductance and increases vulnerability to external fields

Where such a break is made to allow a crossover of two perpendicular conductors, it would be far better if the second signal were carried across both the first and the ground plane by means of a piece of wire. The ground plane then acts as a shield between the two signal conductors, and the two ground return currents, flowing in opposite sides of the ground plane as a result of skin effects, do not interact.

With a multilayer board, both the crossover and the continuous ground plane can be accommodated without the need for a wire link. Multilayer PCBs are expensive and harder to trouble-shoot than more simple double-sided boards, but do offer even better shielding and signal routing. The principles involved remain unchanged but the range of layout options is increased.

The use of double-sided or multilayer PCBs with at least one continuous ground plane is undoubtedly one of the most successful design approaches for high performance mixed signal circuitry. Often the impedance of such a ground plane is sufficiently low to permit the use of a single ground plane for both analog and digital parts of the system. However, whether or not this is possible does depend upon the resolution and bandwidth required, and the amount of digital noise present in the system.

Ground Isolation Techniques

While the use of ground planes does lower impedance and helps greatly in lowering ground noise, there may still be situations where a prohibitive level of noise exists. In such cases, the use of ground error minimization and isolation techniques can be helpful.

Another illustration of a common-ground impedance coupling problem is shown in Figure 7-33. In this circuit, a precision gain-of-100 preamp amplifies a low level signal V_{IN}, using an AD8551 chopper-stabilized amplifier for best dc accuracy. At the load end, the signal V_{OUT} is measured with respect to G2, the local

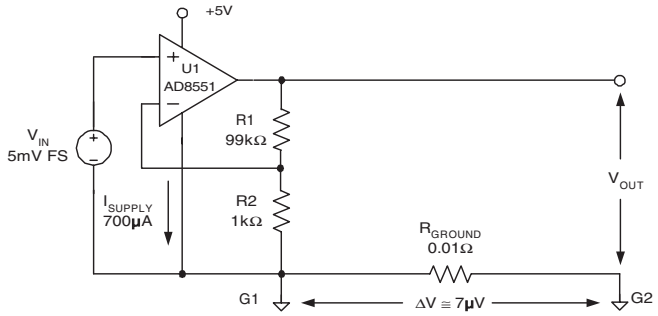


Figure 7-33: Unless care is taken, even small common ground currents can degrade precision amplifier accuracy

ground. Because of the small 700 μA I_{SUPPLY} of the AD8551 flowing between G1 and G2, there is a 7 μV ground error—about seven times the typical input offset expected from the op amp.

This error can be avoided simply by routing the negative supply pin current of the op amp back to star ground G2 as opposed to ground G1, by using a separate trace. This step eliminates the G1-G2 path power supply current, and so minimizes the ground leg voltage error. Note that little error will be developed in the "hot" V_{OUT} lead, as long as the current drain at the load end is small.

In some cases, there may be simply unavoidable ground voltage differences between a source signal and the load point where it is to be measured. Within the context of this "same-board" discussion, this might require rejecting ground error voltages of several tens-of-mV. Or, should the source signal originate from an "off-board" source, the magnitude of the common-mode voltages to be rejected can easily rise into a several volt range (or even tens-of-volts).

Fortunately, full signal transmission accuracy can still be accomplished in the face of such high noise voltages, by employing a principle discussed earlier. This is the use of a differential-input, *ground isolation* amplifier. The ground isolation amplifier minimizes the effect of ground error voltages between stages by processing the signal in differential fashion, thereby rejecting CM voltages by a substantial margin (typically 60 dB or more).

Two ground isolation amplifier solutions are shown in Figure 7-34. This diagram can alternately employ either the AD629 to handle CM voltages up to ±270 V, or the AMP03, which is suitable for CM voltages up to ±20 V.

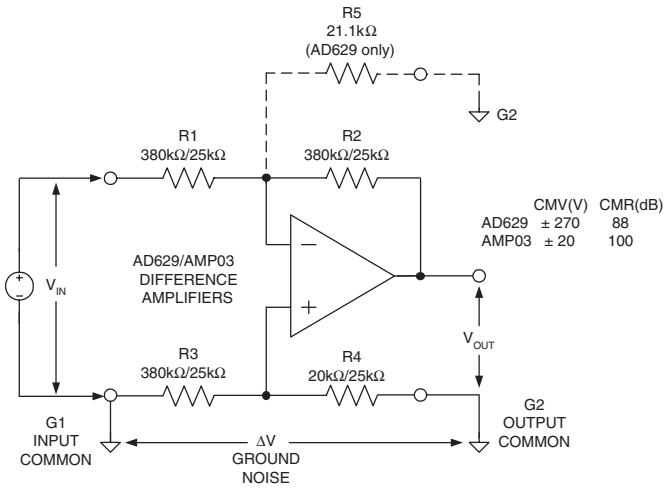


Figure 7-34: A differential input ground isolating amplifier allows high transmission accuracy by rejecting ground noise voltage between source (G1) and measurement (G2) grounds

In the circuit, input voltage V_{IN} is referred to G1, but must be measured with respect to G2. With the use of a high CMR unity-gain difference amplifier, the noise voltage ΔV existing between these two grounds is easily rejected. The AD629 offers a typical CMR of 88 dB, while the AMP03 typically achieves 100 dB. In the AD629, the high CMV rating is done by a combination of high CM attenuation, followed by differential gain, realizing a net differential gain of unity. The AD629 uses the first listed value resistors noted in the figure for R1–R5. The AMP03 operates as a precision four-resistor differential amplifier, using the 25 kΩ value R1–R4 resistors noted. Both devices are complete, one package solutions to the ground-isolation amplifier.

This scheme allows relative freedom from tightly controlling ground drop voltages, or running additional and/or larger PCB traces to minimize such error voltages. Note that it can be implemented with either the fixed gain difference amplifiers shown, or with a standard in amp IC, configured for unity gain. The AD623, for example, also allows single-supply use. In any case, signal polarity is also controllable by simple reversal of the difference amplifier inputs.

In general terms, transmitting a signal from one point on a PCB to another for measurement or further processing can be optimized by two key interrelated techniques. These are the use of high-impedance, differential signal-handling techniques. The high impedance loading of an in amp minimizes voltage drops, and differential sensing of the remote voltage minimizes sensitivity to ground noise.

When the further signal processing is A/D conversion, these transmission criteria can be implemented *without* adding a differential ground isolation amplifier stage. Simply select an ADC that operates differentially. The high input impedance of the ADC minimizes load sensitivity to the PCB wiring resistance. In addition, the differential input feature allows the output of the source to be sensed directly at the source output terminals (even if single-ended). The CMR of the ADC then eliminates sensitivity to noise voltages between the ADC and source grounds.

An illustration of this concept using an ADC with high impedance differential inputs is shown in Figure 7-35. Note that the general concept can be extended to virtually any signal source, driving any load. All loads, even single-ended ones, become differential-input by adding an appropriate differential input stage.

The differential input can be provided by either a fully developed high-Z in amp, or in many cases it can be a simple subtractor stage op amp, such as Figure 7-34.

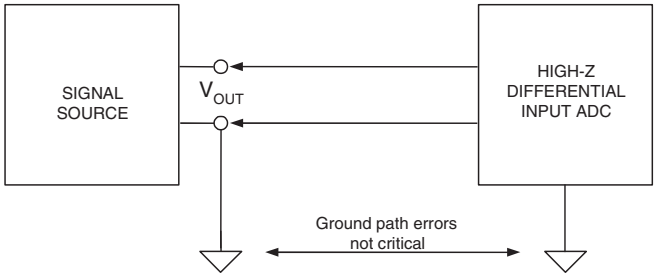


Figure 7-35: A high-impedance differential input ADC also allows high transmission accuracy between source and load

Static PCB Effects

Leakage resistance is the dominant static circuit board effect. Contamination of the PCB surface by flux residues, deposited salts, and other debris can create leakage paths between circuit nodes. Even on well-cleaned boards, it is not unusual to find 10 nA or more of leakage to nearby nodes from 15 V supply rails. Nanoamperes of leakage current into the wrong nodes often cause volts of error at a circuit's output; for example, 10 nA into a 10 megohm resistance causes 0.1 V of error. Unfortunately, the standard op amp pinout places the $-V_S$ supply pin next to the + input, which is often hoped to be at high impedance. To help identify nodes sensitive to the effects of leakage currents ask the simple question: If a spurious current of a few nanoamperes or more were injected into this node, would it matter?

If the circuit is already built, moisture sensitivity can be localized to a suspect node with a classic test. While observing circuit operation, blow on potential trouble spots through a simple soda straw. The straw focuses the breath's moisture which, with the board's salt content in susceptible portions of the design, disrupts circuit operation upon contact.

There are several means of eliminating simple surface leakage problems. Thorough washing of circuit boards to remove residues helps considerably. A simple procedure includes vigorously brushing the boards with isopropyl alcohol, followed by thorough washing with deionized water and an 85°C bakeout for a few hours. Be careful when selecting board-washing solvents, though. When cleaned with certain solvents, some water-soluble fluxes create salt deposits, exacerbating the leakage problem.

Unfortunately, if a circuit displays sensitivity to leakage, even the most rigorous cleaning can offer only a temporary solution. Problems soon return upon handling, or exposure to foul atmospheres, and high humidity. Some additional means must be sought to stabilize circuit behavior, such as conformal surface coating.

Fortunately, there is an answer to this, namely *guarding*, which offers a fairly reliable and permanent solution to the problem of surface leakage. Well-designed guards can eliminate leakage problems, even for circuits exposed to harsh industrial environments. Two schematics illustrate the basic guarding principle, as applied to typical inverting and noninverting op amp circuits.

Figure 7-36 illustrates an inverting mode guard application. In this case, the op amp reference input is grounded, so the guard is a grounded ring surrounding all leads to the inverting input, as noted by the dotted line.

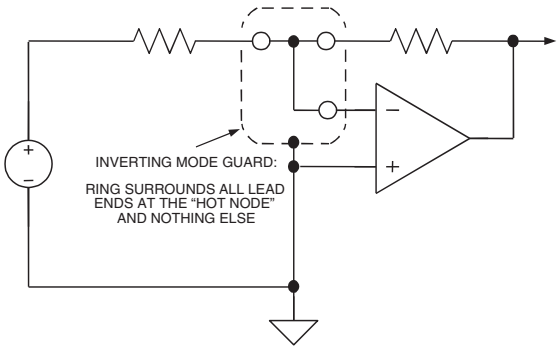


Figure 7-36: Inverting mode guard encloses all op amp inverting input connections within a grounded guard ring

Guarding basic principles are simple: *Completely* surround sensitive nodes with conductors that can readily sink stray currents, and maintain the guard conductors at the exact potential of the sensitive node (as otherwise the guard will serve as a leakage source rather than a leakage sink). For example, to keep leakage into a node below 1 pA (assuming 1000-megohm leakage resistance) the guard and guarded node must be within 1 mV. Generally, the low offset of a modern op amp is sufficient to meet this criterion.

There are important caveats to be noted with implementing a true high-quality guard. For traditional through-hole PCB connections, the guard pattern should appear on *both* sides of the circuit board, to be most effective. And, it should also be connected along its length by several vias. Finally, when either justified or required by the system design parameters, do make an effort to include guards in the PCB design process from the outset—there is little likelihood that a proper guard can be added as an afterthought.

Figure 7-37 illustrates the case for a noninverting guard. In this instance the op amp reference input is directly driven by the source, which complicates matters considerably. Again, the guard ring completely surrounds all of the input nodal connections. In this instance, however, the guard is driven from the low impedance feedback divider connected to the inverting input.

Usually the guard-to-divider junction will be a direct connection, but in some cases a unity gain buffer might be used at "X" to drive a cable shield, or also to maintain the lowest possible impedance at the guard ring.

In lieu of the buffer, another useful step is to use an additional, directly grounded screen ring, "Y," which surrounds the inner guard and the feedback nodes as shown. This step costs nothing except some added layout time, and will greatly help buffer leakage effects into the higher impedance inner guard ring.

Of course what hasn't been addressed to this point is just how the op amp itself is connected into these guarded islands without compromising performance. The traditional method, using a TO-99 metal can package device, was to employ double-sided PCB guard rings, with both op amp inputs terminated within the guarded ring.

The high impedance sensor discussions in Chapter 4 use the above-described method. The section immediately following illustrates how more modern IC packages can be mounted to PCB patterns, and take advantage of guarding and low-leakage operation.

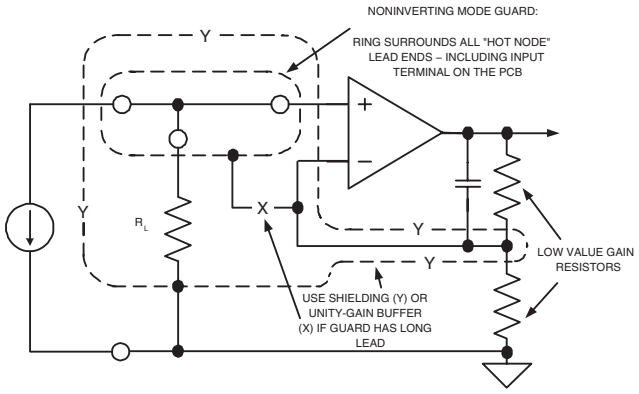


Figure 7-37: Noninverting mode guard encloses all op amp noninverting input connections within a low impedance, driven guard ring

Sample MINIDIP and SOIC Op Amp PCB Guard Layouts

Modern assembly practices have favored smaller plastic packages such as 8-pin MINIDIP and SOIC types. Some suggested partial layouts for guard circuits using these packages is shown in Figures 7-38 and 7-39. While guard traces may also be possible with even more tiny op amp footprints, such as SOT23 and so forth, the required trace separations become even more confining, challenging the layout designer as well as the manufacturing processes.

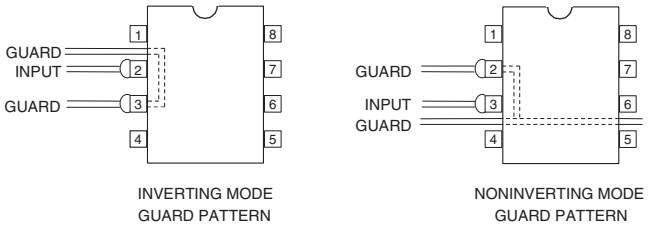


Figure 7-38: PCB guard patterns for inverting and noninverting mode op amps using 8-pin MINIDIP (N) package

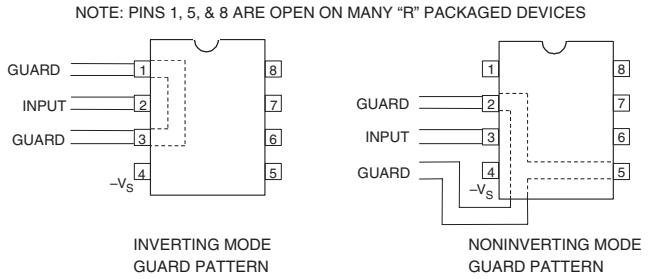


Figure 7-39: PCB guard patterns for inverting and noninverting mode op amps using 8-pin SOIC (R) package

For the ADI "N" style MINIDIP package, Figure 7-38 illustrates how guarding can be accomplished for inverting (left) and noninverting (right) operating modes. This setup would also be applicable to other op amp devices where relatively high voltages occur at Pin 1 or 4. Using a standard 8-pin DIP outline, it can be noted that this package's 0.1" pin spacing allows a PC trace (here, the guard trace) to pass between adjacent pins. This is the key to implementing effective DIP package guarding, as it can adequately prevent a leakage path from the $-V_S$ supply at Pin 4, or from similar high potentials at Pin 1.

For the left-side inverting mode, note that the Pin 3 connected and grounded guard traces surround the op amp inverting input (Pin 2), and run parallel to the input trace. This guard would be continued out to and around the source and feedback connections of Figure 7-36 (or other similar circuit), including an input pad in the case of a cable. In the right-side noninverting mode, the guard voltage is the feedback divider voltage to Pin 2. This corresponds to the inverting input node of the amplifier, from Figure 7-37.

Note that in both cases of Figure 7-38, the guard physical connections shown are only partial—an actual layout would include all sensitive nodes within the circuit. In both the inverting and the noninverting modes using the MINIDIP or other through-hole style package, the PCB guard traces should be located on both sides of the board, with top and bottom traces connected with several vias.

Things become slightly more complicated when using guarding techniques with the SOIC surface-mount ("R") package, as the 0.05" pin spacing doesn't easily allow routing of PCB traces between the pins. But, there is still an effective guarding answer, at least for the inverting case. Figure 7-39 shows guards for the ADI "R" style SOIC package.

Note that for many single op amp devices in this SOIC "R" package, Pins 1, 5, and 8 are "no connect" pins. For such instances, this means that these locations can be employed in the layout to route guard traces. In the case of the inverting mode (left), the guarding is still completely effective, with the dummy Pin 1 and Pin 3 serving as the grounded guard trace. This is a fully effective guard without compromise. Also, with SOIC op amps, much of the circuitry around the device will not use through-hole components. So, the guard ring may only be necessary on the op amp PCB side.

In the case of the follower stage (right), the guard trace must be routed around the negative supply at Pin 4, and thus Pin 4 to Pin 3 leakage isn't fully guarded. For this reason, a precision high impedance follower stage using an SOIC package op amp isn't generally recommended, as guarding isn't possible for dual supply connected devices.

However, an exception to this caveat does apply to the use of a *single-supply* op amp as a noninverting stage. For example, if the AD8551 is used, Pin 4 becomes ground, and some degree of intrinsic guarding is then established by default.

Dynamic PCB Effects

Although static PCB effects can come and go with changes in humidity or board contamination, problems that most noticeably affect the dynamic performance of a circuit usually remain relatively constant. Short of a new design, washing or any other simple fixes can't fix them. As such, they can permanently and adversely affect a design's specifications and performance. The problems of stray capacitance, linked to lead and component placement, are reasonably well known to most circuit designers. Since lead placement can be permanently dealt with by correct layout, any remaining difficulty is solved by training assembly personnel to orient components or bend leads optimally.

Dielectric absorption (DA), on the other hand, represents a more troublesome and still poorly understood circuit-board phenomenon. Like DA in discrete capacitors, DA in a printed-circuit board can be modeled by a series resistor and capacitor connecting two closely spaced nodes. Its effect is inverse with spacing and linear with length.

As shown in Figure 7-40, the RC model for this effective capacitance ranges from 0.1 pF to 2.0 pF, with the resistance ranging from 50 MΩ to 500 MΩ. Values of 0.5 pF and 100 MΩ are most common. Consequently, circuit-board DA interacts most strongly with high-impedance circuits.

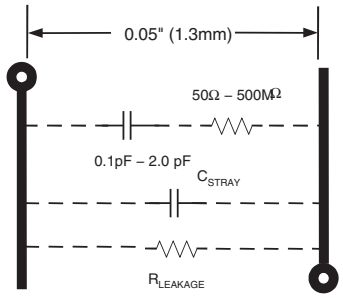


Figure 7-40: DA plagues dynamic response of PCB-based circuits

PCB DA most noticeably influences dynamic circuit response, for example, settling time. Unlike circuit leakage, the effects aren't usually linked to humidity or other environmental conditions but, rather, are a function of the board's dielectric properties. The chemistry involved in producing plated-through holes seems to exacerbate the problem. If circuits don't meet expected transient response specs, consider PCB DA as a possible cause.

Fortunately, there are solutions. As in the case of capacitor DA, external components can be used to compensate for the effect. More importantly, surface guards that totally isolate sensitive nodes from parasitic coupling often eliminate the problem (note that these guards should be duplicated on both sides of the board, in cases of through-hole components). As previously noted, low loss PCB dielectrics are also available.

PCB "hook," similar if not identical to DA, is characterized by variation in effective circuit-board capacitance with frequency (see Reference 1). In general, it affects high impedance circuit transient response where board capacitance is an appreciable portion of the total in the circuit. Circuits operating at frequencies below 10 kHz are the most susceptible. As in circuit board DA, the board's chemical makeup very much influences its effects.

Stray Capacitance

When two conductors aren't short-circuited together, or totally screened from each other by a conducting (Faraday) screen, there is a capacitance between them. So, on any PCB, there will be a large number of capacitors associated with any circuit (which may or may not be considered in models of the circuit). Where high frequency performance matters (and even dc and VLF circuits may use devices with high Ft and therefore be vulnerable to HF instability), it is very important to consider the effects of this stray capacitance.

Any basic textbook will provide formulas for the capacitance of parallel wires and other geometric configurations (see References 9 and 10). The example to be considered in this discussion is the parallel plate capacitor, often formed by conductors on opposite sides of a PCB. The basic diagram describing this capacitance is shown in Figure 7-41.

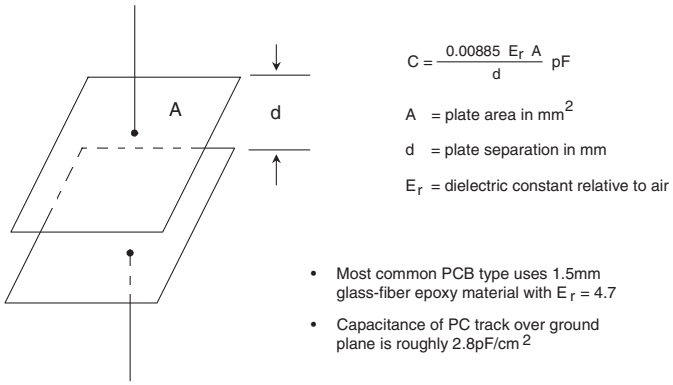


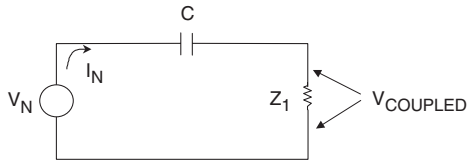
Figure 7-41: Capacitance of two parallel plates

From this formula, it can be calculated that for general-purpose PCB material ($E_r = 4.7$, d = 1.5mm), the capacitance between conductors on opposite sides of the board is just under 3pF/cm^2. In general, such capacitance will be parasitic, and circuits must be designed so that it does not affect their performance.

While it is possible to use PCB capacitance in place of small discrete capacitors, the dielectric properties of common PCB substrate materials cause such capacitors to behave poorly. They have a rather high temperature coefficient and poor Q at high frequencies, which makes them unsuitable for many applications. Boards made with lower-loss dielectrics such as Teflon are expensive exceptions to this rule.

Capacitive Noise and Faraday Shields

There is a capacitance between any two conductors separated by a dielectric (air or vacuum are dielectrics). If there is a change of voltage on one, there will be a movement of charge on the other. A basic model for this is shown in Figure 7-42.



Z_1 = CIRCUIT IMPEDANCE

$Z_2 = 1/j\omega C$

$V_{COUPLED} = V_N \left(\frac{Z_1}{Z_1 + Z_2} \right)$

Figure 7-42: Capacitive coupling equivalent circuit model

It is evident that the noise voltage, $V_{COUPLED}$, appearing across Z_1, may be reduced by several means, all of which reduce noise current in Z_1. They are reduction of the signal voltage V_N, reduction of the frequency involved, reduction of the capacitance, or reduction of Z_1 itself. Unfortunately, however, often none of these circuit parameters can be freely changed, and an alternate method is needed to minimize the interference. The best solution towards reducing the noise coupling effect of C is to insert a grounded conductor, also known as a *Faraday shield*, between the noise source and the affected circuit. This has the desirable effect of reducing Z_1 noise current, thus reducing $V_{COUPLED}$.

A Faraday shield model is shown by Figure 7-43. In the left picture, the function of the shield is noted by how it effectively divides the coupling capacitance, C. In the right picture the net effect on the coupled voltage across Z_1 is shown. Although the noise current I_N still flows in the shield, most of it is now diverted away from Z_1. As a result, the coupled noise voltage $V_{COUPLED}$ across Z_1 is reduced.

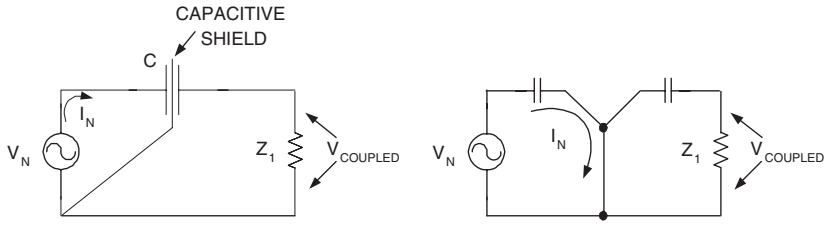


Figure 7-43: An operational model of a Faraday shield

A Faraday shield is easily implemented and almost always successful. Thus capacitively coupled noise is rarely an intractable problem. However, to be fully effective, a Faraday shield must completely block the electric field between the noise source and the shielded circuit. It must also be connected so that the displacement current returns to its source, without flowing in any part of the circuit where it can introduce conducted noise.

The Floating Shield Problem

It is quite important to note here that *a conductor that is intended to function as a Faraday shield must never be left floating, as this almost always increases capacity and exacerbates the noise problem*.

An example of this "floating shield" problem is seen in side-brazed ceramic IC packages. These DIP packages have a small square conducting Kovar lid soldered onto a metallized rim on the ceramic package top. Package manufacturers offer only two options: the metallized rim may be connected to one of the corner pins of the package, or it may be left unconnected.

Most logic circuits have a ground pin at one of the package corners, and therefore the lid is grounded. Alas, many analog circuits don't have a ground pin at a package corner, and the lid is left floating—acting as an antenna for noise. Such circuits turn out to be far more vulnerable to electric field noise than the same chip in a plastic DIP package, where the chip is completely unshielded.

Whenever practical, it is good practice for the user to ground the lid of any side-brazed ceramic IC where the lid is not grounded by the manufacturer, thus implementing an *effective* Faraday shield. This can be done with a wire soldered to the lid (this will not damage the device, as the chip is thermally and electrically isolated from the lid). If soldering to the lid is unacceptable, a grounded phosphor-bronze clip may be used to make the ground connection, or conductive paint from the lid to the ground pin.

A safety note is appropriate at this point. Never attempt to ground such a lid without first verifying that it is unconnected. Occasionally device types are found with the lid connected to a power supply rather than to ground.

A case where a Faraday shield is impracticable is between IC chip bondwires, which has important consequences. The stray capacitance between chip bondwires and associated leadframes is typically ≈ 0.2 pF, with observed values generally between 0.05 pF and 0.6 pF.)

Buffering ADCs against Logic Noise

If a high resolution data converter (ADC or DAC) is connected to a high speed data bus that carries logic noise with a 2 V/ns–5 V/ns edge rate, this noise is easily connected to the converter analog port via stray capacitance across the device. Whenever the data bus is active, intolerable amounts of noise are capacitively coupled into the analog port, thus seriously degrading performance.

This particular effect is illustrated by the diagram of Figure 7-44, where multiple package capacitors couple noisy edge signals from the data bus into the analog input of an ADC.

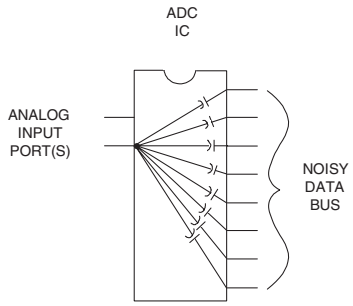


Figure 7-44: A high speed ADC IC sitting on a fast data bus couples digital noise into the analog port, thus limiting performance

Present technology offers no cure for this problem, within the affected IC device itself. The problem also limits performance possible from other broadband monolithic mixed-signal ICs with single-chip analog and digital circuits. Fortunately, this coupled noise problem can be avoided by *not* connecting the data bus directly to the converter.

Instead, *use a CMOS latched buffer as a converter-to-bus interface*, as shown by Figure 7-45. Now the CMOS buffer IC acts as a Faraday shield and dramatically reduces noise coupling from the digital bus. This solution costs money, occupies board area, reduces reliability (very slightly), consumes power, and complicates the design—but it does improve the signal-to-noise ratio of the converter. The designer must decide whether it is worthwhile for individual cases, but in general it is highly recommended.

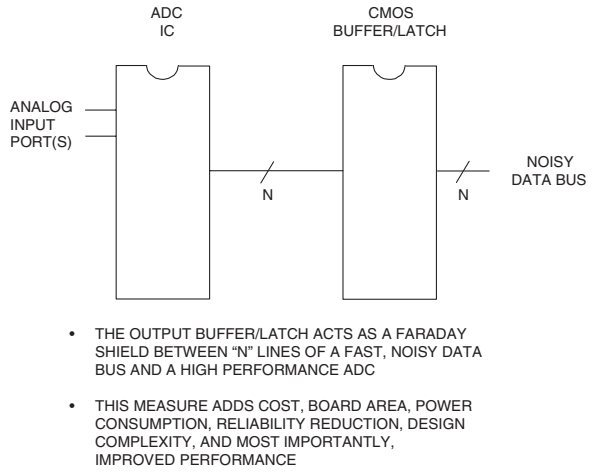


Figure 7-45: A high speed ADC IC using a CMOS buffer/latch at the output shows enhanced immunity of digital data bus noise

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SECTION 7-3

Op Amp Power Supply Systems

Walt Jung, Walt Kester

Op amp circuits have traditionally been powered from well-regulated, low noise linear power supplies. This type of power system is typically characterized by medium-to-low power conversion efficiency. Such linear regulators usually excel in terms of self-generated and radiated noise components. If the designer's life were truly simple, it might continue with such familiar designs offering good performance and minimal side effects.

But, the designer's life is hardly so simple. Modern systems may allow using linear regulators, but multiple output levels and/or polarities are often required. There may also be some additional requirements set for efficiency, which may dictate the use of dc-dc conversion techniques, and, unfortunately, their higher associated noise output.

This section addresses power supply design issues for op amp systems, taking into account the regulator types most likely to be used. The primary dc power sources are assumed to be either rectified and smoothed ac sources (i.e., mains derived), a battery stack, or a switching regulator output. The latter example could be fed from either a battery or a mains-derived dc source.

As noted in Figure 7-46, linear mode regulation is generally recommended as an optimum starting point in all instances (first bullet). Nevertheless, in some cases, a degree of hybridization between fully linear and switching mode regulation may be required (second bullet). This could be either for efficiency or other diverse reasons.

- High performance analog power systems use linear regulators, with primary power derived from:
  - AC line power
  - Battery power systems
  - DC- DC power conversion systems
- Switching regulators should be avoided if at all possible, but if not…
  - Apply noise control techniques
  - Use quality layout and grounding
  - Be aware of EMI

Figure 7-46: Regulation priorities for op amp power supply systems

Whenever switching-type regulators are involved in powering precision analog circuits, noise control is very likely to be a design issue. Therefore some focus of this section is on minimizing noise when using switching regulators.

Linear IC Regulation

Linear IC voltage regulators have long been standard power system building blocks. After an initial introduction in 5 V logic voltage regulator form, they have since expanded into other standard voltage levels spanning from 3 V to 24 V, handling output currents from as low as 100 mA (or less) to as high as 5 A (or more). For several good reasons, linear style IC voltage regulators have been valuable system components since the early days. As mentioned above, a basic reason is the relatively low noise characteristic vis-à-vis the switching type of regulator. Others are a low parts count and overall simplicity compared to discrete solutions. But, because of their power losses, these linear regulators have also been known for being relatively inefficient. Early generation devices (of which many are still available) required 2 V or more of unregulated input above the regulated output voltage, making them lossy in power terms.

More recently however, linear IC regulators have been developed with more liberal (i.e., lower) limits on minimum input-output voltage. This voltage, known more commonly as *dropout* voltage, has led to what is termed the *Low DropOut* regulator, or more simply, the LDO. Dropout voltage (V_{MIN}) is defined simply as that minimum input-output differential where the regulator undergoes a 2% reduction in output voltage. For example, if a nominal 5.0 V LDO output drops to 4.9 V (–2%) under conditions of an input-output differential of 0.5 V, by this definition the LDO's dropout voltage is 0.5 V.

Dropout voltage is extremely critical to a linear regulator's power efficiency. The lower the voltage allowable across a regulator while still maintaining a regulated output, the less power the regulator dissipates as a result. A low regulator dropout voltage is the key to this, as it takes a lower dropout to maintain regulation as the input voltage lowers. In performance terms, the bottom line for LDOs is simply that more useful power is delivered to the load and less heat is generated in the regulator. LDOs are key elements of power systems providing stable voltages from batteries, such as portable computers, cellular phones, and so forth. This is because they maintain a regulated output down to lower points on the battery's discharge curve. Or, within classic mains-powered raw dc supplies, LDOs allow lower transformer secondary voltages, reducing system shutdowns under brownout conditions, as well as allowing cooler operation.

Some Linear Voltage Regulator Basics

A brief review of three terminal linear IC regulator fundamentals is necessary before understanding the LDO variety. Most (but not all) of the general three-terminal regulator types available today are *positive leg, series style* regulators. This simply means that they control the regulated voltage output by means of a pass element in series with the positive unregulated input. And, although they are fewer in number, there are also *negative leg* series style regulators, which operate in a fashion complementary to the positive units.

A basic hookup diagram of a three terminal regulator is shown in Figure 7-47. In terms of basic functionality, many standard voltage regulators operate in a series mode, three-terminal form, just as shown here. As can be noted from this figure, the three I/O terminals are V_{IN}, GND (or Common), and V_{OUT}. Note also that this regulator block, in the absence of any assigned voltage polarity, could in principle be a positive type regulator. Or, it might also be a negative style of voltage regulator—the principle is the same for both—a common terminal, as well as input and output terminals.

In operation, two power components become dissipated in the regulator, one a function of $V_{IN} - V_{OUT}$ and I_L, plus a second, which is a function of V_{IN} and I_{GROUND}. The first of these is usually dominant. Analysis of the situation will reveal that as the dropout voltage V_{MIN} is reduced, the regulator is able to deliver a higher percentage of the input power to the load, and is thus more efficient, running cooler and saving power. This is the core appeal of the modern LDO type of regulator (see Reference 1).

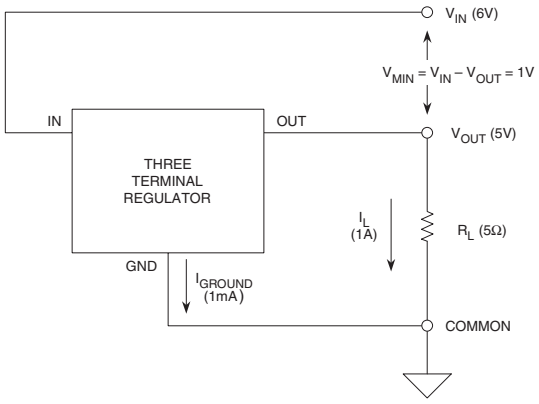

Figure 7-47: A basic three-terminal regulator hookup (either positive or negative)

A more detailed look within a typical regulator block diagram reveals a variety of elements, as is shown in Figure 7-48. Note that all regulators will contain those functional components connected via solid lines. The connections shown dotted indicate options, which might be available when more than three I/O pins are available.

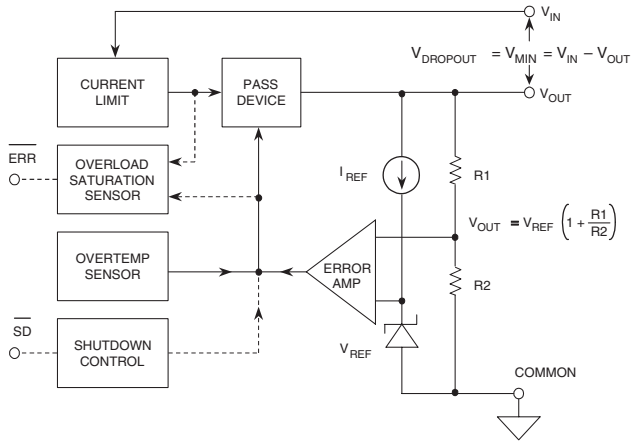

Figure 7-48: Functional diagram of a typical voltage regulator

In operation, a voltage reference block produces a stable voltage V_{REF}, which is almost always a voltage based on the bandgap voltage of silicon, typically ~1.2 V (see Reference 2). This allows output voltages of 3 V or more from supplies as low as 5 V. This voltage drives one input of an error amplifier, with the second input connected to the divider, R1-R2. The error amplifier drives the pass device, which in turn controls the output. The resulting regulated voltage is then simply:

$$V_{OUT} = V_{REF}\left(1 + \frac{R1}{R2}\right) \qquad \text{Eq. 7-1}$$

Pass Devices

The pass device is a foremost regulator part, and the type chosen here has a major influence on almost all regulator performance issues. Most notable among these is dropout voltage, V_{MIN}. Analysis shows that the use of an *inverting* mode pass transistor allows the pass device to be effectively saturated, thus minimizing the associated voltage losses. Therefore, this factor makes the two most desirable pass devices for LDO use a PNP bipolar, or a PMOS transistor. These device types achieve the lowest levels of V_{IN}–V_{OUT} required for LDO operation. In contrast, NPN bipolars are poor as pass devices in terms of low dropout, particularly when they are Darlington connected.

Standard fixed-voltage IC regulator architectures illustrate this point regarding pass devices. For example, the fixed-voltage LM309 5 V regulators and family derivatives such as the 7805, 7815, et al, (and their various low and medium current alternates) are poor in terms of dropout voltage. These designs use a Darlington pass connection, not known for low dropout (~1.5 V typical), or for low quiescent current (~5 mA).

±15 V Regulator Using Adjustable Voltage ICs

Later developments in references and three-terminal regulation techniques led to the development of the *voltage-adjustable* regulator. The original IC to employ this concept was the LM317, a positive regulator. The device produces a fixed reference voltage of 1.25 V, appearing between the V_{OUT} and ADJ pins of the IC. External scaling resistors set up the desired output voltage, adjustable in the range of 1.25 V–30 V. A complementary device, the LM337, operates in similar fashion, regulating negative voltages.

An application example using standard *adjustable* three terminal regulators to implement a ±15 V linear power supply is shown in Figure 7-49. This is a circuit that might be used for powering traditional op amp supply rails. It is capable of better line regulation performance than would an otherwise similar circuit, using standard fixed-voltage regulator devices, such as for example 7815 and 7915 ICs. However, in terms of power efficiency it isn't outstanding, due to the use of the chosen ICs, which require 2 V or more of headroom for operation.

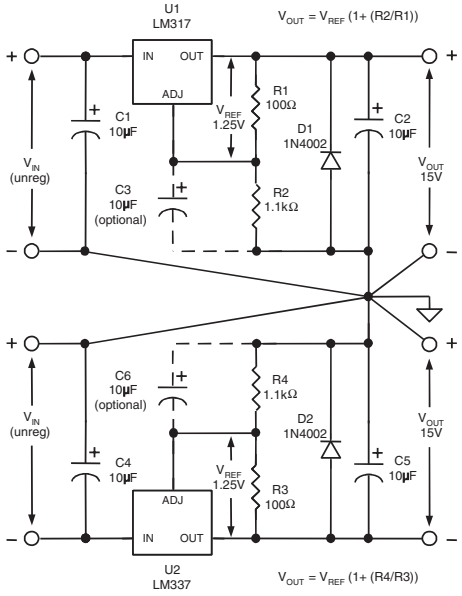

Figure 7-49: A classic ±15 V, 1 A linear supply regulator using adjustable voltage regulator ICs

In the upper portion of this circuit an LM317 adjustable regulator is used, with R2 and R1 chosen to provide a 15 V output at the upper output terminal. If desired, R2 can easily be adjusted for other output levels, according to the figure's V_{OUT} expression. Resistor R1 should be left fixed, as it sets the minimum regulator drain of 10 mA or more.

In this circuit, capacitors C1 and C2 should be tantalum types, and R1-R2 metal films. C3 is optional, but is highly recommended if the lowest level of output noise is desired. The normally reverse biased diode D1 provides a protective output clamp, for system cases where the output voltage would tend to reverse, if one supply should fail. The circuit operates from a rectified and filtered ac supply at V_{IN}, polarized as shown. The output current is determined by choosing the regulator IC for appropriate current capability.

To implement the negative supply portion, the sister device to the LM317 is used, the LM337. The bottom circuit section thus mirrors the operation of the upper, delivering a negative 15 V at the lowest output terminal. Programming of the LM337 for output voltage is similar to that of the LM317, but uses resistors R4 and R3. R4 should be used to adjust the voltage, with R3 remaining fixed. C6 is again optional, but is recommended for reasons of lowest noise.

Low Dropout Regulator Architectures

In contrast to traditional three terminal regulators with Darlington or single-NPN pass devices, low dropout regulators employ lower voltage threshold pass devices. This basic operational difference allows them to operate effectively down to a range of 100 mV–200 mV in terms of their specified V_{MIN}. In terms of use within a system, this factor can have fairly significant operational advantages.

An effective implementation of some key LDO features is contained in the Analog Devices series of anyCAP LDO regulators. Devices of this ADP330x series are so named for their relative insensitivity to the output capacitor, in terms of both its size and ESR. Available in power efficient packages such as the ADI Thermal Coastline (and other thermally-enhanced packages), they come in both stand-alone LDO and LDO controller forms (used with an external PMOS FET). They also offer a wide span of fixed output voltages from 1.8 V to 5 V, with rated current outputs up to 500 mA. User-adjustable output voltage versions are also available. A basic simplified diagram for the family is shown schematically in Figure 7-50.

One of the key differences in the ADP330x LDO series is the use of a high gain vertical PNP pass device, Q1, allowing typical dropout voltages for the series to be on the order of 1 mV/mA for currents of 200 mA or less.

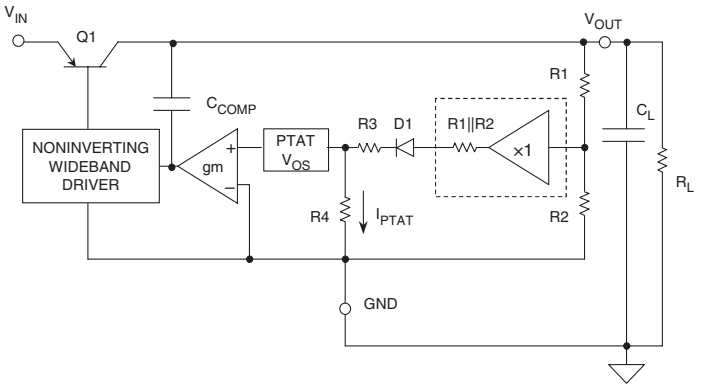

Figure 7-50: The ADP330x anyCAP LDO architecture has both dc and ac performance advantages

In circuit operation, V_{REF} is defined as a reference voltage existing at the output of a zero impedance divider of ratio R1/R2. In Figure 7-50, this is depicted symbolically by the (dotted) unity gain buffer amplifier fed by R1/R2, which has an output of V_{REF}. This reference voltage feeds into a series connection of (dotted) R1‖R2, then actual components D1, R3, R4, and so forth. The regulator output voltage is:

$$V_{OUT} = V_{REF}\left(1+\frac{R1}{R2}\right) \qquad \text{Eq. 7-2}$$

In the various devices of the ADP330X series, the R1-R2 divider is adjusted to produce standard output voltages of 1.8 V, 2.5 V, 2.7 V, 3.0 V, 3.2 V, 3.3 V, and 5.0 V. The regulator behaves as if the entire error amplifier has simply an offset voltage of V_{REF} volts, as seen at the output of a conventional R1-R2 divider.

While the above described dc performance enhancements of the ADP330x series are worthwhile, more dramatic improvements come in areas of ac-related performance. Capacitive loading, and the potential instability it brings, is a major deterrent to easy LDO applications. One method of providing some measure of immunity to variation in an amplifier response pole is the use of a frequency compensation technique called *pole splitting*. In the Figure 7-50 circuit, C_{COMP} functions as the pole splitting capacitor, and provides benefits of a buffered, C_L independent single-pole response. As a result, frequency response is dominated by the regulator's internal compensation, and becomes relatively immune to the value and ESR of load capacitor C_L.

This feature makes the design tolerant of virtually any output capacitor type. C_L, the load capacitor, can be as low as 0.47 µF, and it can also be a multilayer ceramic capacitor (MLCC) type, allowing a very small physical size for the entire regulation function.

Fixed Voltage, 50/100/200/500 mA LDO Regulators

A basic regulator application diagram common to various fixed voltage devices of the ADP330x device series is shown by Figure 7-51. Operation of the various pins and internal functions is discussed next. To adapt this general diagram to a specific current and voltage requirement, select a basic device for output current from the table in the diagram. Then select the output voltage by the part number suffix, consistent with the table.

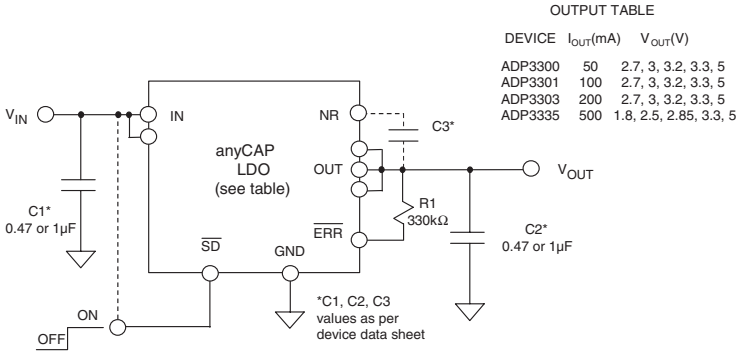

Figure 7-51: A basic LDO regulator hookup useful by device selection from 50 mA to 500 mA, at fixed voltages per table

This circuit is a general one, illustrating common points. For example, the ADP3300 is a 50 mA basic LDO regulator device, designed for those fixed output voltages as noted. An actual ADP3300 device ordered would be ADP3300ART-YY, where the "YY" is a voltage designator suffix such as 2.7, 3, 3.2, 3.3, or 5, for the respective table voltages. The "ART" portion of the part number designates the package (SOT23 6-lead). To produce 5 V from the circuit, use the ADP3300ART-5. Similar comments apply to the other devices, insofar as part numbering. For example, an ADP3301AR-5 depicts an SO-8 packaged 100 mA device, producing 5 V output.

In operation, the circuit produces rated output voltage for loads under the max current limit, for input voltages above $V_{OUT} + V_{MIN}$ (where V_{MIN} is the dropout voltage for the specific device used, at rated current). The circuit is ON when the shutdown input is in a HIGH state, either by a logic HIGH control input to the $\overline{SD}$ pin, or by simply tying this pin to V_{IN} (shown dotted). When $\overline{SD}$ is LOW or grounded, the regulator shuts down, and draws a minimum quiescent current.

The anyCAP regulator devices maintain regulation over a wide range of load, input voltage and temperature conditions. Most devices have a combined error band of ±1.4% (or less). When an overload condition is detected, the open collector $\overline{ERR}$ goes to a LOW state. R1 is a pullup resistor for the $\overline{ERR}$ output. This resistor can be eliminated if the load provides a pullup current.

C3, connected between the OUT and NR pins, can be used for an optional noise reduction (NR) feature. This is accomplished by bypassing a portion of the internal resistive divider, which reduces output noise ~10 dB. When exercised, only the recommended low leakage capacitors as specific to a particular part should be used.

The C1 input and C2 output capacitors should be selected as either 0.47 µF or 1 µF values respectively, again, as per the particular device used. For most devices of the series 0.47 µF suffices, but the ADP3335 uses the 1 µF values. Larger capacitors can also be used, and will provide better transient performance.

Heat sinking of device packages with more than five pins is enhanced, by use of multiple IN and OUT pins. All of the pins available should therefore be used in the PCB design, to minimize layout thermal resistance.

Adjustable Voltage, 200 mA LDO Regulator

In addition to the fixed output voltage LDO devices discussed above, adjustable versions are also available, to realize nonstandard voltages. The ADP3331 is one such device, and shown in Figure 7-52, configured as a 2.8 V output, 200 mA LDO application.

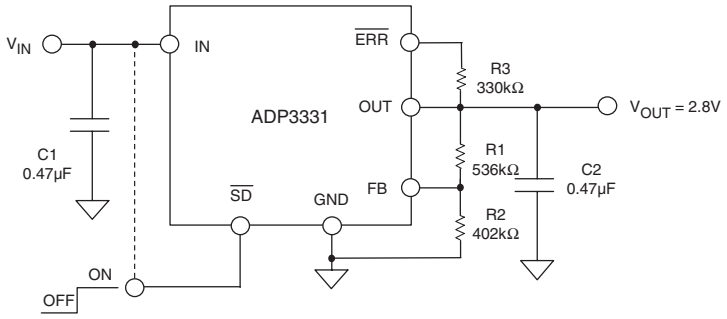

Figure 7-52: An adjustable 200 mA LDO regulator set up for a 2.8 V output

The ADP3331 is generally similar to other anyCAP LDO parts, with two notable exceptions. It has a lower quiescent current (~34 μA when lightly loaded) and most importantly, the output voltage is user-adjustable. As noted in the circuit, R1 and R2 are external precision resistors used to define the regulator operating voltage.

The output of this regulator is V_{OUT}, which is related to feedback pin FB voltage V_{FB} as:

$$V_{OUT} = V_{FB}\left(1+\frac{R1}{R2}\right) \qquad \text{Eq. 7-3}$$

where V_{FB} is 1.204 V. Resistors R1 and R2 program V_{OUT}, and their parallel equivalent should be kept close to 230 kΩ for best stability.

To select R1 and R2, first calculate their ideal values, according to the following two expressions:

$$R1 = 230\left(\frac{V_{OUT}}{V_{FB}}\right)k\Omega \qquad \text{Eq. 7-4}$$

$$R2 = \frac{230}{\left(1+\frac{V_{FB}}{V_{OUT}}\right)}k\Omega \qquad \text{Eq. 7-5}$$

In the example circuit, V_{OUT} is 2.8 V, which yields R1 = 534.9 kΩ, and R2 = 403.5 kΩ. As noted in the figure, closest standard 1% values are used, which provides an output of 2.8093 V (perfect resistors assumed). In practice, the resistor tolerances should be added to the ±1.4% tolerance of the ADP3331 for an estimation of overall error.

To complement the above-discussed anyCAP series of standalone LDO regulators, there is the LDO *regulator controller*. The regulator controller IC picks up where the standalone regulator stops for either load current or power dissipation, using an external PMOS FET pass device. As such, the current capability of the LDO can be extended to several amps. An LDO regulator controller application is shown later in this discussion. The application examples above illustrate a subset of the entire anyCAP family of LDOs. Further information on this series of standalone and regulator controller LDO devices can be found in the references at the end of the section.

Charge-Pump Voltage Converters

Another method for developing supply voltage for op amp systems employs what is known as a *charge-pump* circuit (also called switched capacitor voltage conversion). Charge-pump voltage converters accomplish energy transfer and voltage conversion using charges stored on capacitors, thus the name, charge-pump.

Using switching techniques, charge pumps convert supply voltage of one polarity to a higher or lower voltage, or to an alternate polarity (at either higher or lower voltage). This is accomplished with only an array of low resistance switches, a clock for timing, and a few external storage capacitors to hold the charges being transferred in the voltage conversion process. No inductive components are used, thus EMI generation is kept to a minimum. Although relatively high currents are switched internally, the high current switching is localized, and therefore the generated noise is not as great as in inductive type switchers. With due consideration towards component selection, charge-pump converters can be implemented with reasonable noise performance.

The two common charge-pump voltage converters are the *voltage inverter* and the *voltage doubler* circuits. In a voltage inverter, a charge pump capacitor is charged to the input voltage during the first half of the switching cycle. During the second half of the switching cycle the input voltage stored on the charge pump

capacitor is inverted and applied to an output capacitor and the load. Thus the output voltage is essentially the negative of the input voltage, and the average input current is approximately equal to the output current. The switching frequency impacts the size of the external capacitors required, and higher switching frequencies allow the use of smaller capacitors. The duty cycle—defined as the ratio of charge pump charging time to the entire switching cycle time—is usually 50%, which yields optimal transfer efficiency.

A voltage doubler works similarly to the inverter. In this case the pump capacitor accomplishes a voltage doubling function. In the first phase it is charged from the input, but in the second phase of the cycle it appears in series with the output capacitor. Over time, this has the effect of doubling the magnitude of the input voltage across the output capacitor and load. Both the inverter and voltage doubler circuits provide no voltage regulation in basic form. However, techniques exist to add regulation (discussed below).

There are advantages and disadvantages to using charge-pump techniques, compared to inductor-based switching regulators. An obvious key advantage is the elimination of the inductor and the related magnetic design issues. In addition, charge-pump converters typically have relatively low noise and minimal radiated EMI. Application circuits are simple, and usually only two or three external capacitors are required. Because there are no inductors, the final PCB height can generally be made smaller than a comparable inductance-based switching regulator. Charge-pump inverters are also low in cost, compact, and capable of efficiencies greater than 90%. Obviously, current output is limited by the capacitor size and the switch capacity. Typical IC charge-pump inverters have 150 mA maximum outputs.

On their downside, charge-pump converters don't maintain high efficiency for a wide voltage range of input to output, unlike inductive switching regulators. Nevertheless, they are still often suitable for lower current loads where any efficiency disadvantages are a small portion of a larger system power budget. A summary of general charge-pump operating characteristics is shown in Figure 7-53.

An example of charge-pump applicability is the voltage inverter function. Inverters are often useful where a relatively low current negative voltage (i.e., –3 V) is required, in addition to a primary positive voltage (such as 5 V). This may occur in a single supply system, where only a few high performance parts require the negative voltage. Similarly, voltage doublers are useful in low current applications, where a voltage greater than a primary supply voltage is required.

- No Inductors
- Minimal Radiated EMI
- Simple Implementation: Two External Capacitors (Plus an Input Capacitor)
- Efficiency > 90% Achievable
- Low Cost, Compact, Low Profile (Height)
- Optimized for Doubling or Inverting Supply Voltage:
  – ADM660 or ADM8660
- Voltage Regulated Output Devices Available:
  – ADP3603/ADP3604/ADP3605/ADP3607

Figure 7-53: Some general charge-pump characteristics

Unregulated Inverter and Doubler Charge Pumps

Illustrating these principles are a pair of basic charge-pump ICs from Analog Devices, shown in Figure 7-54. The ADM660 is a popular charge-pump IC, and is shown here operating as both a voltage inverter (left) and the doubler (right). Switching frequency of this IC is selectable between 25 kHz and 120 kHz using the FC input pin. With the FC input is open as shown, the switching frequency is 25 kHz; with it connected to the V+ pin, frequency increases to 120 kHz. Generally, efficiency is greater when operating at the higher frequency. Only two external electrolytic capacitors are required for operation, C1 and C2 (ESR should be <200 mΩ). The value of these capacitors is flexible. For a 25 kHz switching frequency 10 µF tantalum types are recommended; for 120 kHz operation 2.2 µF provides comparable performance. Larger values can also be used, and will provide lower output ripple (at the expense of greater size and cost).

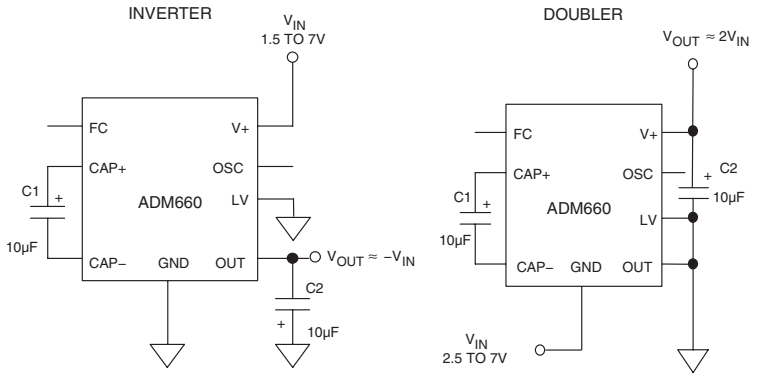

Figure 7-54: ADM660 IC functions as a supply inverter (left) or doubler (right)

These circuits accept V_{IN} inputs over the ranges noted, and deliver a nominal voltage output tracking the input voltage in magnitude, as noted in the output expressions. Although the output voltage is not regulated in these basic designs, it is still relatively low in impedance, due to the nominal 9 Ω resistance of the IC switches.

Efficiency of these circuits using the ADM660/ADM8660 can be 90% or more, for output currents up to 50 mA at a 120 kHz frequency. The ADM8660 is a device similar to the ADM660, however it is optimized for inverter operation, and includes a shutdown feature which reduces the quiescent current to 5 µA.

Regulated Output Charge-Pump Voltage Converters

Adding regulation to a simple charge-pump voltage converter function greatly enhances its usefulness for most applications. There are several techniques for adding regulation to a charge-pump converter. The most straightforward is to follow the charge-pump inverter/doubler with an LDO regulator. The LDO provides the regulated output, and can also reduce the charge-pump converter's ripple. This approach, however, adds complexity and reduces the available output voltage by the dropout voltage of the LDO (~200 mV). These factors may or may not be a disadvantage.

By far the simplest and most effective method for achieving regulation in a charge-pump voltage converter is simply to use a charge-pump design with an internal error amplifier, to control the on-resistance of one of the switches.

This method is used in the ADP3603/ADP3604/ADP3605 voltage inverters, devices offering regulated outputs for positive input voltage ranges. The output is sensed and fed back into the device via a sensing pin, V_{SENSE}. Key features of the series are good output regulation, 3% in the ADP3605, and a high switching frequency of 250 kHz, good for both high efficiency and small component size.

An example circuit for the ADP3605 IC from this series is shown in Figure 7-55. The application is a 5 V to –3 V inverter, with the output regulated ±3% for currents up to 60 mA. In normal operation, the SHUTDOWN pin is connected to ground (as shown dotted). Alternately, a logic HIGH at this pin shuts the device down to a standby current of 2 µA.

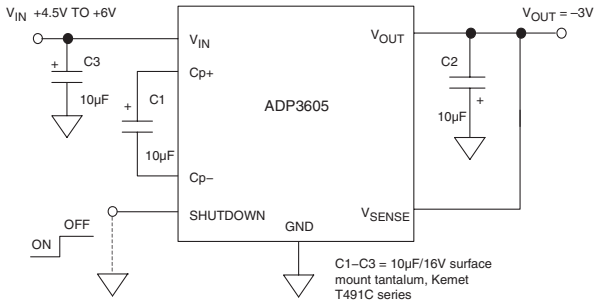

Figure 7-55: ADP3605 5 V to –3 V, 60 mA regulated supply inverter

The 10 µF capacitors for C1–C3 should have ESRs of less than 150 mΩ (4.7 µF can be used at the expense of slightly higher output ripple voltage). C1 is the most critical of the three, because of its higher current flow. The tantalum type listed is recommended for lowest output ripple.

With values as shown, typical output ripple voltage ranges up to approximately 60 mV as the output current varies over the 60 mA range. Although output is regulated for currents up to 60 mA, higher currents of up to 100 mA are also possible with further voltage deviation, and proportionally greater ripple.

These application examples illustrate a subset of the entire charge-pump IC family. Further information on these devices can be found in the end-of-section references.

Linear Post Regulator for Switching Supplies

Another powerful noise reduction option that can be utilized in conjunction with a switching type supply is the option of a *linear post regulator* stage. This is at best an LDO type of regulator, chosen for the desired clean analog voltage level and current. It is preceded by a switching stage, which might be a buck or boost type inductor-based design, or it may also be a charge-pump. The switching converter allows the overall design to be more power-efficient, and the linear post regulator provides clean regulation at the load, reducing the noise of the switcher. This type of regulator can also be termed *hybrid regulation*, since it combines both switching and linear regulation concepts.

An example circuit is shown in Figure 7-56, which features a 3.3 V/1 A low noise, analog-compatible regulator. It operates from a nominal 9 V supply, using a buck or step-down type of switching regulator, as the first stage at the left. The switcher output is set for a few hundred mV above the desired final voltage output, minimizing power in the LDO stage at the right. This feature can eliminate need for a heat sink on the LDO pass device.

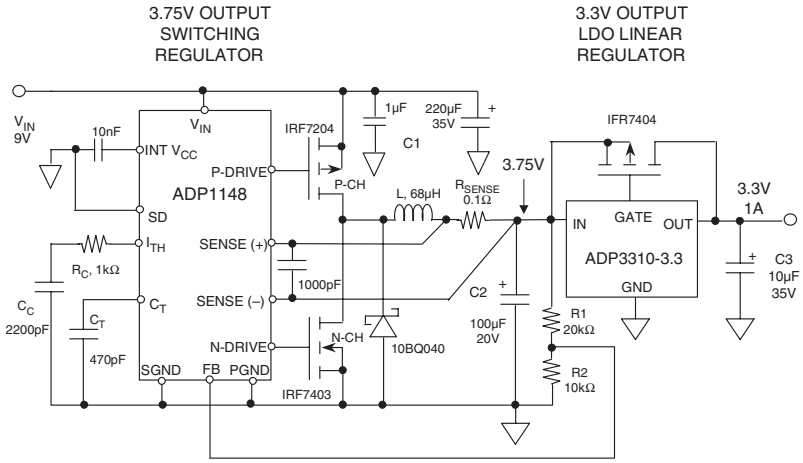

Figure 7-56: A linear post-regulator operating after a switching/ linear regulator is capable of low noise, as well as good dc efficiency

In this example the ADP1148 IC switcher is set up for a 3.75 V output by R1-R2 but, in principle, this voltage can be anything suitable to match the headroom of the companion LDO (within specification limits, of course). In addition, the principle extends to any LDO devices and other current levels, and other switching regulators. The ADP3310-3.3 is a fixed-voltage LDO controller, driving a PMOS FET pass device, with a 3.3 V output.

The linear post regulation stage provides both noise-reduction (in this case about 14 dB), as well as good dc regulation. To realize best results, good grounding practices must be followed. In tests, noise at the 3.3 V output was about 5mV p-p at the 150 kHz switcher frequency. Note that the LDO noise rejection for such relatively high frequencies is much less than at 100 Hz/120 Hz. Note also that C2's ESR will indirectly control the final noise output. The ripple figures given are for a general-purpose C2 part, and can be improved.

Power Supply Noise Reduction and Filtering

During the last decade or so, switching power supplies have become much more common in electronic systems. As a consequence, they also are being used for analog supplies. Good reasons for the general popularity include their high efficiency, low temperature rise, small size, and light weight.

In spite of these benefits, switchers *do* have drawbacks, most notably high output noise. This noise generally extends over a broad band of frequencies, resulting in both conducted and radiated noise, as well as unwanted electric and magnetic fields. Voltage output noise of switching supplies are short-duration voltage transients, or spikes. Although the fundamental switching frequency can range from 20 kHz to 1 MHz, the spikes can contain frequency components extending to 100 MHz or more. While specifying switching supplies in terms of RMS noise is common vendor practice, as a user you should also specify the *peak* (or p-p) amplitudes of the switching spikes, with the output loading of your system.

This section discusses filter techniques for rendering a switching regulator output *analog ready*, that is sufficiently quiet to power precision op amp and other analog circuitry with relatively small loss of dc terminal voltage. The filter solutions presented are generally applicable to all power supply types incorporating switching element(s) in their energy path. This includes charge-pump as well as other switching type converters and supplies. This section focuses on reducing *conducted type* switching power supply noise with external post filters, as opposed to radiated type noise.

Tools useful for combating high frequency switcher noise are shown by Figure 7-57. These differ in electrical characteristics as well as practicality towards noise reduction, and are listed roughly in an order of priorities. Of these tools, L and C are the most powerful filter elements, and are the most cost-effective, as well as small in size.

- Capacitors
- Inductors
- Ferrites
- Resistors
- Linear Post Regulation
- Proper Layout and Grounding
- Physical Separation

Figure 7-57: Tools useful in reducing power supply noise

Capacitors

Capacitors are probably the single most important filter component for reducing switching-related noise. As noted in the first section of this chapter, there are many different types of capacitors. It is also quite true that understanding of their individual characteristics is absolutely mandatory to the design of effective and practical power supply filters. There are generally three classes of capacitors useful in 10 kHz–100 MHz filters, broadly distinguished as the generic dielectric types; *electrolytic*, *film*, and *ceramic*. These discussions complement earlier ones, focusing on power-related concepts. With any dielectric, a major potential filter loss element is ESR (equivalent series resistance), the net parasitic resistance of the capacitor. ESR provides an ultimate limit to filter performance, and requires more than casual consideration, because it can vary both with frequency and temperature in some types. Another capacitor loss element is ESL (equivalent series inductance). ESL determines the frequency where the net impedance characteristic switches from

capacitive to inductive. This varies from as low as 10 kHz in some electrolytics to as high as 100 MHz or more in chip ceramic types. Both ESR and ESL are minimized when a leadless package is used. All capacitor types mentioned are available in surface mount packages, preferable for high speed uses.

The *electrolytic* family provides an excellent, cost-effective low frequency filter component, because of the wide range of values, a high capacitance-to-volume ratio, and a broad range of working voltages. It includes *general-purpose aluminum electrolytic* types, available in working voltages from below 10 V up to about 500 V, and in size from one to several thousand μF (with proportional case sizes). All electrolytic capacitors are polarized, and cannot withstand more than a volt or so of reverse bias without damage.

A subset of the general electrolytic family includes *tantalum* types, generally limited to voltages of 100 V or less, with capacitance of 500 μF or less (see Reference 7). In a given size, tantalums exhibit a higher capacitance-to-volume ratios than do general purpose electrolytics, and have both a higher frequency range and lower ESR. They are generally more expensive than standard electrolytics, and must be carefully applied with respect to surge and ripple currents.

A subset of aluminum electrolytic capacitors is the *switching* type, designed for handling high pulse currents at frequencies up to several hundred kHz with low losses (see Reference 8). This capacitor type can compete with tantalums in high frequency filtering applications, with the advantage of a broader range of values.

A more specialized high performance aluminum electrolytic capacitor type uses an organic semiconductor electrolyte (see Reference 9). The *OS-CON* capacitors feature appreciably lower ESR and higher frequency range than do other electrolytic types, with an additional feature of minimal low temperature ESR degradation.

Film capacitors are available in very broad value ranges and an array of dielectrics, including polyester, polycarbonate, polypropylene, and polystyrene. Because of the low dielectric constant of these films, their volumetric efficiency is quite low, and a 10 μF/50 V polyester capacitor (for example) is actually a handful. Metalized (as opposed to foil) electrodes do help to reduce size, but even the highest dielectric constant units among film types (polyester, polycarbonate) are still larger than any electrolytic, even using the thinnest films with the lowest voltage ratings (50 V). Where film types excel is in their low dielectric losses, a factor that may not necessarily be a practical advantage for filtering switchers. For example, ESR in film capacitors can be as low as 10 mΩ or less, and the behavior of films generally is very high in terms of Q. In fact, this can cause problems of spurious resonance in filters, requiring damping components.

As typically constructed using wound layers, film capacitors can be inductive, which limits their effectiveness for high frequency filtering. Obviously, only noninductively made film caps are useful for switching regulator filters. One specific style which is noninductive is the *stacked-film* type, where the capacitor plates are cut as small overlapping linear sheet sections from a much larger wound drum of dielectric/plate material. This technique offers the low inductance attractiveness of a plate sheet style capacitor with conventional leads (see References 8 and 10). Obviously, minimal lead length should be used for best high frequency effectiveness. Very high current polycarbonate film types are also available, specifically designed for switching power supplies, with a variety of low inductance terminations to minimize ESL (see Reference 11). Dependent upon their electrical and physical size, film capacitors can be useful at frequencies to above 10 MHz. At the highest frequencies, only stacked film types should be considered. Leadless surface-mount packages are now available for film types, minimizing inductance.

Ceramic is often the capacitor material of choice above a few MHz, due to its compact size, low loss, and availability up to several μF in the high-K dielectric formulations (X7R and Z5U), at voltage ratings up to 200 V (see ceramic families of Reference 7).

Multilayer ceramic “chip caps” are very popular for bypassing and/or filtering at 10 MHz or more, simply because their very low inductance design allows near optimum RF bypassing. For smaller values, ceramic

chip caps have an operating frequency range to 1 GHz. For high frequency applications, a useful selection can be ensured by selecting a value that has a self-resonant frequency *above* the highest frequency of interest.

The capacitor model and waveforms of Figure 7-58 illustrate how the various parasitic model elements become dominant, dependent upon the operating frequency. Assume an input current pulse changing from 0 to 1 A in 100 ns, as noted in the figure, and consider what voltage will be developed across the capacitor.

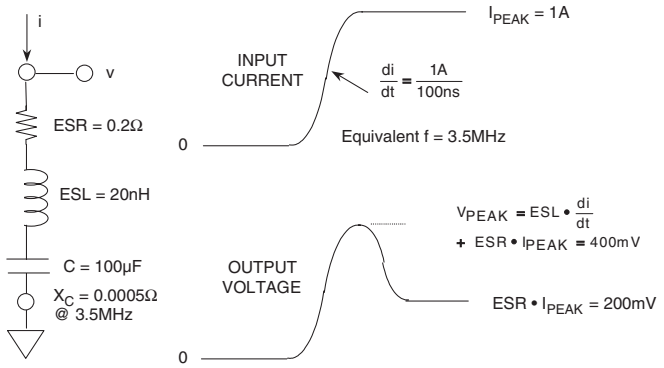

Figure 7-58: Capacitor equivalent circuit and response to input current pulse

The fast-rising edge of the current waveform shown results in an initial voltage peak across the capacitor, which is proportional to the ESL. After the initial transient, the voltage settles down to a longer duration level which is proportional to the ESR of the capacitor. Thus the ESL determines how effective a filter the capacitor is for the fastest components of the current signal, and the ESR is important for longer time frame components. Note that an overall time frame of a few microseconds (or even less) is relevant here. As things turn out, this means switching frequencies in the 100 kHz to 1 MHz range. Unfortunately, however, this happens to be the region where most electrolytic types begin to perform poorly.

All electrolytics will display impedance curves similar in general shape to that of Figure 7-59. In a practical capacitor, at frequencies below about 10 kHz the net impedance seen at the terminals is almost purely capacitive (C region). At intermediate frequencies, the net impedance is determined by ESR, for example

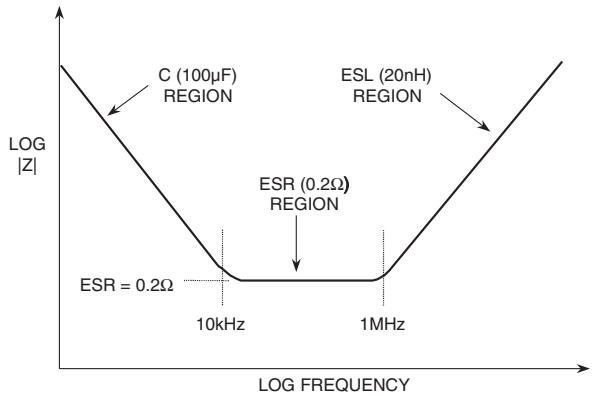

Figure 7-59: Electrolytic capacitor impedance versus frequency