chip caps have an operating frequency range to 1 GHz. For high frequency applications, a useful selection can be ensured by selecting a value that has a self-resonant frequency *above* the highest frequency of interest.

The capacitor model and waveforms of Figure 7-58 illustrate how the various parasitic model elements become dominant, dependent upon the operating frequency. Assume an input current pulse changing from 0 to 1 A in 100 ns, as noted in the figure, and consider what voltage will be developed across the capacitor.

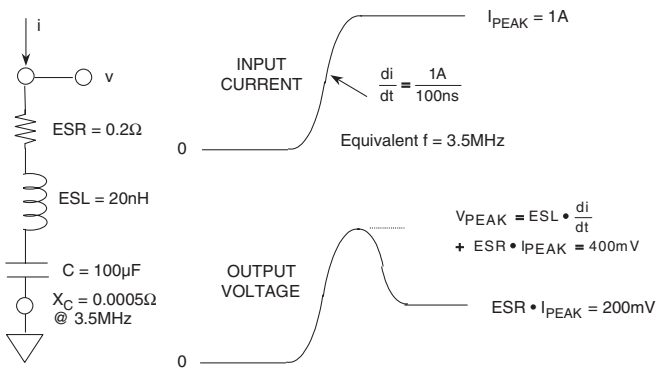


Figure 7-58: Capacitor equivalent circuit and response to input current pulse

The fast-rising edge of the current waveform shown results in an initial voltage peak across the capacitor, which is proportional to the ESL. After the initial transient, the voltage settles down to a longer duration level which is proportional to the ESR of the capacitor. Thus the ESL determines how effective a filter the capacitor is for the fastest components of the current signal, and the ESR is important for longer time frame components. Note that an overall time frame of a few microseconds (or even less) is relevant here. As things turn out, this means switching frequencies in the 100 kHz to 1 MHz range. Unfortunately, however, this happens to be the region where most electrolytic types begin to perform poorly.

All electrolytics will display impedance curves similar in general shape to that of Figure 7-59. In a practical capacitor, at frequencies below about 10 kHz the net impedance seen at the terminals is almost purely capacitive (C region). At intermediate frequencies, the net impedance is determined by ESR, for example

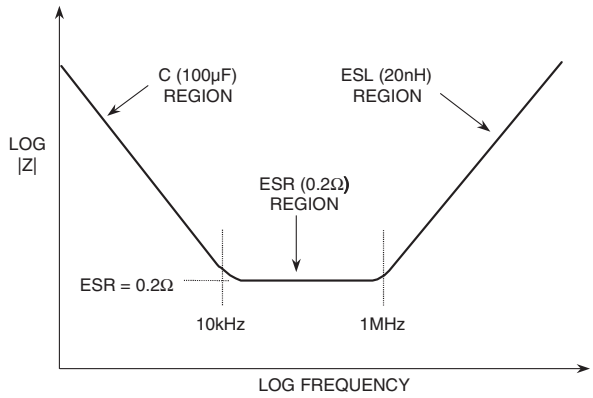


Figure 7-59: Electrolytic capacitor impedance versus frequency

about 0.1 Ω to 0.5 Ω at ~125 kHz, for several types (ESR region). Above about several hundred kHz to 1 MHz these capacitor types become inductive, with net impedance rising (ESL region).

The minimum impedance within the 10 kHz – 1 MHz range will vary with the magnitude of the capacitor's ESR. This is the primary reason why ESR is the most critical item in determining a given capacitor's effectiveness as a switching supply filter element. Higher up in frequency, the inductive region will vary with ESL (which in turn is also strongly affected by package style). It should go without saying that a wideband impedance plot for a capacitor being considered for a filter application will go a long way towards predicting its potential value, as well as for comparing one type against another.

It should be understood that all real-world capacitors have some finite ESR. While it is usually desirable for filter capacitors to possess low ESR, this isn't always so. In some cases, the ESR may actually be helpful in reducing resonance peaks in filters, by supplying "free" damping. For example, in most electrolytic types, a nominally flat broad series resonance region can be noted in an impedance versus frequency plot. This occurs where |Z| falls to a minimum level, nominally equal to the capacitor's ESR at that frequency. This low Q resonance can generally be noted to cover a relatively wide frequency range of several octaves. Contrasted to the high Q sharp resonances of film and ceramic caps, electrolytic's low Q behavior can be useful in controlling resonant peaks.

Ferrites

A second important filter element is the inductor, available in various forms. The use of *ferrite* core materials is prevalent in inductors most practical for power supply filtering. Regarding inductors, ferrites, which are nonconductive ceramics manufactured from the oxides of nickel, zinc, manganese, and so forth., are extremely useful in power supply filters (see Reference 12). Ferrites can act as either inductors or resistors, dependent upon their construction and the frequency range. At low frequencies (<100 kHz), inductive ferrites are useful in low-pass LC filters. At higher frequencies, ferrites become resistive, which can be an important characteristic in high-frequency filters. Again, exact behavior is a function of the specifics. Ferrite impedance depends on material, operating frequency range, dc bias current, number of turns, size, shape, and temperature. Figure 7-60 summarizes a number of ferrite characteristics.

- Ferrites Good for Frequencies Above 25kHz
- Many Sizes / Shapes Available Including Leaded "Resistor Style"
- Ferrite Impedance at High Frequencies Primarily Resistive — Ideal for HF Filtering
- Low DC Loss: Resistance of Wire Passing Through Ferrite is Very Low
- High Saturation Current Versions Available
- Choice Depends Upon:
  - Source and Frequency of Interference
  - Impedance Required at Interference Frequency
  - Environmental: Temperature, AC and DC Field Strength, Size and Space Available
- Always Test the Design

Figure 7-60: A summary of ferrite characteristics

Several ferrite manufacturers offer a wide selection of ferrite materials from which to choose, as well as a variety of packaging styles for the finished network (see References 13 and 14). A simple form is the *bead* of ferrite material, a cylinder of the ferrite which is simply slipped over the power supply lead to the decoupled stage. Alternately, the *leaded ferrite bead* is the same bead, premounted on a length of wire and

used as a component (see Reference 14). More complex beads offer multiple holes through the cylinder for increased decoupling, plus other variations. Surface-mount beads are also available. PSpice models of Fair-Rite ferrites are available, allowing ferrite impedance estimations (see Reference 15). The models match measured rather than theoretical impedances.

Selecting the proper ferrite is not straightforward. A ferrite's impedance is dependent upon a number of interdependent variables, and is difficult to quantify analytically. However, knowing the following system characteristics will make selection easier. First, determine the frequency range of the noise to be filtered. Second, the expected temperature range of the filter should be known, as ferrite impedance varies with temperature. Third, the dc current flowing through the ferrite must be known, to ensure that the ferrite does not saturate. Although models and other analytical tools may prove useful, the general guidelines given above, coupled with actual filter experimentation connected under system load conditions, should lead to a proper ferrite selection.

Card Entry Filter

Using proper component selection, low and high frequency band filters can be designed to smooth a noisy switching supply output to produce an *analog ready* supply. It is most practical to do this over two (and sometimes more) stages, each stage optimized for a range of frequencies.

A basic stage can be used to carry the entire load current, and filter noise by 60 dB or more up to a 1 MHz–10 MHz range. Figure 7-61 illustrates this type of filter, which is used as a *card entry filter,* providing broadband filtering for all power entering a PC card.

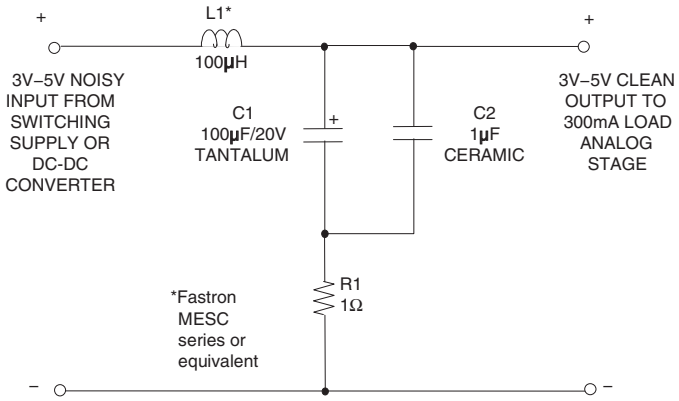


Figure 7-61: A card-entry filter is useful for low-medium frequency power line noise filtering in analog systems

In this filter, L1 and C1 perform the primary filtering, which provides a corner frequency of about 1.6 kHz. With the corner thus placed well below typical switching frequencies, the circuit can have good attenuation up to 1 MHZ, where the typical attenuation is on the order of 60 dB. At higher frequencies parasitics limit performance, and a second filter stage will be more useful.

The ultimate level of performance available from this filter will be related to the components used within it. L1 should be derated for the operating current, thus for 300 mA loads it is a 1 A type. The specified L1 choke has a typical DCR of 0.65 Ω, for low drop across the filter (see Reference 16). C1 can be either a tantalum

or an aluminum electrolytic, with moderately low ESR. For current levels lower than 300 mA, L1 can be proportionally downsized, saving space. The resistor R1 provides damping for the LC filter, to prevent possible ringing. R1 can be reduced or even possibly eliminated, if the ESR of C1 provides a comparable impedance.

While the example shown is a single-supply configuration, obviously the same filter concepts apply for dual supplies.

Rail Bypass/Distribution Filter

A complement to the card-entry filter is the rail-bypass filter scheme of Figure 7-62. When operating from relatively clean power supplies, the heavy noise filtering of the card entry filter may not be necessary. However, some sort of low frequency bypassing with appreciable energy storage is almost always good, and this is especially true if high currents are being delivered by the stages under power.

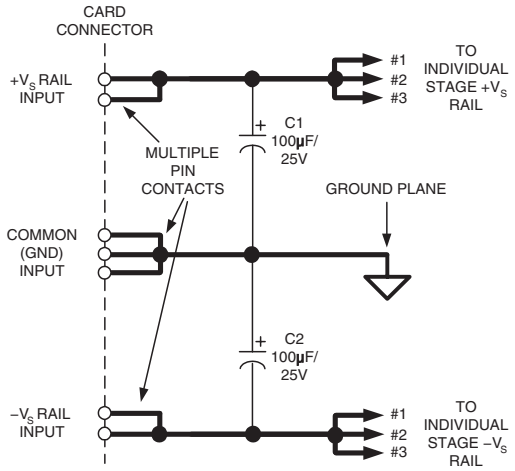


Figure 7-62: Dual-supply low frequency rail bypass/distribution filter

In such cases, some lumped low frequency bypassing is appropriate on the card. Although these energy storage filters need not be immediately adjacent to the ICs they serve, they should be within a few inches. This type of bypassing scheme should be considered a minimum for powering any analog circuit. The exact capacitor values aren't critical, and can vary appreciably. The most important thing is to avoid leaving them out.

The circuit shown uses C1 and C2 as these bypasses in a dual-rail system. Note that multiple card contacts are recommended for the I/O pins, especially ground connection. From the capacitors outward, supply rail traces are distributed to each stage as shown, in "star" distribution fashion. Note: while this is the optimum method to minimize inter-stage crosstalk, in practice some degree of "daisy chaining" is often difficult to avoid. A prudent designer should therefore carefully consider common supply currents effects in designing these PCB distribution paths.

Wider than normal traces are recommended for these supply rails, especially those carrying appreciable current. If the current levels are in the ampere region, then star-type supply distribution with ultrawide traces should be considered mandatory. In extreme cases, a dedicated power plane can be used. The impedance of the ground return path is minimized by the use of a ground plane.

Local High Frequency Bypass/Decoupling

At each individual analog stage, further local, high-frequency-only filtering is used. With this technique, used in conjunction with either the card-entry filter or the low frequency bypassing network, such smaller and simpler local filter stages provide optimum high frequency decoupling. *These stages are provided directly at the power pins, of* all *individual analog stages*.

Figure 7-63 shows this technique, in both correct (left) as well as incorrect example implementations (right). In the left example, a typical 0.1 µF chip ceramic capacitor goes directly to the opposite PCB side ground plane, by virtue of the via, and on to the IC's GND pin by a second via. In contrast, the less desirable setup at the right adds additional PCB trace inductance in the ground path of the decoupling cap, reducing effectiveness.

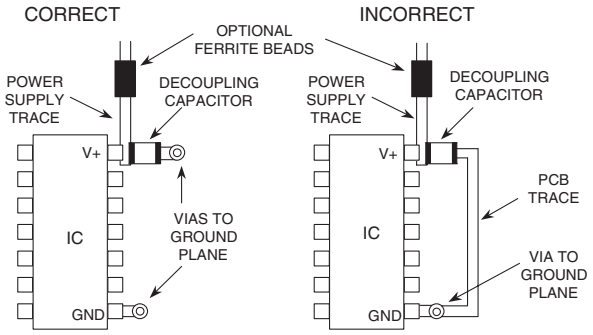


Figure 7-63: Localized high frequency supply filter(s) provides optimum filtering and decoupling via short low-inductance path (ground plane)

The general technique is shown here as suitable for a single-rail power supply, but the concept obviously extends to dual rail systems. Note: if the decoupled IC in question is an op amp, the GND pin shown is the $-V_S$ pin. For dual supply op amp uses, there is no op amp GND pin per se, so the dual decoupling networks should go directly to the ground plane when used, or other local ground.

All high frequency (i.e., ≥10 MHz) ICs should use a bypassing scheme similar to Figure 7-63 for best performance. Trying to operate op amps and other high performance ICs without local bypassing is almost always folly. It *may* be possible in a few circumstances, *if* the circuitry is strictly micropower in nature, and the gain-bandwidth in the kHz range. To put things into an overall perspective however, note that a pair of 0.1 µF ceramic bypass caps cost less than 25 cents. Hardly a worthy saving compared to the potential grief and lost time of troubleshooting a system without bypassing.

In contrast, the ferrite beads aren't 100% necessary, but they will add extra HF noise isolation and decoupling, which is often desirable. Possible caveats here would be to verify that the beads never saturate, when the op amps are handling high currents.

Note that with some ferrites, even before full saturation occurs, some beads can be nonlinear, so if a power stage is required to operate with a low distortion output, this should also be lab checked.

Figure 7-64 summarizes the previous points of this section regarding power supply conditioning techniques for op amp circuitry.

- Use Proper Layout and Grounding Techniques
- At HF Local Decoupling at IC Power Pins is Mandatory
- At HF Ground Planes are Mandatory
- External LC Filters Very Effective in Reducing Ripple
- Low ESR/ESL Capacitors Give Best Results
- Parallel Caps Lower ESR/ESL and Increase C
- Linear Post Regulation Effective for Noise Reduction and Best Regulation
- Completely Analytical Approach Difficult
  - Prototyping Required for Optimum Results

Once Design is Final, Don't Switch Vendors or Substitute Parts
  - Without First Verifying Performance within the Circuit

Figure 7-64: A summary of power supply conditioning techniques for high performance op amp circuitry

References: Op Amp Power Supply Systems

1. Walt Jung, "References and Low Dropout Linear Regulators," Section 2 within Walt Kester, Ed., **Practical Design Techniques for Power and Thermal Management**, Analog Devices, Inc., 1998, ISBN 0-916550-19-2.
2. Paul Brokaw, "A Simple Three-Terminal IC Bandgap Voltage Reference," **IEEE Journal of Solid-State Circuits**, Vol. SC-9, December, 1974.
3. Frank Goodenough, "Vertical-PNP-Based Monolithic LDO Regulator Sports Advanced Features," **Electronic Design**, May 13, 1996.
4. Frank Goodenough, "Low Dropout Regulators Get Application Specific," **Electronic Design**, May 13, 1996.
5. Walt Kester, Brian Erisman, Gurgit Thandi, "Switched Capacitor Voltage Converters," Section 4 within Walt Kester, Editor, **Practical Design Techniques for Power and Thermal Management**, Analog Devices, Inc., 1998, ISBN 0-916550-19-2.
6. Walt Jung, Walt Kester, Bill Chesnut, "Power Supply Noise Reduction and Filtering," portion of Section 8 within Walt Kester, Editor, **Practical Design Techniques for Power and Thermal Management**, Analog Devices, Inc., 1998, ISBN 0-916550-19-2.
7. **Tantalum Electrolytic and Ceramic Capacitor Families**, Kemet Electronics, Box 5928, Greenville, SC, 29606, 803-963-6300.
8. Type HFQ Aluminum Electrolytic Capacitor and Type V Stacked Polyester Film Capacitor, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, 201-348-7000.
9. **OS-CON Aluminum Electrolytic Capacitor Technical Book**, Sanyo, 3333 Sanyo Road, Forrest City, AK, 72335, 501-633-6634.
10. Ian Clelland, "Metallized Polyester Film Capacitor Fills High Frequency Switcher Needs," **PCIM**, June, 1992.
11. Type 5MC Metallized Polycarbonate Capacitor, Electronic Concepts, Inc., Box 1278, Eatontown, NJ, 07724, 908-542-7880.
12. Henry W. Ott, **Noise Reduction Techniques in Electronic Systems, 2nd Edition**, John Wiley, Inc., 1988, ISBN: 0-471-85068-3.
13. **Fair-Rite Linear Ferrites Catalog**, Fair-Rite Products, Box J, Wallkill, NY, 12886, 914-895-2055.
14. Type EXCEL leaded ferrite bead EMI filter, and Type EXC L leadless ferrite bead, Panasonic, 2 Panasonic Way, Secaucus, NJ, 07094, 201-348-7000.
15. Steve Hageman, "Use Ferrite Bead Models to Analyze EMI Suppression," **The Design Center Source,** MicroSim Newsletter**,** January, 1995.
16. "MESC series RFI suppression chokes," FASTRON GmbH, Zum Kaiserblick 25, 83620 Feldkirchen-Westerham, Germany, www.fastron.de.

This page intentionally left blank

SECTION 7-4

Op Amp Protection

Walt Jung, Walt Kester, James Bryant, Joe Buxton, Wes Freeman

Frequently, op amps and other analog ICs require protection against destructive potentials at their input and output terminals. One basic reason behind this is that these ICs are by nature relatively fragile components. Although designed to be as robust as possible *for normal signals*, there are nevertheless certain application and/or handling conditions where they can see voltage transients beyond their ratings. This situation can occur for either of two instances. The first of these is *in-circuit,* that is, operating within an application circuit. The second instance is *out-of-circuit,* which might be at anytime after receipt from a supplier, but prior to final assembly and mounting of the IC. In either case, under over-voltage conditions, it is a basic fact of life that unless the designer limits the fault currents at the input (or possibly output) of the IC, it can be damaged or destroyed.

So, obviously, the designer should fully understand all of the fault mechanisms internal to those ICs that may require protection. This then allows design of networks that can protect the in-circuit IC throughout its lifetime, without undue compromise of speed, precision, and so forth. Or, for the out-of-circuit IC, it can help define proper protective handling procedures until it reaches its final destination. This section of the chapter examines a variety of protection schemes to ensure adequate protection for op amps and other analog ICs for in-circuit applications, as well as for out-of-circuit environments.

In-Circuit Overvoltage Protection

There are many common cases that stress op amps and other analog ICs at the input, while operating within an application, i.e., in-circuit. Since these ICs must often interface with the outside world, this may entail handling voltages exceeding their absolute maximum ratings. For example, sensors are often placed in environments where a fault condition can expose the circuit to a dangerously high voltage. With the sensor connected to a signal processing amplifier, the input then sees excessive voltages during a fault.

General Input Common-Mode Limitations

Whenever an op amp input common-mode (CM) voltage goes outside its supply range, the op amp can be damaged, even if the supplies are turned off. Accordingly, the absolute maximum input ratings of almost all op amps limits the greatest applied voltage to a level equal to the positive and negative supply voltage, plus about 0.3 V beyond these voltages (i.e., $+V_S + 0.3$ V, or $-V_S - 0.3$ V). While some exceptions to this general rule might exist it is important to note this: *Most IC op amps require input protection when over-voltage of more than 0.3 V beyond the rails occurs.*

A safe operating rule is to always keep the applied op amp CM voltage between the rail limits. Here, "safe" implies prevention of outright IC destruction. As will be seen later, there are also intermediate "danger-zone" CM conditions between the rails with certain op amps, which can invoke dangerous (but not necessarily destructive) behavior.

Speaking generally, it is important to note that almost *any* op amp input will break down, given sufficient overvoltage to the positive or negative rail. Under breakdown conditions high and uncontrolled current can flow, so the danger is obvious. The exact breakdown voltage is entirely dependent on the individual op amp input stage. It may be a 0.6 V diode drop, or a process-related breakdown of 50 V or more. In many cases, overvoltage stress can result in currents over 100 mA, which destroys a part almost instantly.

Therefore, unless otherwise stated on the data sheet, op amp input fault current should be limited to ≤5 mA to avoid damage. This is a conservative rule of thumb, based on metal trace widths in a typical op amp input. Higher levels of current can cause *metal migration*, a cumulative effect, which, if sustained, eventually leads to an open trace. Should a migration situation be present, failure may only appear after a long time due to multiple overvoltages, a very difficult failure to identify. So, even though an amplifier may appear to withstand overvoltage currents well above 5 mA for a short time period, it is important to limit the current to 5 mA (or preferably less) for long term reliability.

Figure 7-65 illustrates an external, general-purpose op amp CM protection circuit. The basis of this scheme is the use of Schottky diodes D1 and D2, plus an external current limiting resistor, R_{LIMIT}. With appropriate selection of these parts, input protection for a great many op amps can be ensured. Note that an op amp may also have *internal* protection diodes to the supplies (as shown) which conduct at about 0.6 V forward drop above or below the respective rails. In this case however, the external Schottky diodes effectively parallel any internal diodes, so the internal units never reach their threshold. Diverting fault currents externally eliminates potential stress, protecting the op amp.

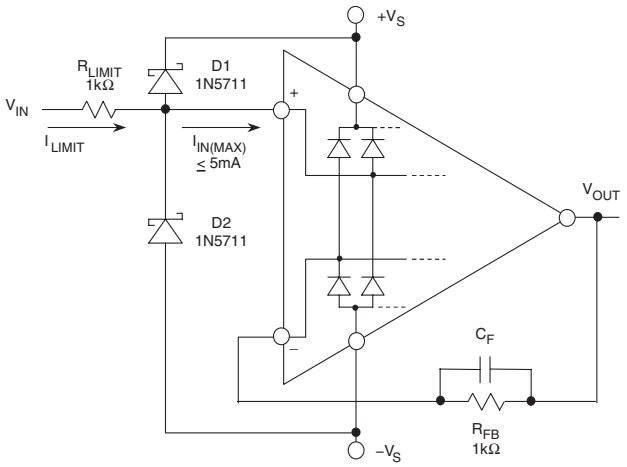


Figure 7-65: A general-purpose op amp CM overvoltage protection network using Schottky clamp diodes with current limit resistance

The external diodes also allow other degrees of freedom, some not so obvious. For example, if fault current is allowed to flow in the op amp, R_{LIMIT} must then be chosen so that the maximum current is no more than 5 mA for the worst case V_{IN}. This criterion can result in rather large R_{LIMIT} values, and the associated increase in noise and offset voltage may not be acceptable. For instance, to protect against a V_{IN} of 100 V with the 5 mA criterion, R_{LIMIT} must be ≥20 kΩ. However with external Schottky clamping diodes, this allows R_{LIMIT} to be governed by the maximum allowable D1-D2 current, which can be larger than 5 mA. However, care must be used here, for at very high currents the Schottky diode drop may exceed 0.6 V, possibly activating internal op amp diodes.

It is very useful to keep the R_{LIMIT} value as low as possible, to minimize offset and noise errors. R_{LIMIT}, in series with the op amp input, produces a bias-current-proportional voltage drop. Left uncorrected, this voltage appears as an increase in the circuit's offset voltage. Thus for op amps where the bias currents are moderate and approximately equal (most bipolar types), compensation resistor R_{FB} balances the dc effect, and minimizes this error. For low bias current op amps (Ib ≤10 nA, or FET types) it is likely R_{FB} won't be necessary. To minimize noise associated with R_{FB}, bypass it with a capacitor, C_F.

Clamping Diode Leakage

For obvious reasons, it is critical that diodes used for protective clamping at an op amp input have a leakage sufficiently low to not interfere with the bias level of the application.

Figure 7-66 illustrates how some well-known diodes differ in terms of leakage current, as a function of the reverse bias voltage, Vbias.

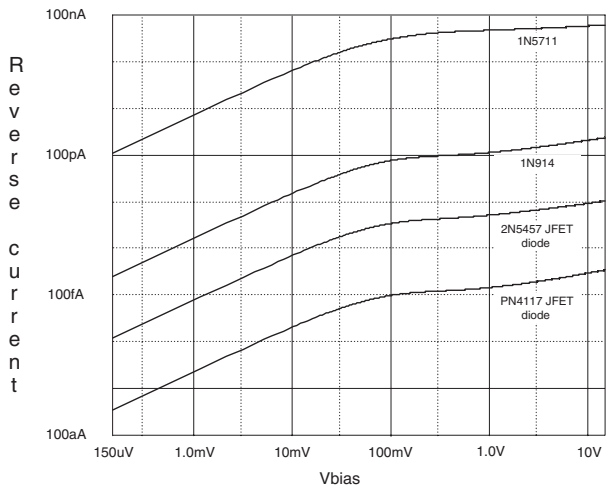


Figure 7-66: Reverse bias current characteristics for diodes useful in protective clamping networks (PSpice simulation)

In this chart, a 25°C simulation using PSpice diode models, it is easy to see that not only is the diode type critical, so is the reverse bias. The 1N5711 Schottky type for example, has a leakage of nearly 100 nA at a reverse bias of 15 V, as it would typically be used with a ±15 V powered op amp. With this level of leakage, such diodes will only be useful with op amps with bias currents of several µA. For protection of appreciably lower bias current op amps (particularly most FET input devices) much lower leakage is necessary.

As the data of Figure 7-66 shows, not only does selecting a better diode help control leakage current, but operating it at a low bias voltage condition reduces leakage substantially. For example, while an ordinary 1N914 or 1N4148 diode may have 200 pA of leakage at 15 V, this is reduced to slightly more than a pA with bias controlled to 1 mV. But there is a caveat here. When used in a high impedance clamp circuit, glass diodes such as the 1N914/1N4148 families should either be shielded from incident light, or use opaque packages. This is necessary to minimize parasitic photocurrent from the surrounding light, which effectively appears as diode leakage current.

Specialty diodes with much lower leakage are also available, such as diode-connected FET devices characterized as protection diodes (see DPAD series of Reference 2). Within the data of Figure 7-66, the 2N5457 is a general purpose JFET, and the 2N4117/PN4117 family consists of parts designed for low current levels. Other low leakage and specialty diodes are described in References 3 and 4.

A Flexible Voltage Follower Protection Circuit

Of course, it isn't a simple matter to effectively apply protective clamping to op amp inputs, while reducing diode bias level to a sub-mV level.

The circuit of Figure 7-67 shows low leakage input clamping and other means used with a follower connected FET op amp, with protection at input and output, for both power on or off conditions.

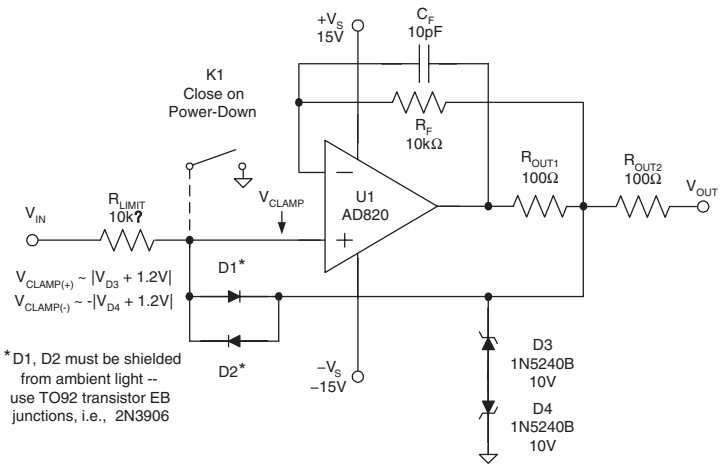


Figure 7-67: Bootstrapping the D1-D2 protection network reduces diode leakage to negligible levels, and is voltage-programmable for clamp level.

Disregarding the various diodes momentarily, this circuit is an output-current-limited voltage follower. With the addition of diodes D1-D2 and D3-D4, it has both a voltage-limited output, and an overvoltage protected input. Operating below the voltage threshold of output series-connected zener diodes D3-D4, the circuit behaves as a precision voltage follower. Under normal follower operation, that is at input/output voltages $< | V_Z + 0.6 |$ volts (where V_Z is the breakdown voltage of D3 or D4), diodes D1-D2 see only the combined offset and CM voltage errors of U1 as bias voltage. This reduces the D1-D2 leakage to very low levels, consistent with the pA level bias current of a FET input op amp. Note that D1-D2 *must* be prevented from photoconduction, and one direct means of this is to use opaque package diodes, such as the 2N3906 EB junctions discussed by Pease (see References 3 and 4). If 1N914s are used they must be light shielded. In either case, bootstrapping greatly reduces the effective D1-D2 leakage.

For input/output voltage levels greater than $V_Z + 0.6$ V, zener diodes D3-D4 break down. This action clamps both the V_{OUT} output node and the V_{CLAMP} node via D1-D2. The input of the op amp is clamped to either polarity of the two input levels of V_{CLAMP}, as indicated within the figure. Under clamp conditions, input voltage V_{IN} can rise to levels beyond the supply rails of U1 without harm, with excess current limited by R_{LIMIT}. If sustained high-level (~100 V) inputs will be applied, R_{LIMIT} should be rated as a 1–2W (or fusible) type.

This circuit has very good dc characteristics, due to the fact that the clamping network is bootstrapped. This produces very low input/output errors below the V_{CLAMP} threshold (consistent with the op amp specifications, of course). Note that this bootstrapping has ac benefits as well, as it reduces the D1-D2 capacitance seen by the source. While the ~100 pF capacitance of D3-D4 might cause a loading problem with some op amps, this is mitigated by the isolating effect of R_{OUT1}, plus the feedback compensation of C_F. Both R_{OUT1} and R_{OUT2} protect the op amp output.

The input voltage clamping level is also programmable, and is set by the choice of zener voltage V_Z. This voltage plus 1.2 V should be greater than the maximum input, but below the rail voltage, as summarized in the figure. The example uses 10 V ±5% zener diodes, so input clamping typically will occur at ±11.2 V, allowing ±10 V swings.

An important caveat to the above is that it applies for *power-on* conditions. With *power-off*, D1–D4 still clamp to the noted levels, but this now produces a condition whereby the U1 input and output voltage can exceed the rails.

Note that this could be dangerous, for a given U1 device. If so, an optional and simple means towards providing a lower, safe clamping level for power off conditions is to use a relay at the V_{CLAMP} node. The contacts are open with power applied, and closed with power absent. With attention paid to an overall PCB layout, this can preserve a pA level bias current of FET op amps used for U1.

CM Over-Voltage Protection Using CMOS Channel Protectors

A much simpler alternative for overvoltage protection is the CMOS *channel protector*. A channel protector is a device in series with the signal path; for example, preceding an op amp input. It provides overvoltage protection by dynamically altering its resistance under fault conditions. Functionally, it has the distinct advantage of affording protection for sensitive components from voltage transients, whether the power supplies are present or not. Representative devices are the ADG465/ADG466/ADG467, which are channel protectors with single, triple, and octal channel options. Because this form of protection works whether supplies are present or not, the devices are ideal for use in applications where input overvoltages are common, or where correct power sequencing can't always be guaranteed. One such example is within hot-insertion rack systems.

An application of a channel protector for overvoltage protection of a precision buffer circuit is shown in Figure 7-68. A single channel device, the ADG465 at U2, is used here at the input of the U1 precision op amp buffer, an OP777.

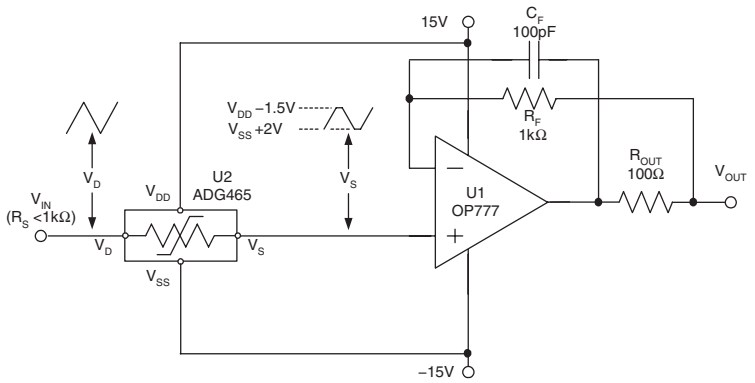


Figure 7-68: Using an ADG465 channel protector IC with a precision buffer offers great simplicity of protection and fail-safe operation during power off.

In operation, a channel protector behaves just like a series resistor of 60 Ω to 80 Ω in normal operation (i.e., nonfault conditions). Consisting of a series connection of multiple P and N MOSFETs, the protector dynamically adjusts channel resistance according to the voltage seen at the V_D terminal. Normal conduction occurs with V_D more than a threshold level above or below the rails, i.e., $(V_{SS} + 2\ V) < V_D < (V_{DD} - 1.5\ V)$. For fault conditions the analog input voltage exceeds this range, causing one of the series MOSFETs to switch off, thus raising the channel resistance to a high level. This clamps the V_S output at one extreme range, either $V_{SS} + 2$ V or $V_{DD} - 1.5$ V, as shown in Figure 7-68.

A major channel protector advantage is the fact that both circuit and signal source protection are provided, in the event of overvoltage or power loss. Although shown here operating from op amp ±15 V supplies, these channel protectors can handle total supplies of up to 40 V. They also can withstand overvoltage inputs from $V_{SS} - 20$ V to $V_{DD} + 20$ V with power on (or ±35 V in the circuit shown). With power off ($V_{DD} = V_{SS} = 0$ V), maximum input voltage is ±35 V. Maximum room temperature channel leakage is 1 nA, making them suitable for op amps and in-amps with bias currents of several nA and up.

Related to the ADG46x series of channel protectors are several *fault-protected multiplexers*, for example the ADG508F/ADG509F, and the ADG438F/ADG439F families. Both the channel protectors and the fault-protected multiplexers are low power devices, and even under fault conditions, their supply current is limited to sub microampere levels. A further advantage of the fault-protected multiplexer devices is that they retain proper channel isolation, even for input conditions of one channel seeing an overvoltage; that is, the remaining channels still function.

CM Overvoltage Protection Using High CM Voltage In Amp

The ultimate simplicity for analog channel overvoltage protection is achieved with resistive input attenuation ahead of a precision op amp. This combination equates to a high voltage capable in amp, such as the AD629, which is able to linearly process differential signals riding upon CM voltages of up to ±270 V. Further, and most important to overvoltage protection considerations, the on-chip resistors afford protection for either common mode or differential voltages of up to ±500 V. All of this is achieved by virtue of a precision laser-trimmed thin-film resistor array and op amp, as shown in Figure 7-69.

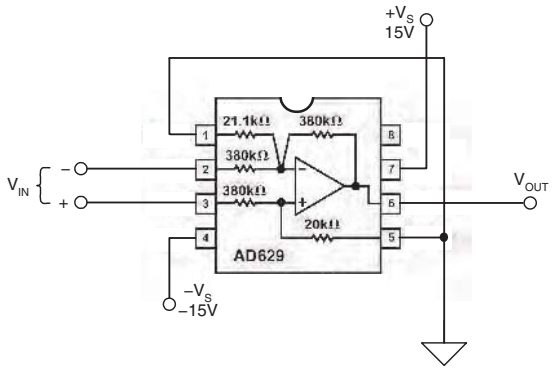


Figure 7-69: The AD629 high voltage in amp IC offers ± 500 V input overvoltage protection, one-component simplicity, and fail-safe power-off operation

Examination of this topology shows that the resistive network around the AD629's precision op amp acts to divide down the applied CM voltage at V_{IN} by a factor of 20/1. The AD629 simultaneously processes the input differential mode signal V_{IN} to a single-ended output referred to a local ground, at a gain factor of unity. Gain errors are no more than ±0.03% or 0.05%, while offset voltage is no more than 0.5 mV or 1 mV (grade dependent). The AD629 operates over a supply range of ±2.5 V to ±18 V.

These factors combine to make the AD629 a simple, one-component choice for the protection of off-card analog inputs that can potentially see dangerous transient voltages. Due to the relatively high resistor values used, protection of the device is also inherent with no power applied, since the input resistors safely limit fault currents. In addition, it offers those operating advantages inherent to an in amp: high CMR (86 dB minimum at 500 Hz), excellent overall dc precision, and the flexibility of simple polarity changes. On the flip side of performance issues, several factors make the AD629's output noise and drift relatively high, if compared to a lower gain in amp configuration such as the AMP03. These are the Johnson noise of the high value resistors, and the high noise gain of the topology (21×). These factors raise the op amp noise and drift along with the resistor noise by a factor higher than typical. Of course, whether or not this is an issue relevant to an individual application will require evaluation on a case-by-case basis.

Inverting Mode Op Amp Protection Schemes

There are some special cases of overvoltage protection requirements that don't fit into the more general CM protection schemes above. Figure 7-70 is one such example, a low bias current FET input op amp I/V converter.

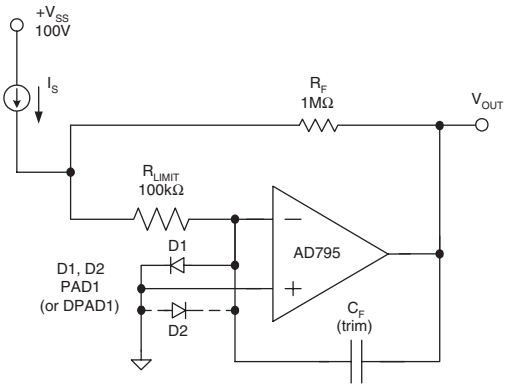


Figure 7-70: A low bias current FET input op amp I/V converter with overvoltage protection network RLIMIT and D1

In this circuit the AD795 1 pA bias current op amp is used as a precision inverter. Some current-source nature signals can originate from a high voltage potential, such as the 100 V V_{SS} level shown. As such, they have the potential of developing fault voltage levels beyond the op amp rails, producing fault current into the op amp well above safe levels. To prevent this, protection resistor R_{LIMIT} is used inside the feedback loop as shown, along with voltage clamp D1 (D2).

For normal signal condition (i.e., I_S ≤10 uA) the op amp's inverting node is very close to ground, with just a tiny voltage drop across R_{LIMIT}. Normal I/V conversion takes place, with gain set by R_F. For protection, D1 is a special low leakage diode, clamping any excess voltage at the (–) node to ~0.6 V, thus protecting the op amp. The value of R_{LIMIT} is chosen to allow a 1 mA max current under fault conditions. Bootstrapping the

D1 (and/or D2) clamp diodes as shown minimizes the normal operating voltage across the inverting node, keeping the diode leakage low (see Figure 7-66). Note that for a positive source voltage as shown, only positive clamping is needed, so just one diode suffices.

Only the lowest leakage diodes (≤1 pA) such as the PAD1 (or the DPAD1 dual) should be used in this circuit. As previously noted, any clamping diode used here should either be shielded from light (or use opaque packaging), to minimize photocurrent from ambient light. Even so, the diode(s) will increase the net input current and shunt capacitance, and feedback compensation C_F will likely be necessary to control response peaking. C_F should be a very low leakage type. Also, with the use of very low input bias current devices such as the AD795, it isn't possible to use the same level of internal protection circuitry as with other ADI op amps. This factor makes the AD795 more sensitive to handling, so ESD precautions should be taken.

Amplifier Output Voltage Phase-Reversal

As alluded to above, there are "gray-area" op amp groups that have anomalous CM voltage zones, falling between the supply rails. As such, protection for these devices cannot be guaranteed by simply ensuring that the inputs stay between the rails—they must additionally stay *entirely* within their rated CM range, for consistent behavior.

Peculiar to some op amps, this misbehavior phenomenon is called *output voltage phase-reversal.* It is seen when one or both of the op amp inputs exceed their allowable input CM voltage range. Note that the inputs may still be well within the extremes of rail voltage, but simply below one specified CM limit. Typically, this is towards the negative range. Phase-reversal is most often associated with JFET and/or BiFET amplifiers, but some bipolar single-supply amplifiers are also susceptible to it.

The Figure 7-71 waveforms illustrate this general phenomenon, with an overdriven voltage follower input on the left, and the resulting output phase-reversal at the right.

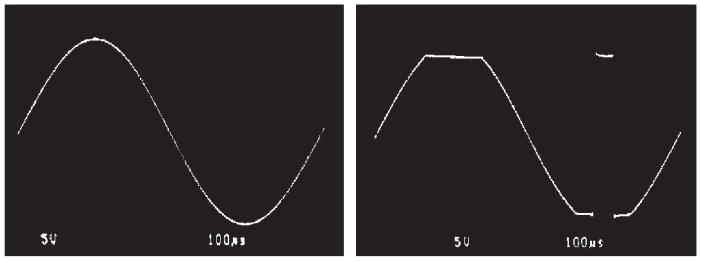


Figure 7-71: An illustration of input overdriving waveform (left) and the resulting output phase-reversal (right), using a JFET input op amp

While the specific details of the internal mechanism may vary with individual op amps, it suffices to say that the output phase-reversal occurs when a critical section of the amplifier front end saturates, causing the input-output sign relationship to temporarily reverse. Under this condition, when the CM range is exceeded, the negative-going input waveform in Figure 7-71 (left) does not continue going more negative in the output waveform, Figure 7-71 (right). Instead, the input-output relationship *phase-reverses*, with the output suddenly going positive, i.e., the spike. It is important to note that this is *not* a latching form of phase-reversal, as the output will once again continue to properly track the input, when the input returns to the CM range. In Figure 7-71, this can be seen in the continuance of the output sine wave, after the positive-going phase-reversal spike settles.

In most applications, this output voltage phase-reversal does no harm to the op amp, nor to the circuit where it is used. Indeed, since it is triggered when the CM limit is exceeded, noninverting stages with appreciable signal gain never see it, since their applied CM voltage is too small.

Note that with inverting applications the output phase-reversal problem is nonexistent, as the CM range isn't exercised. So, although a number of (mostly older) op amps suffer from phase-reversal, it still is rarely a serious problem in system design.

Nevertheless, when and if a phase-reversal susceptible amplifier used in a servo loop application sees excess CM voltage, the effect can be disastrous—it goes **Bang!** So, the best advice is to be forewarned.

An Output Phase-Reversal Do-it-Yourself Test

Since output phase-reversal may not always be fully described on a data sheet, it is quite useful to test for it. This is easily done in the lab, by driving a questionable op amp as a unity-gain follower, from a source impedance (R_{LIMIT}) of ~1kΩ. It is helpful to make this a variable, 1 kΩ –100 kΩ range resistance.

With a low resistance setting (1 kΩ), while bringing the driving signal level slowly up towards the rail limits, observe the amplifier output. If a phase-reversal mechanism is present when the CM limit of the op amp is exceeded, the output will suddenly reverse (see Figure 7-71, right). If there is no phase-reversal present in an amplifier, the output waveform will simply clip at the limits of its swing. It may prove helpful to have a well-behaved op amp available for this test, to serve as a performance reference. One such device is the AD8610.

Note that, in general, some care should be used with this test. Without a series current-limit resistor, if the generator impedance is too low (or level too high), it could possibly damage an internal junction of the op amp under test. So, obviously, caution is best for such cases.

Once a suitable R_{LIMIT} resistance value is found, well-behaved op amps will simply show a smooth, bipolar range, clipped output waveform when overdriven. This clipping will appear more like the *upper (positive swing)* portion of the waveform within Figure 7-71, right.

Fixes For Output Phase–Reversal

An op amp manufacturer might not always give the R_{LIMIT} resistance value appropriate to prevent output phase-reversal. But, the value can be determined empirically with the driving method mentioned above. Most often, the R_{LIMIT} resistor value providing protection against phase-reversal will also safely limit fault current through any input CM clamping diodes. If in doubt, a nominal value of 1 kΩ is a good starting point for testing.

Typically, FET input op amps will need only the current limiting series resistor for protection, but bipolar input devices are best protected with this same limiting resistor, *along with a Schottky diode* (i.e., R_{LIMIT} and D2, of Figure 7-65).

For a more detailed description of the output voltage phase-reversal effect, see References 7 and 8. Figure 7-72 summarizes a number of the key points relating to output voltage phase-reversal.

- Nonlatching Inversion of Transfer Function, Triggered by Exceeding Common-Mode Limit
- Sometimes Occurs in FET and Bipolar (Single-Supply) Op Amps
- Doesn't Harm Amplifier… but *Disastrous* for Servo Systems
- Not Usually Specified on Data Sheet, so Amplifier Must be Checked
- Easily Prevented:
  - All op amps: Limit applied CM voltage by clamping or other means
  - BiFETs: Add series input resistance, R_{LIMIT}
  - Bipolars: R_{LIMIT} and Schottky clamp diode to rail

Figure 7-72: A summary of key points regarding output phase-reversal in FET and bipolar input op amps

Alternately, any of the several previously mentioned CM clamping schemes can be used to prevent output phase-reversal, by setting the clamp voltage to be less than the amplifier CM range limit where phase-reversal occurs. For example, Figure 7-67 would operate to prevent phase-reversal in FET amplifiers susceptible to it, if the negative clamp limit is set so that $V_{CLAMP(-)}$ never exceeds the typical negative CM range of –11 V on a –15 V rail.

For validation of this or any of the previous overvoltage protection schemes, the circuit should be verified on a number of op amps, over a range of conditions as suitable to the final application environment.

Input Differential Protection

The discussions thus far have been on overvoltage common-mode conditions, which is typically associated with forward biasing of PN junctions inherent in the structure of the input stage. There is another equally important aspect of protection against overvoltage, which is that due to excess *differential* voltages. Excessive differential voltage, when applied to certain op amps, can lead to degradation of their operating characteristics.

This degradation is brought about by *reverse junction breakdown,* a second case of undesirable input stage conduction, occurring under conditions of *differential* over-voltage. However, in the case of reverse breakdown of a PN junction, the problem can be more subtle in nature. It is illustrated by the partial op amp input stage in Figure 7-73.

This circuit, applicable to a low noise op amp such as the OP27, is also typical of many others using low noise bipolar transistors for differential pair Q1-Q2. In the absence of any protection, it can be shown that voltages above about 7 V between the two inputs will cause a reverse junction breakdown of either Q2 or Q1 (dependent upon relative polarity). Note that in cases of E-B breakdown, even small reverse currents can cause degradation in both transistor gain and noise (see Reference 6). After E-B breakdown occurs, op amp parameters such as the bias currents and noise may well be out of specification. This is usually permanent, and it can occur gradually and quite subtly, particularly if triggered by transients. For these reasons,

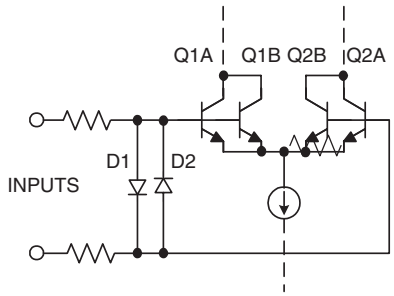


Figure 7-73: An op amp input stage with D1-D2 input differential overvoltage protection network

virtually all low noise op amps, whether NPN or PNP based, utilize protection diodes such as D1-D2 across the inputs. These diodes conduct for applied voltages greater than ±0.6 V, protecting the transistors.

The dotted series resistors function as current limiters (protection for the protection diodes) but aren't used in all cases. For example, the AD797 doesn't have the resistors, simply because they would degrade the part's specified noise of $1\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$. Note: when the resistors are absent internally, some means of external current limiting must be provided, when and if differential overvoltage conditions do occur. Obviously, this is a trade-off situation, so the confidence of full protection must be weighed against the noise degradation. Note that an application circuit itself may provide sufficient resistance in the op amp inputs, such that additional resistance isn't needed.

In applying a low noise bipolar input stage op amp, first check the chosen part's data sheet for internal protection. When necessary, protection diodes D1-D2, if not internal to the op amp, should be added to guarantee prevention of Q1-Q2 E-B breakdown. If differential transients of more than 5 V can be seen by the op amp in the application, the diodes are in order. Ordinary low capacitance diodes will suffice, such as the 1N4148 family. Add current limiting resistors as necessary, to limit diode current to safe levels.

Other IC device junctions, such as base-collector and JFET gate-source junctions don't exhibit the same degradation in performance upon breakdown, and for these the input current should be limited to 5mA, unless the data sheet specifies a different value.

Protecting In Amps Against Overvoltage

From a protection standpoint, instrumentation amplifiers (in amps) are similar in many ways to op amps. Like op amps, their absolute maximum ratings must be observed for both common and differential mode input voltages.

A much simplified schematic of the AD620 in amp is shown in Figure 7-74, showing the input differential transistors and their associated protection parts.

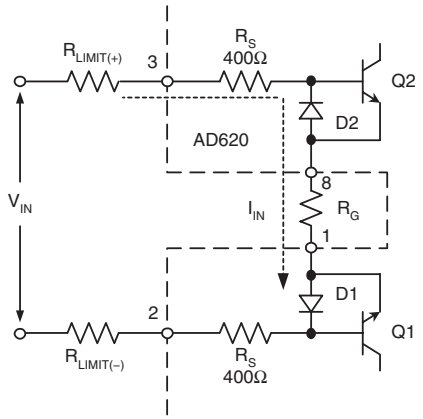


Figure 7-74: The AD620 in amp input internally uses D1-D2 and series resistors R_S for protection (additional protection can be added externally)

An important point, unique to the AD620 device, is the fact that the 400 Ω internal R_S protection resistors are *thin-film types*. Therefore these resistors don't show symptoms of diode-like conduction to the IC substrate (as would be the case were they diffused resistors). Practically, this means that the input ends of these resistors (Pins 3 and 2) can go above or below the supplies. Differential fault currents will be limited by the combination of twice the internal R_S plus the external gain resistance, R_G. Excess applied CM voltages will show current limited by R_S.

In more detail, it can be noted that input transistors Q1 and Q2 have protection diodes D1 and D2 across their base-emitter junctions, to prevent reverse breakdown. For differential voltages, analysis of shows that a fault current, I_{IN}, flows through the external R_{LIMIT} resistors (if present), the internal R_S resistors, the gain-setting resistor R_G, and two diode drops (Q2, D1). For the AD620 topology, R_G varies inversely with gain, and a worst-case (lowest resistance) occurs with the maximum gain of 1000, when R_G is 49.9 Ω. Therefore the lowest total internal path series resistance is about 850 Ω.

For the AD620, any combination of CM and differential input voltages should be limited to levels that limit the input fault current to 20 mA, maximum. A purely differential voltage of 17 V would result in this current level, for the lowest resistance case. For CM voltages that may go beyond either rail, an internal diode not shown in Figure 7-74 conducts, effectively clamping the driven input to either $+V_S$ or $–V_S$ at the R_S inner end. For this overvoltage CM condition, the 400 Ω value of R_S and the excess voltage beyond the rail determines the current level. If, for example, V_{IN} is 23 V with $+V_S$ at 15 V, 8 V appears across R_S, and the 20 mA current rating is reached. Higher fault voltages can be dealt with by adding R_{LIMIT} resistance, to maintain fault current at 20 mA or less.

A more generalized external voltage protection circuit for an in amp like the AD620 is shown in Figure 7-75.

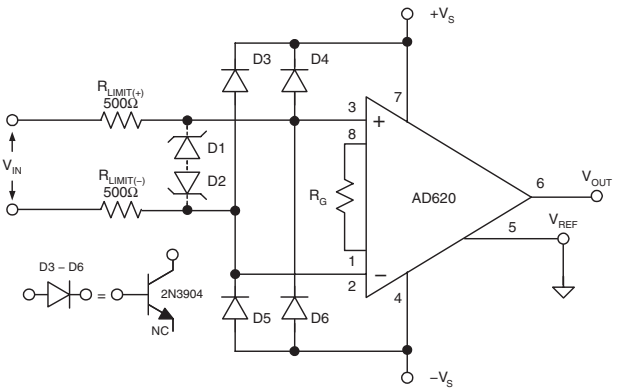


Figure 7-75: A generalized diode protection circuit for the AD620 and other in amps uses D3–D6 for CM clamping and series resistors R_{LIMIT} for protection

In this circuit, low-leakage diodes D3–D6 are used as CM clamps. Since the in amp bias current may be only 1 nA or so (for the AD620), a low leakage diode type is mandatory. As can be noted from the topology, diode bootstrapping isn't possible with this configuration.

It should be noted that not only must the diodes have basically low leakage, they must also maintain low leakage at the highest expected temperature. This suggests either FET type diodes (see Figure 7-66), or the transistor C-B types shown. The R_{LIMIT} resistors are chosen to limit the maximum diode current under fault conditions. If additional *differential* protection is used, either back-back zener or Transzorb clamps can be used, shown as D1-D2. If this is done, leakage of these diodes should be carefully considered.

The protection scheme of Figure 7-75, while effective using appropriate parts, has the downside of being busy for components. A much more simple in amp protection using fault protected devices is shown in Figure 7-76. Although shown with an AD620, this circuit is useful with many other dual-supply in amps with bias currents of 1 nA or more. It uses two-thirds of a triple ADG466 channel-protector for the in amp differential inputs.

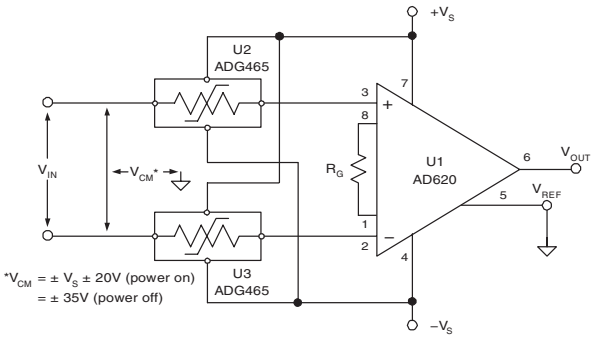


Figure 7-76: A channel protector device (or fault-protected multiplexer) provides protection for dual-supply in amps with a minimum of extra parts

Because the nature of a channel protection device is to turn off as V_{IN} approaches either rail, the scheme of Figure 7-76 doesn't function with rail sensing single-supply in amps. If near-rail operation and protection is required in an in amp application, an alternative method is necessary. Many single-supply in-amps are topologically similar to the two-amplifier in amp circuit which is shown within the dotted box of Figure 7-77.

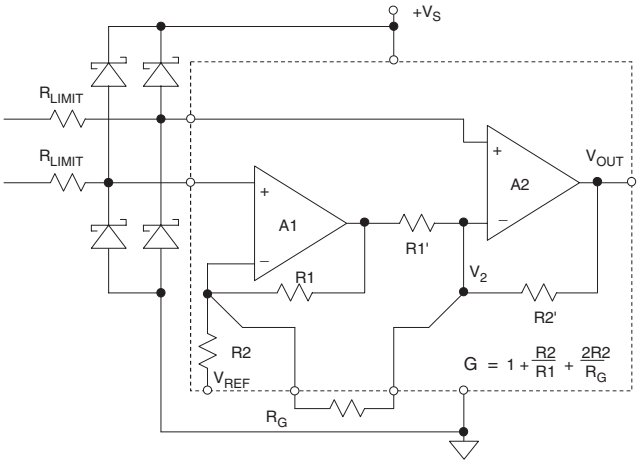


Figure 7-77: Single-supply in amps may or may not require external protection in the form of resistors and clamp diodes—if so, they can be added as shown

In terms of the necessity for externally added protection components, a given in amp may or may not require them. Each case needs to be considered individually. For example, some in amps have clamp diodes as shown, but *internal to the device*. The AD623 is such a part, but it lacks the series resistors, which can be added externally when and if necessary. Note that this approach allows the R_{LIMIT} value to be optimized for protection, with negligible impact on noise for those applications not needing the protection.

Also, some in amp devices have both internal protection resistors *and* clamping diodes, an example here is the AD627. In this device, the internal protection is adequate for transients up to 40 V beyond the supplies (a 20 mA fault current in the internal resistors). For overvoltage levels higher than this, external R_{LIMIT} resistors can be added.

The use of the Schottky diodes as shown at the two inputs is an option for in amp protection. If no clamping is specifically provided internally, then they are applicable. Their use is generally similar to the op amp protection case of Figure 7-65, with comparable caveats as far as leakage. Note that in many cases, due to internal protection networks of modern in amps, these diodes just won't be necessary. But again, there aren't hard rules on this, so always check the data sheet before finalizing an application.

To summarize, Figure 7-78 reviews the major points of the in-circuit overvoltage issues discussed in this section.

If these varied overvoltage precautions for op amps and in amps seem complex, they are. Whenever op amp (or in amp) inputs (and outputs) go outside equipment boundaries, dangerous or destructive things can happen to them. Obviously, for highest reliability these potentially hazardous situations should be anticipated.

Fortunately, most applications are contained entirely within the equipment, and usually see inputs and outputs to/from other ICs on the same power system. Therefore clamping and protection schemes typically aren't necessary for these cases.

- INPUT VOLTAGES MUST NOT EXCEED ABSOLUTE MAXIMUM RATINGS
  (Usually Specified with Respect to Supply Voltages)
- Requires $V_{IN(CM)}$ Stay Within a Range Extending to ≤0.3V Beyond Rails
  ($-V_S-0.3V \geq V_{IN} \leq +V_S+0.3V$)
- IC Input Stage Fault Currents *Must* Be Limited
  (≤ 5mA Unless Otherwise Specified)
- Avoid Reverse-Bias Breakdown in Input Stage Junctions!
- Differential and Common-Mode Ratings Often Differ
- No Two Amplifiers are Exactly the Same
- Watch Out for Output Phase-Reversal in JFET and SS Bipolar Op Amps
- Some ICs Contain *Internal* Input Protection
  - Diode Voltage Clamps, Current Limiting Resistors (or both)
  - Absolute Maximum Ratings Must Still Be Observed

Figure 7-78: A summary of in-circuit overvoltage points

Out-of-Circuit Overvoltage Protection

Linear ICs such as op amps and in amps must also be protected prior to the time they are mounted to a printed circuit board, that is an *out-of-circuit* state. In such a condition, ICs are completely at the mercy of their environment as to what stressful voltage surges they may see. Most often the harmful voltage surges come from *electrostatic discharge,* or, as more commonly referenced, ESD. This is a single, fast, high current transfer of electrostatic charge resulting from one of two conditions. These conditions are:

1) *Direct contact transfer between two objects at different potentials (sometimes called contact discharge)*
2) *A high electrostatic field between two objects when they are in close proximity (sometimes called air discharge)*

The prime sources of static electricity are mostly insulators and are typically synthetic materials, e.g., vinyl or plastic work surfaces, insulated shoes, finished wood chairs, Scotch tape, bubble pack, soldering irons with ungrounded tips, and so forth. Voltage levels generated by these sources can be extremely high since their charge is not readily distributed over their surfaces or conducted to other objects.

The generation of static electricity caused by rubbing two substances together is called the *triboelectric* effect. Some common examples of ordinary acts producing significant ESD voltages are shown in Figure 7-79.

- Walking across a Carpet
  1000V – 1500V
- Walking across a Vinyl Floor
  150V – 250V
- Handling Material Protected by Clear Plastic Covers
  400V – 600V
- Handling Polyethylene Bags
  1000V – 2000V
- Pouring Polyurethane Foam into a Box
  1200V – 1500V
- Note: Above Assumes 60% RH. For Low RH (30%) Voltages Can Be > 10 Times

Figure 7-79: ESD voltages generated by various ordinary circumstances

ICs can be damaged by the high voltages and high peak currents generated by ESD. Precision analog circuits, often featuring very low bias currents, are more susceptible to damage than common digital circuits, because traditional input-protection structures that protect against ESD damage increase input leakage—and thus can't be used.

For the design engineer or technician, the most common manifestation of ESD damage is a catastrophic failure of the IC. However, exposure to ESD can also cause increased leakage or degrade other parameters. If a device appears to not meet a data sheet specification during evaluation, the possibility of ESD damage should be considered. Figure 7-80 outlines some relevant points on ESD induced failures.

- ESD Failure Mechanisms:
  - Dielectric or junction damage
  - Surface charge accumulation
  - Conductor fusing
- ESD Damage Can Cause:
  - Increased leakage
  - Degradation in performance
  - Functional failures of ICs
- ESD Damage is often Cumulative:
  - For example, each ESD "zap" may increase junction damage until, finally, the device fails.

Figure 7-80: Understanding ESD damage

All ESD-sensitive devices are shipped in protective packaging. ICs are usually contained in either conductive foam or antistatic shipping tubes, and the container is then sealed in a static-dissipative plastic bag. The sealed bag is marked with a distinctive sticker, such as in Figure 7-81, which outlines the appropriate handling procedures.

The presence of outside package notices such as those shown in Figure 7-81 is notice to the user that device handling procedures appropriate for ESD protection are necessary.

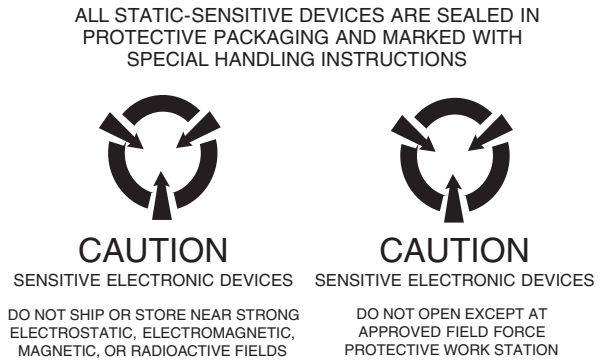
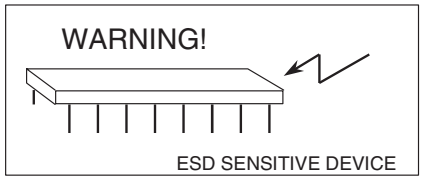


Figure 7-81: Recognizing ESD-sensitive devices by package and labeling

In addition, data sheets for ESD-sensitive ICs generally have a bold statement to that effect, as shown in Figure 7-82.

Once ESD-sensitive devices are identified, protection is relatively easy. Obviously, keeping ICs in their original protective packages as long as possible is a first step. A second step is discharging potentially damaging ESD sources before IC damage occurs. Discharging such voltages can be done quickly and safely, through a high impedance.



CAUTION

ESD (Electrostatic Discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADxxx features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Figure 7-82: ESD data sheet statement for linear ICs

A key component required for ESD-safe IC handling is a workbench with a static-dissipative surface, shown in the workstation of Figure 7-83. The surface is connected to ground through a 1 MΩ resistor, which dissipates any static charge, while protecting the user from electrical ground fault shock hazards. If existing bench tops are nonconductive, a static-dissipative mat should be added, along with the discharge resistor.

Note that the surface of the workbench has a moderately high sheet resistance. It is neither necessary nor desirable to use a low resistance surface (such as a sheet of copper-clad PC board) for the work surface. Remember, a high peak current may flow if a charged IC is discharged through a low impedance. This is precisely what happens when a charged IC contacts a grounded copper clad board. When the same charged IC is placed on the high impedance surface of Figure 7-83, however, the peak current isn't high enough to damage the device.

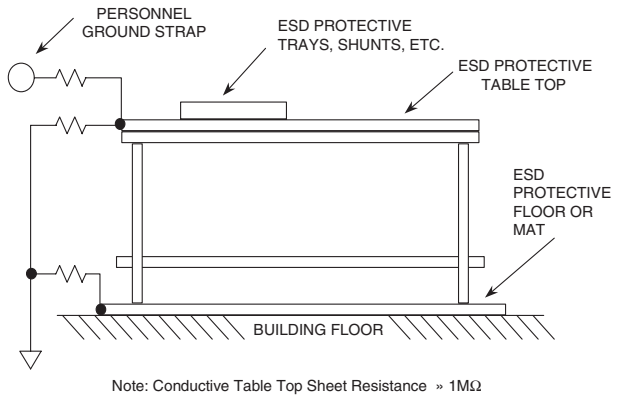


Figure 7-83: A workstation environment suitable for handling ESD-sensitive ICs

Several personnel-handling techniques are keys to minimizing ESD-related damage. At the workstation, a conductive wrist strap is recommended while handling ESD-sensitive devices. The wrist strap ensures that normal tasks, such as peeling tape from packages, won't cause IC damage. Again, a 1 MΩ resistor, from the wrist strap to ground, is required for safety. When building prototype breadboards or assembling PC boards that contain ESD-sensitive ICs, all passive components should be inserted and soldered before the ICs. This minimizes the ESD exposure of the sensitive devices. The soldering iron must, of course, have a grounded tip.

Protecting ICs from ESD requires the participation of both the IC manufacturer and the customer. IC manufacturers have a vested interest in providing the highest possible level of ESD protection for their products. IC circuit designers, process engineers, packaging specialists and others are constantly looking for new and improved circuit designs, processes, and packaging methods to withstand or shunt ESD energy.

A complete ESD protection plan, however, requires more than building ESD protection into ICs. The users of ICs must also provide their employees with the necessary knowledge of and training in ESD handling procedures, so that protection can be built in at all key points along the way, as outlined in Figure 7-84.

Special care should be taken when breadboarding and evaluating ICs. The effects of ESD damage can be cumulative, so repeated mishandling of a device can eventually cause a failure. Inserting and removing ICs from a test socket, storing devices during evaluation, and adding or removing external components on the breadboard should all be done while observing proper ESD precautions. Again, if a device fails during a prototype system development, repeated ESD stress may be the cause.

ANALOG DEVICES:

- Circuit Design and Fabrication

↓ Design and manufacture products with the highest level of ESD
↓ protection consistent with required analog and digital performance.

- Pack and Ship

↓ Pack in static dissipative material. Mark packages with ESD warning.

CUSTOMERS:

- Incoming Inspection

↓ Inspect at grounded workstation. Minimize handling.

- Inventory Control

↓ Store in original ESD-safe packaging. Minimize handling.

- Manufacturing

↓ Deliver to work area in original ESD-safe packaging. Open packages only at
↓ grounded workstation. Package subassemblies in static dissipative packaging.

- Pack and Ship

Pack in static dissipative material if required. Replacement or optional boards may require special attention.

Figure 7-84: ESD protection requires a partner relationship between ADI and the end customer with control at key points

The key word to remember with respect to ESD is *prevention*. There is no way to undo ESD damage, or to compensate for its effects.

ESD Models and Testing

Some applications have higher sensitivity to ESD than others. ICs located on a PC board surrounded by other circuits are generally much less susceptible to ESD damage than circuits that must interface with other PC boards or the outside world. These ICs are generally not specified or guaranteed to meet any particular ESD specification (with the exception of MIL-STD-883 Method 3015 classified devices). A good example of an ESD-sensitive interface is the RS-232 interface port ICs on a computer, which can easily be exposed to excess voltages. In order to guarantee ESD performance for such devices, the test methods and limits must be specified.

A host of test waveforms and specifications have been developed to evaluate the susceptibility of devices to ESD. The three most prominent of these waveforms currently in use for semiconductor or discrete devices are: The Human Body Model (HBM), the Machine Model (MM), and the Charged Device Model (CDM). Each of these models represents a fundamentally different ESD event, consequently, correlation between the test results for these models is minimal.

Since 1996, all electronic equipment sold to or within the European Community must meet Electromechanical Compatibility (EMC) levels as defined in specification IEC1000-4-x. Note that this does not apply to individual ICs, *but to the end equipment.* These standards are defined along with test methods in the various IEC1000 specifications, and are listed in Figure 7-85.

- IEC1000-4 Electromagnetic Compatibility EMC
- IEC1000-4-1 Overview of Immunity Tests
- IEC1000-4-2 Electrostatic Discharge Immunity (ESD)
- IEC1000-4-3 Radiated Radio-Frequency Electromagnetic Field Immunity
- IEC1000-4-4 Electrical Fast Transients (EFT)
- IEC1000-4-5 Lightening Surges
- IEC1000-4-6 Conducted Radio Frequency Disturbances above 9kHz
- Compliance Marking: CE

Figure 7-85: A listing of the IEC standards applicable to ESD specifications and testing procedures

IEC1000-4-2 specifies compliance testing using two coupling methods, *contact discharge* and *air-gap discharge*.

Contact discharge calls for a direct connection to the unit being tested. Air-gap discharge uses a higher test voltage, but does not make direct contact with the unit under test. With air discharge, the discharge gun is moved toward the unit under test, developing an arc across the air gap, hence the term air discharge. This method is influenced by humidity, temperature, barometric pressure, distance and rate of closure of the discharge gun. The contact-discharge method, while less realistic, is more repeatable and is gaining acceptance in preference to the air-gap method.

Although very little energy is contained within an ESD pulse, the extremely fast rise time coupled with high voltages can cause failures in unprotected ICs. Catastrophic destruction can occur immediately as a result of arcing or heating. Even if catastrophic failure does not occur immediately, the device may suffer from parametric degradation, which may result in degraded performance. The cumulative effects of continuous exposure can eventually lead to complete failure.

I-O lines are particularly vulnerable to ESD damage. Simply touching or plugging in an I-O cable can result in a static discharge that can damage or completely destroy the interface product connected to the I-O port (such as RS-232 line drivers and receivers).

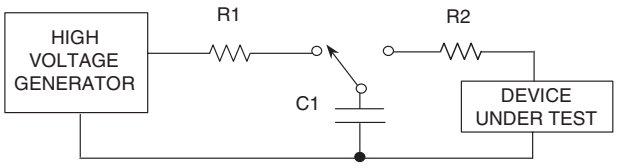
Traditional ESD test methods such as MIL-STD-883B Method 3015.7 do not fully test a product's susceptibility to this type of discharge. This test was intended to test a product's susceptibility to ESD damage during handling. Each pin is tested with respect to all other pins. There are some important differences between the MIL-STD-883B Method 3015.7 test and the IEC test, noted as follows:

1) *The IEC test is much more stringent in terms of discharge energy. The peak current injected is over four times greater.*

2) *The current rise time is significantly faster in the IEC test.*
3) *The IEC test is carried out while power is applied to the device.*

It is possible that ESD discharge could induce latch-up in the device under test. This test is therefore more representative of a real-world I-O discharge where the equipment is operating normally with power applied. For maximum confidence, however, both tests should be performed on interface devices, thus ensuring maximum protection both during handling, and later, during field service.

A comparison of the test circuit values for the IEC1000-4-2 model versus the MIL-STD-883B Method 3015.7 Human Body Model is shown in Figure 7-86.

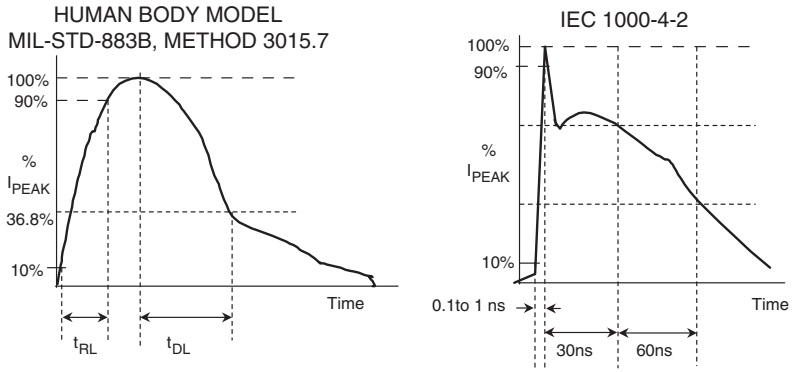


ESD TEST METHOD	R2	C1
Human Body Model MIL STD 883B Method 3015.7	1.5kΩ	100pF
IEC 1000-4-2	330Ω	150pF

NOTE: CONTACT DISCHARG E VOLTAGE SPEC FOR IEC 1000-4-2 IS ±8kV

Figure 7-86: ESD test circuits and values

The ESD waveforms for the MIL-STD-883B, METHOD 3015.7 and IEC 1000-4-2 tests are compared in Figure 7-87, left and right, respectively.



- Voltage : 8 kV
- Peak Current :
  - MIL-883B, Method 3015.7 HBM: 5 A
  - IEC 1000-4-2: 25 A

Figure 7-87: ESD test waveforms

Suitable ESD-protection design measures are relatively easy to incorporate, and most of the overvoltage protection methods already discussed in this section will help.

Additional protection can also be obtained. For RS-232 and RS-485 drivers and receivers, the ADMxxx-E series is supplied with guaranteed 15 kV (HBM) ESD specifications.

For more general uses, the addition of TransZorbs at appropriate places in a system can provide protection against ESD (see References).

Figure 7-88 summarizes the major points about ESD prevention, from both an out-of-circuit as well as an in-circuit perspective.

- Observe all Absolute Maximum Ratings on Data Sheet
- Read ADI AN-397 (See Reference 16)
- Purchase ESD-Specified Digital Interface Devices
  - ADMxxx-E Series of RS-232/RS-485 Drivers/Receivers (See Reference 18)
- Follow General Overvoltage Protection Recommendations
  - Add Series Resistance to Limit Currents
  - Add Zeners or Transient Voltage Suppressors (TVS) for Extra Protection (See Reference 19)

Figure 7-88: A summary of ESD points

References: Op Amp Protection

1. Walt Kester, Wes Freeman, Joe Buxton, "Overvoltage Protection," portion of Section 10 within Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, Inc., 1999, ISBN 0-916550-20-6.
2. Siliconix PAD/JPAD/SSTPAD series Low leakage Pico-Amp Diodes, Vishay/Siliconix, www.vishay.com/brands/siliconix/SSFsglld.html.
3. Bob Pease, "Bounding, Clamping Techniques Improve Circuit Performance," **EDN**, November 10, 1983, p. 277.
4. Bob Pease, "Understanding Diodes and Their Problems," Chapter 6 within **Troubleshooting Analog Circuits**, Butterworth-Heinemann, 1991, ISBN 0-7506-9184-0.
5. Dov Kurz, Avner Cohen, "Bootstrapping Reduces Amplifier Input Capacitance," **EDN**, March 20, 1978.
6. C.D. Motchenbacher, J.A. Connelly, Chapter 5, within **Low Noise Electronic System Design**, John Wiley, 1993.
7. Adolfo Garcia**,** "Operational Amplifier Output Voltage Phase Reversal**,**" Section 11, pp. 1–10 within Walt Kester, Editor, **1992 Amplifier Applications Guide**, Analog Devices, Inc., Norwood, MA, 1992, ISBN 0-916550-10-9.
8. Adolfo Garcia**,** Wes Freeman*,* "Overvoltage Effects On Analog Integrated Circuits," Section 7 within Walt Kester, Editor, **Practical Analog Design Techniques**, Analog Devices, Inc., Norwood, MA, 1995, ISBN 0-916550-16-8.
9. Charles Kitchen, Lew Counts, **A Designer's Guide to Instrumentation Amplifiers**, Analog Devices, Inc., 2000.
10. Walt Kester, Wes Freeman, James Bryant, "Electrostatic Discharge," portion of Section 10 within Walt Kester, Editor, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, Inc., 1999, ISBN 0-916550-20-6.
11. MIL-STD-883 Method 3015, "Electrostatic Discharge Sensitivity Classification." Available from Standardization Document Order Desk, 700 Robbins Ave., Building #4, Section D, Philadelphia, PA, 19111-5094.
12. EIAJ ED-4701 Test Method C-111, "Electrostatic Discharges." Available from the Japan Electronics Bureau, 250 W 34th St., New York NY 10119, Attn.: Tomoko.
13. ESD Association Standard S5.2 for "Electrostatic Discharge (ESD) Sensitivity Testing -Machine Model (MM)-Component Level." Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.
14. ESD Association Draft Standard DS5.3 for "Electrostatic Discharge (ESD) Sensitivity Testing – Charged Device Model (CDM) Component Testing." Available from the ESD Association, Inc., 200 Liberty Plaza, Rome, NY 13440.
15. **ESD Prevention Manual**, Analog Devices, Inc.
16. Niall Lyne, "Electrically Induced Damage to Standard Linear Integrated Circuits: The Most Common Causes and the Associated Fixes to Prevent Reoccurrence," **Analog Devices AN397**.
17. Mike Byrne, "How to Reliably Protect CMOS Circuits Against Power Supply Overvoltaging," **Analog Devices AN311**.
18. Data sheet for **ADM3311E RS-232 Port Transceiver**, Analog Devices, Inc., www.analog.com.
19. TransZorbs are available from General Semiconductor, Inc., 10 Melville Park Road, Melville, NY, 11747-3113, 631-847-3000, www.vishay.com.

This page intentionally left blank

SECTION 7-5

Thermal Considerations

Walt Jung

For reliability reasons, op amp systems handling appreciable power are increasingly called upon to observe *thermal management*. All semiconductors have some specified safe upper limit for junction temperature (T_J), usually on the order of 150°C (sometimes 175°C). Like maximum power supply voltages, maximum junction temperature is a worst-case limitation which shouldn't be exceeded. In conservative designs, it won't be approached by less than an ample safety margin. Note that this is critical, since semiconductor lifetime is inversely related to operating junction temperature. Simply put, the cooler op amps are, the more they can approach their maximum life.

This limitation of power and temperature is basic, and is illustrated by a typical data sheet statement as in Figure 7-89. In this case it is for the AD8017AR, an 8-pin SOIC device.

> *The maximum power that can be safely dissipated by the AD8017 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately +150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.*

Figure 7-89: Maximum power dissipation data sheet statement for the AD8017AR, an ADI thermally-enhanced SOIC packaged device

The maximum power that can be safely dissipated by the AD8017 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated device is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

Tied to these statements are certain conditions of operation, such as the power dissipated by the device, and the package mounting specifics to the printed circuit board (PCB). In the case of the AD8017AR, the part is rated for 1.3 W of power at an ambient of 25°C. This assumes operation of the 8-lead SOIC package on a two-layer PCB with about 4 inches^2 (~2500 mm^2) of 2 oz. copper for heat sinking purposes. Predicting safe operation for the device under other conditions is covered next.

Thermal Basics

The symbol θ is generally used to denote *thermal resistance*. Thermal resistance is in units of °C/watt (°C/W). Unless otherwise specified, it defines the resistance heat encounters transferring from a hot IC junction to the ambient air. It might also be expressed more specifically as θ_{JA}, for *thermal resistance, junction-to-ambient*. θ_{JC} and θ_{CA} are two additional θ forms used. Following is a further explanation.

In general, a device with a thermal resistance θ equal to 100°C/W will exhibit a temperature differential of 100°C for a power dissipation of 1 W, as measured between two reference points. Note that this is a linear relationship, so 1 W of dissipation in this part will produce a 100°C differential (and so on, for other powers). For the AD8017AR example, θ is about 95°C/W, so 1.3 W of dissipation produces about a 124°C junction-to-ambient temperature differential. It is of course this rise in temperature that is used to predict the internal temperature, in order to judge the thermal reliability of a design. With the ambient at 25°C, this allows an internal junction temperature of about 150°C. In practice, most ambient temperatures are above 25°C, so less power can then be handled.

For any power dissipation P (in watts), one can calculate the effective temperature differential (ΔT) in °C as:

$$\Delta T = P \times \theta \qquad \text{Eq. 7-6}$$

where θ is the total applicable thermal resistance.

Figure 7-90 summarizes a number of basic thermal relationships.

- θ = Thermal Resistance (°C/W)
- P = Total Device Power Dissipation (W)
- T = Temperature (°C)
- ΔT = Temperature Differential = $P \times \theta$
- θ_{JA} = Junction-Ambient Thermal Resistance
- θ_{JC} = Junction-Case Thermal Resistance
- θ_{CA} = Case-Ambient Thermal Resistance
- $\theta_{JA} = \theta_{JC} + \theta_{CA}$
- $T_J = T_A + (P \times \theta_{JA})$
- Note: $T_{J(Max)}$ = 150°C (Sometimes 175°C)

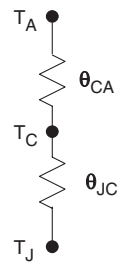


Figure 7-90: Basic thermal relationships

Note that series thermal resistances, such as the two shown in Figure 7-91, model the total thermal resistance path a device may see. Therefore the total θ for calculation purposes is the sum, i.e., $\theta_{JA} = \theta_{JC}$ and θ_{CA}. Given the ambient temperature T_A, P, and θ, then T_J can be calculated. As the relationships signify, to maintain a low T_J, either θ or the power being dissipated (or both) must be kept low. A low ΔT is the key to extending semiconductor lifetimes, as it leads to lower maximum junction temperatures.

In ICs, one temperature reference point is always the device junction, taken to mean the hottest spot inside the chip operating within a given package. The other relevant reference point will be either T_C, the case of the device, or T_A, that of the surrounding air. This leads in turn to the above-mentioned individual thermal resistances, θ_{JC} and θ_{JA}.

Taking the simplest case first, θ_{JA} is the thermal resistance of a given device measured between its *junction* and the *ambient* air. This thermal resistance is most often used with small, relatively low power ICs such as op amps, which often dissipate 1 W or less. Generally, θ_{JA} figures typical of op amps and other small devices are on the order of 90°C/W–100°C/W for a plastic 8-pin DIP package, as well as the better SOIC packages.

It should be clearly understood that these thermal resistances are *highly* package-dependent, as different materials have different degrees of thermal conductivity. As a general rule of thumb, thermal resistance of conductors is analogous to electrical resistances, that is, copper is the best, followed by aluminum, steel, and so on. Thus copper lead frame packages offer the highest performance, i.e., the lowest θ.

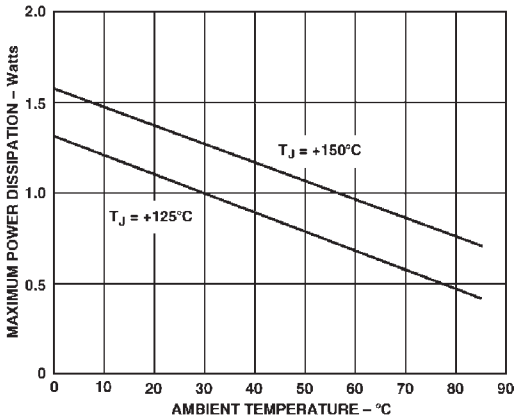


Figure 7-91: Thermal rating curves for AD8017AR op amp

Heat Sinking

By definition, a *heat sink* is an added low thermal resistance device attached to an IC to aid heat removal. A heat sink has additional thermal resistance of its own, θ_{CA}, rated in °C/W. However, most current op amp packages don't easily lend themselves to heat sink attachment (exceptions are older TO99 metal can types). Devices meant for heat sink attachment will often be noted by a θ_{JC} dramatically lower than the θ_{JA}. In this case θ will be composed of more than one component. Thermal impedances add, making a net calculation relatively simple. For example, to compute a net θ_{JA} given a relevant θ_{JC}, the thermal resistance of the heat sink, θ_{CA}, or *case* to *ambient* is added to the θ_{JC} as:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \qquad \text{Eq. 7-7}$$

and the result is the θ_{JA} for that specific circumstance.

More generally however, modern op amps *don't* use commercially available heat sinks. Instead, when significant power needs to be dissipated, such as ≥1 W, low thermal resistance copper PCB traces are used as the heat sink. In such cases, the most useful form of manufacturer data for this heat sinking are the boundary conditions of a sample PCB layout, and the resulting θ_{JA} for those conditions. This is, in fact, the type of specific information supplied for the AD8017AR, as mentioned earlier. Applying this approach, example data illustrating thermal relationships for such conditions is shown by Figure 7-91. These data apply for an AD8017AR mounted to a heat sink with an area of about 4 square inches on a 2-layer, 2-ounce copper PCB.

These curves indicate the maximum power dissipation versus temperature characteristic for the AD8017, for maximum junction temperatures of both 150°C and 125°C. Such curves are often referred to as *derating* curves, since allowable power decreases with ambient temperature.

With the AD8017AR, the proprietary ADI *Thermal Coastline* IC package is used, which allows additional power to be dissipated with no increase in the SO-8 package size. For a $T_{J(max)}$ of 150°C, the upper curve shows the allowable power in this package, which is 1.3 W at an ambient of 25°C. If a more conservative $T_{J(max)}$ of 125°C is used, the lower of the two curves applies.

A performance comparison for an 8-pin standard SOIC and the ADI Thermal Coastline version is shown in Figure 7-92. Note that the Thermal Coastline provides an allowable dissipation at 25°C of 1.3 W, whereas a standard package allows only 0.8 W. In the Thermal Coastline heat transferal is increased, accounting for the package's lower θ_{JA}.

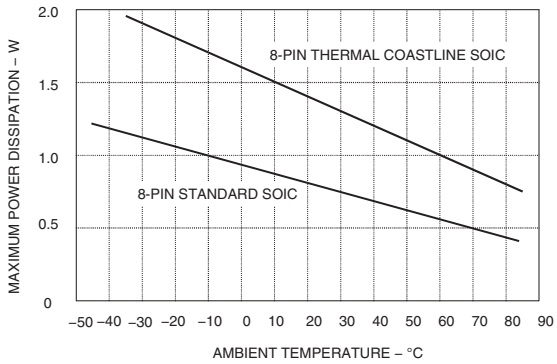


Figure 7-92: Thermal rating curves for standard (lower) and ADI Thermal Coastline (upper) 8-pin SOIC packages

Even higher power dissipation is possible, with the use of IC packages better able to transfer heat from chip to PCB. An example is the AD8016 device, available with two package options rated for 5.5 W and 3.5 W at 25°C, respectively, as shown in Figure 7-93.

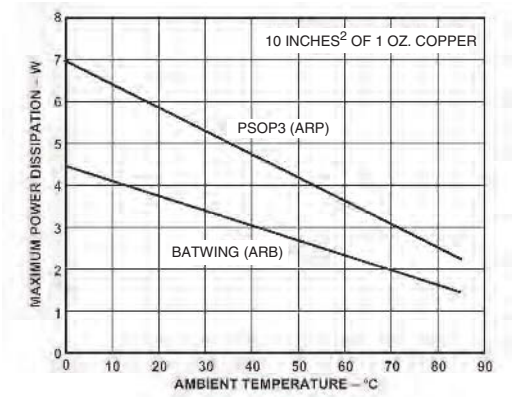


Figure 7-93: Thermal characteristic curves for the AD8016 BATWING (lower) and PSOP3 (upper) packages, for $T_{J(max)}$ equal to 125°C

Taking the higher rated power option, the AD8016ARP PSOP3 package, when used with a 10-inch^2 1 oz. heat sink plane, the combination is able to handle up to 3 W of power at an ambient of 70°C, as noted by the upper curve. This corresponds to a θ_{JA} of 18°C/W, which in this case applies for a maximum junction temperature of 125°C.

The reason the PSOP3 version of the AD8016 is better able to handle power lies with the use of a large area copper slug. Internally, the IC die rest directly on this slug, with the bottom surface exposed as shown in Figure 7-94. The intent is that this surface be soldered directly to a copper plane of the PCB, thereby extending the heat sinking.

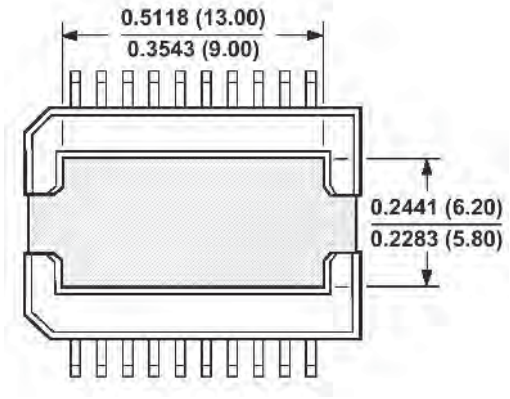


Figure 7-94: Bottom view of AD8016 20-lead PSOP3 package showing copper slug for aid in heat transfer (central gray area)

Both of AD8016 package options are characterized for both still and moving air, but the thermal information given above applies *without* the use of directed airflow. Therefore, adding additional airflow lowers thermal resistance further (see Reference 2).

For reliable, low thermal resistance designs with op amps, several design *Do's and Don'ts* are listed below. Consider all of these points, as may be practical.

1) *Do use as large an area of copper as possible for a PCB heat sink, up to the point of diminishing returns.*
2) *In conjunction with 1), do use multiple (outside) PCB layers, connected together with multiple vias.*
3) *Do use as heavy copper as is practical (2 oz. or more preferred).*
4) *Do provide sufficient natural ventilation inlets and outlets within the system, to allow heat to freely move away from hot PCB surfaces.*
5) *Do orient power-dissipating PCB planes vertically, for convection-aided airflow across heat sink areas.*
6) *Do consider the use of external* power buffer *stages, for precision op amp applications.*
7) *Do consider the use of* forced air, *for situations where several watts must be dissipated in a confined space.*
8) *Don't use solder mask planes over heat dissipating traces.*
9) *Don't use excessive supply voltages on ICs delivering power.*

For the most part, these points are obvious. However, one that could use some elaboration is number 9. Whenever an application requires only modest *voltage* swings (such as for example standard video, 2 V p-p) a wide supply voltage range can often be used. But, as the data of Figure 7-95 indicates, operation of an op amp driver on higher supply voltages produces a large IC dissipation, even though the load power is constant.

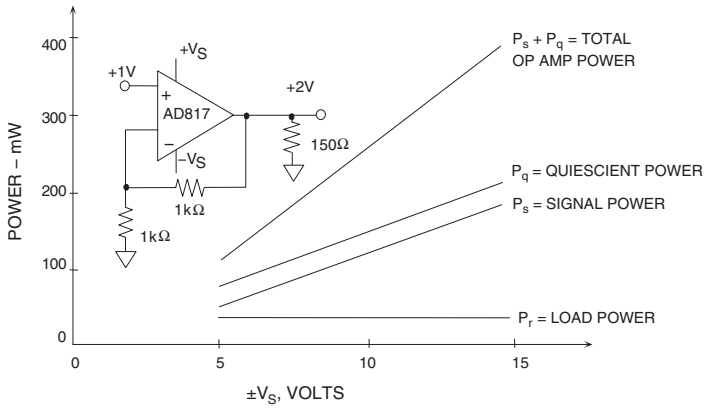


Figure 7-95: Power dissipated in video op amp driver for various supply voltages with low voltage output swing

In such cases, as long as the distortion performance of the application doesn't suffer, it can be advantageous to operate the IC on lower supplies, say ±5 V, as opposed to ±15 V. The above example data was calculated on a dc basis, which will generally tax the driver more in terms of power than a sine wave or a noise-like waveform, such as a DMT signal (see Reference 2). The general principles still hold for these ac waveforms, i.e., the op amp power dissipation is high when load current is high and the voltage low.

While there is ample opportunity for high power handling with the thermally enhanced packages described above for the AD8016 and AD8107, the increasingly popular smaller IC packages actually move in an opposite direction. Without question, it is true that today's smaller packages do noticeably sacrifice thermal performance. But, it must be understood that this is done in the interest of realizing a smaller size for the packaged op amp, and, ultimately, a much greater final PCB density for the overall system.

These points are illustrated by the thermal ratings for the AD8057 and AD8058 family of single and dual op amp devices, as is shown in Figure 7-96. The AD8057 and AD8058 op amps are available in three different packages. These are the SOT-23-5, and the 8-pin µSOIC, along with standard SOIC.

As the data shows, as the package size becomes smaller and smaller, much less power is capable of being removed. Since the lead frame is the only heatsinking possible with such tiny packages, their thermal performance is thus reduced. The θ_{JA} for the packages mentioned is 240°C/W, 200°C/W, and 160°C/W, respectively. Note this is more of a *package* than *device* limitation. Other ICs with the same packages have similar characteristics.

These discussions on the thermal application issues of op amps haven't dealt with the classic techniques of using clip-on (or bolt-on) type heat sinks. They also have not addressed the use of forced air cooling, generally considered only when tens of watts must be handled. These omissions are mainly because these approaches are seldom possible or practical with today's op amp packages.

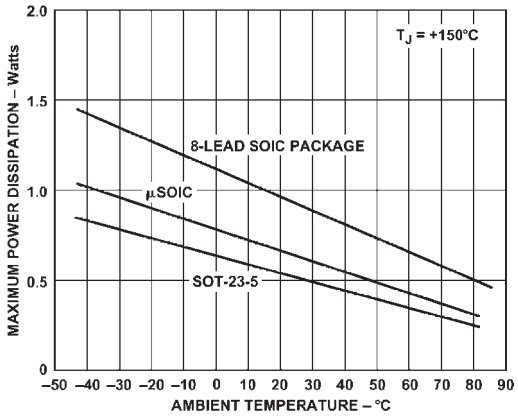


Figure 7-96: Comparative thermal performance for several AD8057/58 op amp package options

The more general discussions within References 4-7 can be consulted for this and other supplementary information.

References: Thermal Considerations

1. Data sheet for **AD8017 Dual High Output Current, High Speed Amplifier**, Analog Devices, Inc., www.analog.com.
2. Data sheet for **AD8016 Low Power, High Output Current, xDSL Line Driver**, Analog Devices, Inc., www.analog.com.
3. "Power Consideration Discussions," data sheet for **AD815 High Output Current Differential Driver**, Analog Devices, Inc., www.analog.com.
4. Walt Jung, Walt Kester, "Thermal Management," portion of Section 8 within Walt Kester, Editor, **Practical Design Techniques for Power and Thermal Management**, Analog Devices, Inc., 1998, ISBN 0-916550-19-2.
5. General Catalog, **AAVID Thermal Technologies, Inc.**, One Kool Path, Laconia, NH, 03246, 603-528-3400.
6. Seri Lee, "How to Select a Heat Sink," **Aavid Thermal Technologies**, www.aavid.com.
7. Seri Lee, "Optimum Design and Selection of Heat Sinks," **11th IEEE SEMI-THERM™ Symposium**, 1995, www.aavid.com.

SECTION 7-6

EMI/RFI Considerations

James Bryant, Walt Jung, Walt Kester

Analog circuit performance is often adversely affected by high frequency signals from nearby electrical activity. And, equipment containing analog circuitry may also adversely affect systems external to it. Reference 1 (page 4) describes this complementary transmission of undesirable high frequency signals from or into local equipment as per an IEC50 definition. These corresponding aspects of broad arena of *electromagnetic compatibility*, better known as EMC, are:

- *It describes the ability of electrical and electronic systems to operate without interfering with other systems . . .*
- *It also describes the ability of such systems to operate as intended within a specified electromagnetic environment.*

Complete EMC assurance would indicate that the equipment under design should neither produce spurious signals, nor be vulnerable to out-of-band external signals (i.e., those outside its intended frequency range). It is the latter class of EMC problem to which analog equipment most often falls prey. It is the graceful handling of these spurious signals that are emphasized within this section.

The externally produced electrical activity may generate noise, and is referred to either as electromagnetic interference (EMI), or radio frequency interference (RFI). In this section, we will refer to EMI in terms of both electromagnetic and radio frequency interference. One of the more challenging tasks of the analog designer is the control of equipment against undesired operation due to EMI. It is important to note that in this context, *EMI and or RFI is almost always detrimental*. Once given entrance into the equipment, it can and will degrade its operation, quite often considerably.

This section is heavily oriented towards minimizing undesirable analog circuit operation due to the *receipt* of EMI/RFI. Misbehavior of this sort is also known as EMI or RFI *susceptibility*, indicating a tendency towards anomalous equipment behavior when exposed to EMI/RFI. There is, of course, a complementary EMC issue, namely with regard to spurious *emissions.* However, since analog circuits typically involve fewer of pulsed, high speed, high current signal edges that give rise to such spurious signals (compared to high speed logic, for example), this aspect of EMC isn't as heavily treated here. Nevertheless, the reader should bear in mind that it can be important, particularly if the analog circuitry is part of a mixed-signal environment along with high speed logic.

Since all of these various EMC design points can be critical, *the end-of-chapter references are strongly recommended for supplementary study*. Indeed, for a thorough, fully competent design with respect to EMI, RFI, and EMC, the designer will need to become intimately acquainted with one or more of these references (see References 1–6). As for the material following, it is best viewed as an introduction to this extremely broad but increasingly important topic.

EMI/RFI Mechanisms

To understand and properly control EMI and RFI, it is helpful to first segregate it into manageable portions. Thus it is useful to remember that when EMI/RFI problems do occur, they can be fundamentally broken down into a *Source*, a *Path*, and a *Receiver*. As a systems designer, you have under your direct control the receiver part of this landscape, and perhaps some portion of the path. But seldom will the designer have control over the actual source.

EMI Noise Sources

There are countless ways in which undesired noise can couple into an analog circuit to ruin its accuracy. Some of the many examples of these noise sources are listed in Figure 7-97.

- EMI/RFI noise sources can couple from anywhere
- Some common sources of externally generated noise:
  - Radio and TV Broadcasts
  - Mobile Radio Communications
  - Cellular Telephones
  - Vehicular Ignition
  - Lightning
  - Utility Power Lines
  - Electric Motors
  - Computers
  - Garage Door Openers
  - Telemetry Equipment

Figure 7-97: Some common EMI noise sources

Since little control is possible over these sources of EMI, the next best management tool to exercise over them is to recognize and understand the possible paths by which they couple into the equipment under design.

EMI Coupling Paths

The EMI coupling paths are actually very few in terms of basic number. Three very general paths are by:

1. *Interference due to conduction (common-impedance)*
2. *Interference due to capacitive or inductive coupling (near-field interference)*
3. *Electromagnetic radiation (far-field interference)*

Noise Coupling Mechanisms

EMI energy may enter wherever there is an impedance mismatch or discontinuity in a system. In general this occurs at the interface where cables carrying sensitive analog signals are connected to PC boards, and through power supply leads. Improperly connected cables or poor supply filtering schemes are often perfect conduits for interference.

Conducted noise may also be encountered when two or more currents share a common path (impedance). This common path is often a high impedance “ground” connection. If two circuits share this path, noise currents from one will produce noise voltages in the other. Steps may be taken to identify potential sources of this interference (see References 1 and 2, plus Section 2 of this chapter).

Figure 7-98 shows some of the general ways noise can enter a circuit from external sources.

- Impedance mismatches and discontinuities
- Common-mode impedance mismatches → Differential Signals
- Capacitively Coupled (Electric Field Interference)
  - dV/dt → Mutual Capacitance → Noise Current
    (Example: 1V/ns produces 1mA/pF)
- Inductively Coupled (Magnetic Field)
  - di/dt → Mutual Inductance → Noise Voltage
    (Example: 1mA/ns produces 1mV/nH)

Figure 7-98: How EMI finds paths into equipment

There is a capacitance between any two conductors separated by a dielectric (air and vacuum are dielectrics, as well as all solid or liquid insulators). If there is a change of voltage on one conductor there will be change of charge on the other, and a *displacement current* will flow in the dielectric. Where either the capacitance or the dV/dT is high, noise is easily coupled. For example, a 1 V/ns rate-of-change gives rise to displacement currents of 1 mA/pF.

If changing magnetic flux from current flowing in one circuit threads another circuit, it will induce an emf in the second circuit. Such *mutual inductance* can be a troublesome source of noise coupling from circuits with high values of dI/dT. As an example, a mutual inductance of 1 nH and a changing current of 1 A/ns will induce an emf of 1 V.

Reducing Common-Impedance Noise

Steps to be taken to eliminate or reduce noise due to the conduction path sharing of impedances, or *common-impedance noise* are outlined in Figure 7-99.

- Common-impedance noise
  - Decouple op amp power leads at LF and HF
  - Reduce common-impedance
  - Eliminate shared paths
- Techniques
  - Low impedance electrolytic (LF) and local low inductance (HF) bypasses
  - Use ground and power planes
  - Optimize system design

Figure 7-99: Some solutions to common-impedance noise

These methods should be applied in conjunction with all of the related techniques discussed earlier within Section 2 of this chapter.

Power supply rails feeding several circuits are good common-impedance examples. Real-world power sources may exhibit low output impedance, or may they not—especially over frequency. Furthermore, PCB traces used to distribute power are both inductive and resistive, and may also form a ground loop. The use of power and ground planes also reduces the power distribution impedance. These dedicated conductor layers in a PCB are continuous (ideally, that is) and, as such, offer the lowest practical resistance and inductance.

In some applications where low level signals encounter high levels of common-impedance noise it will not be possible to prevent interference and the system architecture may need to be changed. Possible changes include:

1. *Transmitting signals in differential form*
2. *Amplifying signals to higher levels for improved S/N*
3. *Converting signals into currents for transmission*
4. *Converting signals directly into digital form*

Noise Induced by Near-Field Interference

Crosstalk is the second most common form of interference. In the vicinity of the noise source, i.e., near-field, interference is not transmitted as an electromagnetic wave, and the term crosstalk may apply to either inductively or capacitively coupled signals.

Reducing Capacitance-Coupled Noise

Capacitively-coupled noise may be reduced by reducing the coupling capacity (by increasing conductor separation), but is most easily cured by shielding. A conductive and grounded shield (known as a *Faraday shield*) between the signal source and the affected node will eliminate this noise, by routing the displacement current directly to ground.

With the use of such shields, it is important to note that it is always *essential* that a Faraday shield be grounded. A floating or open-circuit shield almost invariably increases capacitively-coupled noise. For a brief review of this shielding, consult Section 2 of this chapter, and see References 2 and 3 at the end of this section.

Methods to eliminate capacitance-coupled interference are summarized in Figure 7-100.

- Reduce Level of High dV/dt Noise Sources
- Use Proper Grounding Schemes for Cable Shields
- Reduce Stray Capacitance
  - Equalize Input Lead Lengths
  - Keep Traces Short
  - Use Signal-Ground Signal-Routing Schemes
- Use Grounded Conductive Faraday Shields to Protect
- Against Electric Fields

Figure 7-100: Methods to reduce capacitance-coupled noise

Reducing Magnetically-Coupled Noise

Methods to eliminate interference caused by magnetic fields are summarized in Figure 7-101.

To illustrate the effect of magnetically-coupled noise, consider a circuit with a closed-loop area of A cm^2 operating in a magnetic field with an rms flux density value of B gauss. The noise voltage V_n induced in this circuit can be expressed by the following equation:

$$V_n = 2\pi f B A \cos\theta \times 10^{-8} V \qquad \text{Eq. 7-8}$$

In this equation, *f* represents the frequency of the magnetic field, and θ represents the angle of the magnetic field B to the circuit with loop area A. Magnetic field coupling can be reduced by reducing the circuit loop

- Careful Routing of Wiring
- Use Conductive Screens for HF Magnetic Shields
- Use High Permeability Shields for LF Magnetic Fields (Mu-Metal)
- Reduce Loop Area of Receiver
  - Twisted Pair Wiring
  - Physical Wire Placement
  - Orientation of Circuit to Interference
- Reduce Noise Sources
  - Twisted Pair Wiring
  - Driven Shields

Figure 7-101: Methods to reduce magnetically-coupled noise

area, the magnetic field intensity, or the angle of incidence. Reducing circuit loop area requires arranging the circuit conductors closer together. Twisting the conductors together reduces the loop net area. This has the effect of canceling magnetic field pickup, because the sum of positive and negative incremental loop areas is ideally equal to zero. Reducing the magnetic field directly may be difficult. However, since magnetic field intensity is inversely proportional to the cube of the distance from the source, physically moving the affected circuit away from the magnetic field has a very great effect in reducing the induced noise voltage. Finally, if the circuit is placed perpendicular to the magnetic field, pickup is minimized. If the circuit's conductors are in parallel to the magnetic field the induced noise is maximized because the angle of incidence is zero.

There are also techniques that can be used to reduce the amount of magnetic-field interference, *at its source*. In the previous paragraph, the conductors of the receiver circuit were twisted together, to cancel the induced magnetic field along the wires. The same principle can be used on the source wiring. If the source of the magnetic field is large currents flowing through nearby conductors, these wires can be twisted together to reduce the net magnetic field.

Shields and cans are not nearly as effective against magnetic fields as against electric fields, but can be useful on occasion. At low frequencies magnetic shields using high permeability material such a Mu-metal can provide modest attenuation of magnetic fields. At high frequencies simple conductive shields are quite effective provided that the thickness of the shield is greater than the skin depth of the conductor used (at the frequency involved). Note—copper skin depth is $6.6/\sqrt{f}$ cm, with f in Hz.

Passive Components: Arsenal Against EMI

Passive components, such as resistors, capacitors, and inductors, are powerful tools for reducing externally induced interference when used properly.

Simple RC networks make efficient and inexpensive one-pole, low-pass filters. Incoming noise is converted to heat and dissipated in the resistor. But note that a fixed resistor does produce thermal noise of its own. Also, when used in the input circuit of an op amp or in amp, such resistor(s) can generate input-bias-current induced offset voltage. While matching the two resistors will minimize the dc offset, the noise will remain. Figure 7-102 summarizes some popular low-pass filters for minimizing EMI.

LP Filter Type	ADVANTAGE	DISADVANTAGE
RC Section	Simple Inexpensive	Resistor Thermal Noise $I_B \times R$ Drop $\rightarrow$ Offset Single-Pole Cutoff
LC Section (Bifilar)	Very Low Noise at LF Very Low IR Drop Inexpensive Two-Pole Cutoff	Medium Complexity Nonlinear Core Effects Possible
π Section (C-L-C)	Very Low Noise at LF Very Low IR Drop Pre-packaged Filters Multiple-Pole Cutoff	Most Complex Nonlinear Core Effects Possible Expensive

Figure 7-102: Using passive components within filters to combat EMI

In applications where signal and return conductors aren't well coupled magnetically, a common-mode (CM) choke can be used to increase their mutual inductance. Note that these comments apply mostly to in amps, which naturally receive a balanced input signal (whereas op amps are inherently unbalanced inputs—unless one constructs an in amp with them). A CM choke can be simply constructed by winding several turns of the differential signal conductors together through a high permeability (> 2000) ferrite bead. The magnetic properties of the ferrite allow differential-mode currents to pass unimpeded while suppressing CM currents.

Capacitors can also be used before and after the choke, to provide additional CM and differential-mode filtering, respectively. Such a CM choke is cheap and produces very low thermal noise and bias current-induced offsets, due to the wire's low DCR. However, there is a field around the core. A metallic shield surrounding the core may be necessary to prevent coupling with other circuits. Also, note that high current levels should be avoided in the core as they may saturate the ferrite.

The third method for passive filtering takes the form of packaged π-networks (C-L-C). These packaged filters are completely self-contained and include feedthrough capacitors at the input and the output as well as a shield to prevent the inductor's magnetic field from radiating noise. These more expensive networks offer high levels of attenuation and wide operating frequency ranges, but the filters must be selected so that for the operating current levels involved the ferrite doesn't saturate.

Reducing System Susceptibility to EMI

The general examples discussed above and the techniques illustrated earlier in this section outline the procedures that can be used to reduce or eliminate EMI/RFI. Considered on a *system* basis, a summary of possible measures is given in Figure 7-103.

- Always Assume that Interference Exists
- Use Conducting Enclosures Against Electric and HF
- Magnetic Fields
- Use Mu-Metal Enclosures against LF Magnetic Fields
- Implement Cable Shields Effectively
- Use Feedthrough Capacitors and Packaged PI Filters

Figure 7-103: Reducing system EMI/RFI susceptibility

Other examples of filtering techniques useful against EMI are illustrated later in this section, under "Reducing RFI rectification within op amp and in amp circuits."

The section immediately below further details shielding principles.

A Review of Shielding Concepts

The concepts of shielding effectiveness presented next are background material. Interested readers should consult References 4–9 cited at the end of the section for more detailed information.

Applying the concepts of shielding effectively requires an understanding of the source of the interference, the environment surrounding the source, and the distance between the source and point of observation (the receiver). If the circuit is operating close to the source (in the *near*, or induction-field), the field characteristics are determined by the source. If the circuit is remotely located (in the *far*, or radiation-field), the field characteristics are determined by the transmission medium.

A circuit operates in a near-field if its distance from the source of the interference is less than the wavelength (λ) of the interference divided by 2π, or $\lambda/2\pi$. If the distance between the circuit and the source of the interference is larger than this quantity, then the circuit operates in the far field. For instance, the interference caused by a 1 ns pulse edge has an upper bandwidth of approximately 350 MHz. The wavelength of a 350 MHz signal is approximately 32 inches (the speed of light is approximately 12"/ns). Dividing the wavelength by 2π yields a distance of approximately 5 inches, the boundary between near- and far-field. If a circuit is within 5 inches of a 350 MHz interference source, then the circuit operates in the near-field of the interference. If the distance is greater than 5 inches, the circuit operates in the far-field of the interference.

Regardless of the type of interference, there is a characteristic impedance associated with it. The characteristic, or wave impedance of a field is determined by the ratio of its electric (or E-) field to its magnetic (or H-) field. In the far field, the ratio of the electric field to the magnetic field is the characteristic (wave impedance) of free space, given by $Z_o = 377\ \Omega$. In the near field, the wave-impedance is determined by the nature of the interference and its distance from the source. If the interference source is high current and low voltage (for example, a loop antenna or a power line transformer), the field is predominately magnetic and exhibits a wave impedance less than 377 Ω. If the source is low current and high voltage (for example, a rod antenna or a high speed digital switching circuit), the field is predominately electric and exhibits a wave impedance greater than 377 Ω.

Conductive enclosures can be used to shield sensitive circuits from the effects of these external fields. These materials present an *impedance mismatch* to the incident interference, because the impedance of the shield

is lower than the wave impedance of the incident field. The effectiveness of the conductive shield depends on two things: First is the loss due to the *reflection* of the incident wave off the shielding material. Second is the loss due to the *absorption* of the transmitted wave *within* the shielding material. The amount of reflection loss depends upon the type of interference and its wave impedance. The amount of absorption loss, however, is independent of the type of interference. It is the same for near- and far-field radiation, as well as for electric or magnetic fields.

Reflection loss at the interface between two media depends on the difference in the characteristic impedances of the two media. For electric fields, reflection loss depends on the frequency of the interference and the shielding material. This loss can be expressed in dB, and is given by:

$$R_e\,(\mathrm{dB}) = 322 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f^3 r^2}\right] \qquad \text{Eq. 7-9}$$

where σ_r = relative conductivity of the shielding material, in Siemens per meter;

μ_r = relative permeability of the shielding material, in Henries per meter;

f = frequency of the interference, and

r = distance from source of the interference, in meters

For magnetic fields, the loss depends also on the shielding material and the frequency of the interference. Reflection loss for magnetic fields is given by:

$$R_m\,(\mathrm{dB}) = 14.6 + 10\log_{10}\left[\frac{fr^2\sigma_r}{\mu_r}\right] \qquad \text{Eq. 7-10}$$

and, for plane waves ($r > \lambda/2\pi$), the reflection loss is given by:

$$R_{pw}\,(\mathrm{dB}) = 168 + 10\log_{10}\left[\frac{\sigma_r}{\mu_r f}\right] \qquad \text{Eq. 7-11}$$

Absorption is the second loss mechanism in shielding materials. Wave attenuation due to absorption is given by:

$$A\,(\mathrm{dB}) = 3.34\ t\sqrt{\sigma_r \mu_r f} \qquad \text{Eq. 7-12}$$

where t = thickness of the shield material, in inches. This expression is valid for plane waves, electric and magnetic fields. Since the intensity of a transmitted field decreases exponentially relative to the thickness of the shielding material, the absorption loss in a shield one skin-depth (δ) thick is 9 dB. Since absorption loss is proportional to thickness and inversely proportional to skin depth, increasing the thickness of the shielding material improves shielding effectiveness at high frequencies.

Reflection loss for plane waves in the far field decreases with increasing frequency because the shield impedance, Z_s, increases with frequency. Absorption loss, on the other hand, increases with frequency because skin depth decreases. For electric fields and plane waves, the primary shielding mechanism is reflection loss, and at high frequencies, the mechanism is absorption loss.

Thus for high frequency interference signals, lightweight, easily worked high conductivity materials such as copper or aluminum can provide adequate shielding. At low frequencies however, both reflection and absorption loss to magnetic fields is low. It is thus very difficult to shield circuits from low frequency magnetic fields. In these applications, high permeability materials that exhibit low reluctance provide the

best protection. These low reluctance materials provide a magnetic shunt path that diverts the magnetic field away from the protected circuit.

To summarize the characteristics of metallic materials commonly used for shielded purposes: Use high conductivity metals for HF interference, and high permeability metals for LF interference.

A properly shielded enclosure is very effective at preventing external interference from disrupting its contents as well as confining any internally-generated interference. However, in the real world, openings in the shield are often required to accommodate adjustment knobs, switches, connectors, or to provide ventilation. Unfortunately, these openings may compromise shielding effectiveness by providing paths for high-frequency interference to enter the instrument.

The longest dimension (not the total area) of an opening is used to evaluate the ability of external fields to enter the enclosure, because the openings behave as slot antennas. Eq. 7-13 can be used to calculate the shielding effectiveness, or the susceptibility to EMI leakage or penetration, of an opening in an enclosure:

$$\text{Shielding Effectiveness}\ (\text{dB}) = 20\log_{10}\left(\frac{\lambda}{2\cdot L}\right) \qquad \text{Eq. 7-13}$$

where λ = wavelength of the interference and

L = maximum dimension of the opening

Maximum radiation of EMI through an opening occurs when the longest dimension of the opening is equal to one half-wavelength of the interference frequency (0 dB shielding effectiveness). A rule of thumb is to keep the longest dimension less than 1/20 wavelength of the interference signal, as this provides 20 dB shielding effectiveness.

Furthermore, a few small openings on each side of an enclosure is preferred over many openings on one side. This is because the openings on different sides radiate energy in different directions and, as a result, shielding effectiveness is not compromised. If openings and seams cannot be avoided, then conductive gaskets, screens, and paints alone or in combination should be used judiciously to limit the longest dimension of any opening to less than 1/20 wavelength. Any cables, wires, connectors, indicators, or control shafts penetrating the enclosure should have circumferential metallic shields physically bonded to the enclosure at the point of entry. In those applications where unshielded cables/wires are used, filters are recommended at the shield entry point.

General Points on Cables and Shields

Although covered in detail elsewhere, it is worth noting that the improper use of cables and their shields can be a significant contributor to both radiated and conducted interference. Rather than developing an entire treatise on these issues, the interested reader should consult References 2, 3, 5, and 6 for background.

As shown in Figure 7-104, proper cable/enclosure shielding confines sensitive circuitry and signals *entirely within the shield*, with no compromise to shielding effectiveness.

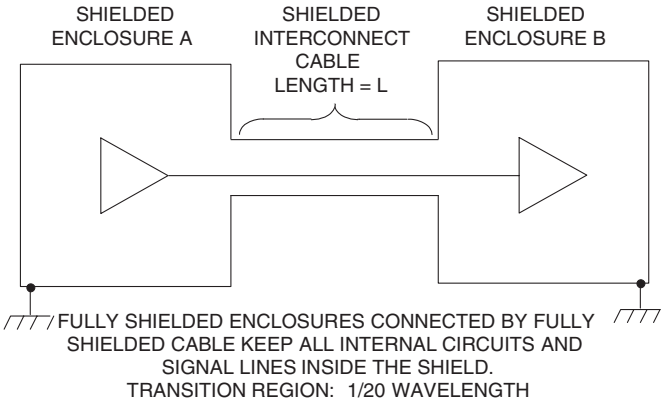


Figure 7-104: Shielded interconnect cables are either electrically long or short, depending upon the operating frequency

As can be noted by this diagram, the enclosures and the shield must be properly grounded, otherwise they can act as an antenna, thereby making the radiated and conducted interference problem worse (rather than better).

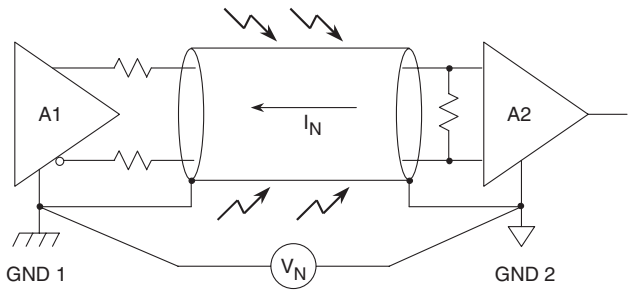
Depending on the type of interference (pickup/radiated, low/high frequency), proper cable shielding is implemented differently and is very dependent on the length of the cable. The first step is to determine whether the length of the cable is *electrically short* or *electrically long* at the frequency of concern. A cable is considered electrically short if the length of the cable is less than 1/20 wavelength of the highest frequency of the interference. Otherwise, it is considered to be electrically long.

For example, at 50 Hz/60 Hz, an electrically short cable is any cable length less than 150 miles, where the primary coupling mechanism for these low frequency electric fields is capacitive. As such, for any cable length less than 150 miles, the amplitude of the interference will be the same over the entire length of the cable.

In applications where the length of the cable is electrically long, or protection against high frequency interference is required, the preferred method is to connect the cable shield to low impedance points, *at both ends*. As will be seen shortly, this can be a direct connection at the driving end, and a capacitive connection at the receiver. If left ungrounded, unterminated transmission lines effects can cause reflections and standing waves along the cable. At frequencies of 10 MHz and above, circumferential (360°) shield bonds and metal connectors are required to main low impedance connections to ground.

In summary, for protection against low frequency (<1 MHz), electric-field interference, grounding the shield at one end is acceptable. For high frequency interference (>1 MHz), the preferred method is grounding the shield at both ends, using 360° circumferential bonds between the shield and the connector, and maintaining metal-to-metal continuity between the connectors and the enclosure.

In practice, however, there is a caveat involved with directly grounding the shield at both ends. When this is done, it creates a low frequency ground loop, shown in Figure 7-105.



- V_N Causes Current in Shield (Usually 50Hz/60Hz)
- Differential Error Voltage is Produced at Input of A2 unless:
  - A1 Output is Perfectly Balanced and
  - A2 Input is Perfectly Balanced and
  - Cable is Perfectly Balanced

Figure 7-105: Ground loops in shielded twisted pair cable can cause errors

Whenever two systems A1 and A2 are remote from each other, there is usually a difference in the ground potentials at each system, i.e., V_N. The frequency of this potential difference is generally the line frequency (50 Hz or 60 Hz) and multiples thereof. But, if the shield is directly grounded at both ends as shown, noise current I_N flows in the shield. In a perfectly balanced system, the common-mode rejection of the system is infinite, and this current flow produces no differential error at the receiver A2. However, perfect balance is never achieved in the driver, its impedance, the cable, or the receiver, so a certain portion of the shield current will appear as a differential noise signal, at the input of A2. The following illustrates correct shield grounding for various examples.

As noted above, cable shields are subject to both low and high frequency interference. Good design practice requires that the shield be grounded at both ends if the cable is electrically long to the interference frequency, as is usually the case with RF interference.

Figure 7-106 shows a remote passive RTD sensor connected to a bridge and conditioning circuit by a shielded cable. The proper grounding method is shown in the upper part of the figure, where the shield is grounded at the receiving end.

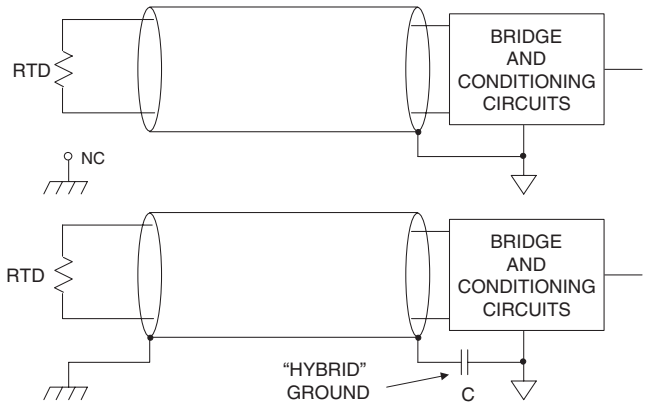


Figure 7-106: Hybrid grounding of shielded cable with passive sensor

Safety considerations may require that the remote end of the shield also be grounded. If this is the case, the receiving end can be grounded with a low inductance ceramic capacitor (0.01 μF to 0.1 μF), still providing high frequency grounding. The capacitor acts as a ground to RF signals on the shield but blocks low frequency line current to flow in the shield. This technique is often referred to as a *hybrid ground*.

A case of an active remote sensor and/or other electronics is shown Figure 7-107. In both situations, a hybrid ground is also appropriate, either for the balanced (upper) or the single-ended (lower) driver case. In both instances the capacitor "C" breaks the low frequency ground loop, providing effective RF grounding of the shielded cable at the A2 receiving end at the right side of the diagram.

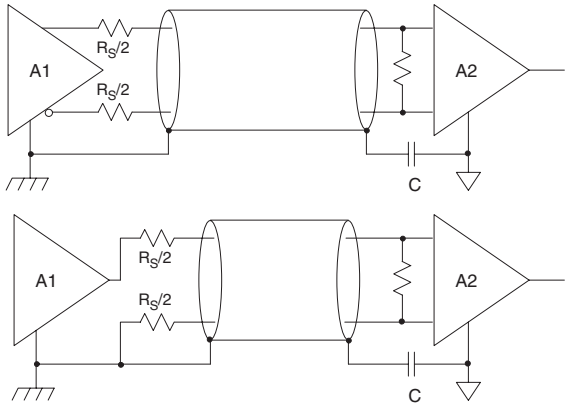


Figure 7-107: Impedance-balanced drive of balanced shielded cable aids noise-immunity with either balanced or single-ended source signals

There are also more subtle points that should be made with regard to the source termination resistances used, R_S. In both the balanced as well as the single-ended drive cases, the driving signal seen on the balanced line originates from a net impedance of R_S, which is split between the two twisted pair legs as twice $R_S/2$. In the upper case of a fully differential drive, this is straightforward, with an $R_S/2$ valued resistor connected in series with the complementary outputs from A1.

In the bottom case of the single-ended driver, note that there are still two $R_S/2$ resistors used, one in series with both legs. Here the grounded dummy return leg resistor provides an impedance-balanced ground connection drive to the differential line, aiding in overall system noise immunity. Note that this implementation is only useful for those applications with a balanced receiver at A2, as shown.

Coaxial cables are different from shielded twisted pair cables in that the signal return current path is through the shield. For this reason, the ideal situation is to ground the shield at the driving end and allow the shield to float at the differential receiver (A2) as shown in the upper portion of Figure 7-108. For this technique to work, however, the receiver must be a differential type with good high frequency CM rejection.

However, the receiver may be a single-ended type, such as typical of a standard single op amp type circuit. This is true for the bottom example of Figure 7-108, so there is no choice but to ground the coaxial cable shield at both ends for this case.

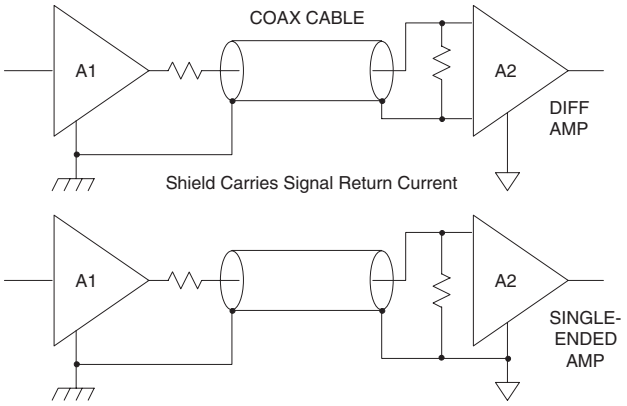


Figure 7-108: Coaxial cables can use either balanced or single-ended receivers

Input-Stage RFI Rectification Sensitivity

A well-known but poorly understood phenomenon in analog integrated circuits is *RFI rectification*, specifically as it occurs in op amps and in amps. While amplifying very small signals these devices can rectify large-amplitude, out-of-band HF signals, i.e., RFI. As a result, dc errors appear at the output in addition to the desired signal. The undesired HF signals can enter sensitive analog circuits by various means. Conductors leading into and out of the circuit provide a path for interference coupling into a circuit. These conductors pick up noise through capacitive, inductive, or radiation coupling, as discussed earlier. The spurious signals appear at the amplifier inputs, along with the desired signal. The spurious signals can be several tens of mV in amplitude, however, which causes problems. Simply stated, it cannot be assumed that a sensitive, low bandwidth dc amplifier will always reject out-of-band spurious signals. While this would

be the case for a simple linear low-pass filter, op amp and in amp devices actually rectify high level HF signals, leading to nonlinearities and anomalous offsets. Methods of analysis for, as well as the prevention of, RFI rectification are discussed in this section.

Background: Op amp and In Amp RFI Rectification Sensitivity Tests

Just about all in amp and op amp input stages use emitter-coupled BJT or source-coupled FET differential pairs of some type. Depending on the device operating current, the interfering frequency and its relative amplitude, these differential pairs can behave as high frequency detectors. As will be shown, the detection process produces spectral components at the harmonics of the interference, as well at dc. It is the detected dc component of the interference that shifts amplifier bias levels, leading to inaccuracies.

The effect of RFI rectification within op amps and in amps can be evaluated with relatively simple test circuits, as described for the *RFI Rectification Test Configuration* (see page 1-38 of Reference 10). In these tests, an op amp or in amp is configured for a gain of –100 (op amp), or 100 (in amp), with dc output measured after a 100 Hz low-pass filter, preventing interference from other signals. A 100 MHz, 20 mV p-p signal is the test stimulus, chosen to be well above test device frequency limits. In operation, the test evaluates dc output shift observed under stimulus presence. While an ideal dc shift for this measurement would be zero, the actual dc shift of a given part indicates the relative RFI rectification sensitivity. Devices using both BJT and FET technologies can be tested by this method, as can devices operating at either low or high supply current levels.

In the original op amp test device set of Reference 10, some FET-input devices (OP80, OP42, OP249 and AD845) exhibited no observable shift in their output voltages, while several others showed shifts of less than 10 μV referred to the input. Of the BJT-input op amps, the amount of shift decreased with increasing device supply current. Only two devices showed no observable output voltage shift (AD797 and AD827), while others showed shifts of less than 10 μV referred to the input (OP200 and OP297). For other op amps, it is to be expected that similar patterns would be shown under such testing.

From these tests, some generalizations on RFI rectification can be made. First, device susceptibility appears to be inversely proportional to supply current; that is, devices biased at low quiescent supply currents exhibit greatest output voltage shift. Second, Ics with FET-input stages appeared to be less susceptible to rectification than those with BJTs. Note that these points are independent of whether the device is an op amp or an in amp. In practice this means that the lower power op amps *or* in amps will tend to be more susceptible to RFI rectification effects. And, FET-input op amps (or in amps) will tend to be *less* susceptible to RFI, especially those operating at higher currents.

Based on these data and from the fundamental differences between BJTs and FETs, we can summarize what we know. Bipolar transistor action is controlled by a forward-biased p-n junction (the base-emitter junction) whose I-V characteristic is exponential and quite nonlinear. FET behavior, on the other hand, is controlled by voltages applied to a reverse-biased p-n junction diode (the gate-source junction). The I-V characteristic of FETs is a square-law, and thus it is inherently more linear than that of BJTs.

For the case of the lower supply current devices, transistors in the circuit are biased well below their peak f_T collector currents. Although the ICs may be constructed on processes whose device f_Ts can reach hundreds of MHz, charge transit times increase, when transistors are operated at low current levels. The impedance levels used also make RFI rectification in these devices worse. In low power op amps, impedances are on the order of hundreds to thousands of kΩs, whereas in moderate supply-current designs impedances might be no more than just a few kΩ. Combined, these factors tend to degrade a low-power device's RFI rectification sensitivity.

Figure 7-109 summarizes these general observations on RFI rectification sensitivity, and is applicable to both op amps and in-amps.

- BJT input devices *rectify* readily
  - Forward-biased B-E junction
  - Exponential I-V Transfer Characteristic
- FET input devices less sensitive to rectifying
  - Reversed-biased p-n junction
  - Square-law I-V Transfer Characteristic
- Low I_{supply} devices versus High I_{supply} devices
  - Low I_{supply} $\Rightarrow$ Higher rectification sensitivity
  - High I_{supply} $\Rightarrow$ Lower rectification sensitivity

Figure 7-109: Some general observations on op amp and in amp input stage RFI rectification sensitivity

An Analytical Approach: BJT RFI Rectification

While lab experiments can demonstrate that BJT-input devices exhibit greater RFI rectification sensitivity than comparable devices with FET inputs, a more analytical approach can also be taken to explain this phenomenon.

RF circuit designers have long known that p-n junction diodes are efficient rectifiers because of their nonlinear I-V characteristics. A spectral analysis of a BJT transistor current output for a HF sinewave input reveals that, as the device is biased closer to its "knee," nonlinearity increases. This, in turn, makes its use as a detector more efficient. This is especially true in low power op amps, where input transistors are biased at very low collector currents.

A rectification analysis for the collector current of a BJT has been presented in Reference 10, and will not be repeated here except for the important conclusions. These results reveal that the original quadratic second-order term can be simplified into a frequency-dependent term, $\Delta i_c(ac)$, at twice the input frequency and a dc term, $\Delta i_c(dc)$. The latter component can be expressed as noted in Eq. 7-14, the final form for the rectified dc term:

$$\Delta i_C(DC) = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} \qquad \text{Eq. 7-14}$$

This expression shows that the dc component of the second-order term is directly proportional to the *square* of the HF noise amplitude V_X, and, also, to I_C, the quiescent collector current of the transistor. To illustrate this point on rectification, note that the change in dc collector current of a bipolar transistor operating at an I_C of 1 mA with a spurious 10 mV_{peak} high frequency signal impinging upon it will be about 38 uA.

Reducing the amount of rectified collector current is a matter of reducing the quiescent current, or the magnitude of the interference. Since the op amp and in amp input stages seldom provide adjustable quiescent collector currents, reducing the level of interfering noise V_X is by far the best (and almost always the only) solution. For example, reducing the amplitude of the interference by a factor of 2, down to 5 mV_{peak} produces a net 4 to 1 reduction in the rectified collector current. Obviously, this illustrates the importance of keeping spurious HF signals away from RFI sensitive amplifier inputs.

An Analytical Approach: FET RFI Rectification

A rectification analysis for the drain current of a JFET has also been presented in Reference 10, and isn't repeated here. A similar approach was used for the rectification analysis of a FET's drain current as a function of a small voltage V_X, applied to its gate. The results of evaluating the second-order rectified term for the FET's drain current are summarized in Eq. 7-15. Like the BJT, an FET's second-order term has an ac and a dc component. The simplified expression for the dc term of the rectified drain current is given here, where the rectified dc drain current is directly proportional to the square of the amplitude of V_X, the spurious signal. However, Eq. 7-15 also reveals a very important difference between the *degree* of the rectification produced by FETs relative to BJTs.

$$\Delta i_D(DC) = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} \qquad \text{Eq. 7-15}$$

Whereas in a BJT the change in collector current has a direct relationship to its quiescent collector current level, the change in a JFET's drain current is proportional to its drain current at zero gate-source voltage, I_{DSS}, and inversely proportional to the square of its channel pinch-off voltage, V_P—parameters that are geometry and process dependent. Typically, JFETs used in the input stages of in amps and op amps are biased with their quiescent current of ~0.5 • I_{DSS}. Therefore, the change in a JFET's drain current is independent of its quiescent drain current; hence, independent of the operating point.

A quantitative comparison of second-order rectified dc terms between BJTs and FETs is illustrated in Figure 7-110. In this example, a bipolar transistor with a unit emitter area of 576 μm² is compared to a unit-area JFET designed for an I_{DSS} of 20 μA and a pinch-off voltage of 2 V. Each device is biased at 10 μA and operated at T_A = 25°C.

- BJT:
  Emitter area = 576 μm²
  I_C = 10μA
  V_T = 25.68mV @ 25°C

$$\Delta i_C = \left(\frac{V_X}{V_T}\right)^2 \bullet \frac{I_C}{4} = \frac{V_X^2}{264}$$

- JFET:
  I_{DSS} = 20μA (Z/L=1)
  V_P = 2V
  I_D = 10μA

$$\Delta i_D = \left(\frac{V_X}{V_P}\right)^2 \bullet \frac{I_{DSS}}{2} = \frac{V_X^2}{400x10^3}$$

- Conclusion: BJTs ~1500 more sensitive than JFETs

Figure 7-110: Relative sensitivity comparison – BJT versus JFET

The important result is that, under identical quiescent current levels, the change in collector current in bipolar transistors is about 1500 times greater than the change in a JFET's drain current. This explains why FET-input amplifiers behave with less sensitivity to large amplitude HF stimulus. As a result, they offer more RFI rectification immunity.

What all this boils down to is this: Since a user has virtually no access to the amplifier's internal circuitry, the prevention of IC circuit performance degradation due to RFI is left essentially to those means which are external to the ICs.

As the analysis above shows, regardless of the amplifier type, *RFI rectification is directly proportional to the square of the interfering signal's amplitude*. Therefore, to minimize RFI rectification in precision amplifiers, the level of interference must be reduced or eliminated, *prior to the stage*. The most direct way to reduce or eliminate the unwanted noise is by proper filtering.

This topic is covered in the section immediately following.

Reducing RFI Rectification within Op Amp and In Amp Circuits

EMI and RFI can seriously affect the dc performance of high accuracy analog circuits. Because of their relatively low bandwidth, precision op amps and in amps simply won't accurately amplify RF signals in the MHz range. However, if these out-of-band signals are allowed to couple into a precision amplifier through either its input, output, or power supply pins, they can be internally rectified by various amplifier junctions, ultimately causing an undesirable dc offset at the output. The previous theoretical discussion of this phenomenon has shown its basic mechanisms. The logical next step is to show how proper filtering can minimize or eliminate these errors.

Elsewhere in this chapter we have discussed how proper supply decoupling minimizes RFI on IC power pins. Further discussion is required with respect to the amplifier inputs and outputs, *at the device level*. It is assumed at this point that system level EMI/RFI approaches have already been implemented, such as an RFI-tight enclosure, properly grounded shields, power rail filtering, and so forth. The steps following can be considered as circuit-level EMI/RFI prevention.

Op Amp Inputs

The best way to prevent input stage rectification is to use a low-pass filter located close to the op amp input as shown in Figure 7-111. In the case of the inverting op amp at the left, filter capacitor C is placed between equal-value resistors R1-R2. This results in a simple corner frequency expression, as shown in the figure. At very low frequencies or dc, the closed loop gain of the circuit is –R3/(R1+R2). Note that C cannot be connected directly to the inverting input of the op amp, since that would cause instability. The filter bandwidth can be chosen at least 100 times the signal bandwidth to minimize signal loss.

For the noninverting case on the right, capacitor C can be connected directly to the op amp input as shown, and an input resistor with a value "R" yields the same corner frequency as the inverting case. In both cases low inductance chip-style capacitors should be used, such as NP0 ceramics. The capacitor should in any case be free of losses or voltage coefficient problems, which limits it to either the NP0 mentioned, or a film type.

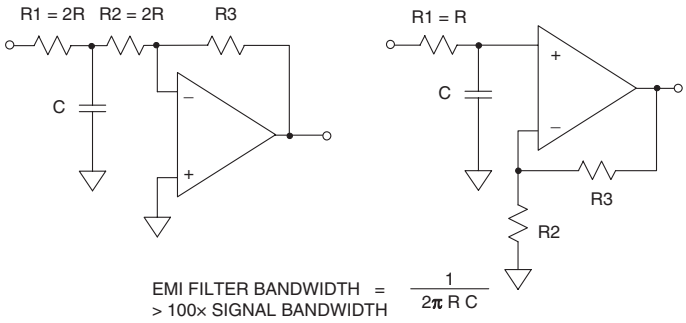


Figure 7-111: Simple EMI/RFI noise filters for op amp circuits

It should be noted that a ferrite bead can be used instead of R1, however ferrite bead impedance is not well controlled and is generally no greater than 100 Ω at 10 MHz to 100 MHz. This requires a large value capacitor to attenuate lower frequencies.

In Amp Inputs

Precision in amps are particularly sensitive to dc offset errors due to the presence of CM EMI/RFI. This is very much like the problem in op amps. And, as is true with op amps, the sensitivity to EMI/RFI is more acute with the lower power in amp devices.

A general-purpose approach to proper filtering for device level application of in amps is shown in Figure 7-112. In this circuit the in amp could, in practice, be any one of a number of devices. The relatively complex balanced RC filter preceding the in amp performs all of the high frequency filtering. The in amp would be programmed for the gain required in the application, via its gain-set resistance (not shown).

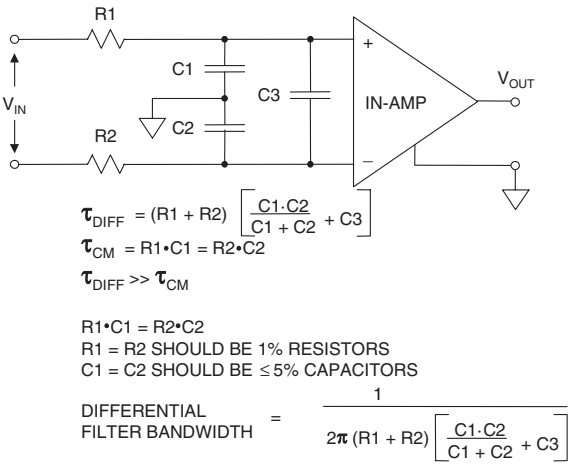
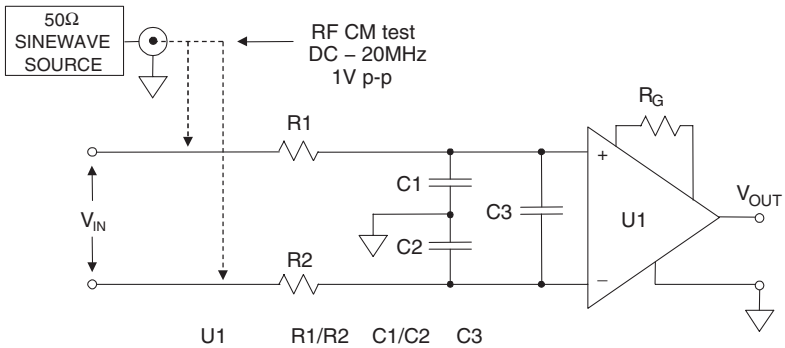


Figure 7-112: A general-purpose common-mode/ differential-mode RC EMI/RFI filter for in amps

Within the filter, note that fully balanced filtering is provided for both CM (R1-C1 and R2-C2) as well as differential mode (DM) signals (R1+R2, and C3 ‖ the series connection of C1-C2). If R1-R2 and C1-C2 aren't well matched, some of the input common-mode signal at V_{IN} will be converted to a differential mode signal at the in amp inputs. For this reason, C1 and C2 should be matched to within at least 5% of each other. Also, to aid this matching, R1 and R2 should be 1% metal film resistors. It is assumed that the source resistances seen at the V_{IN} terminals are low with respect to R1-R2, and matched. In this type of filter, C3 should be chosen much larger than C1 or C2 (C3 ≥ C1, C2), in order to suppress spurious differential signals due to CM⇒DM conversion resulting from mismatch of the R1-C1 and R2-C2 time constants.

The overall filter bandwidth should be at least 100 times the input signal bandwidth. Physically, the filter components should be symmetrically mounted on a PC board with a large area ground plane and placed close to the in amp inputs for optimum performance.

Figure 7-113 shows a family of these filters, as suited to a range of different in amps. The RC components should be tailored to the different in amp devices, as per the table. These filter components are selected for a reasonable balance of low EMI/RFI sensitivity and a low increase in noise (vis-à-vis that of the related in amp, without the filter).



U1	R1/R2 1%	C1/C2 ≤5%	C3 10%
AD620/621/622	4.02k	1nF	47nF
AD623	10k	1nF	22nF
AD627	20k	1nF	22nF

Figure 7-113: Flexible common-mode and differential-mode RC EMI/RFI filters are useful with the AD620 series, the AD623, AD627, and other in amps

To test the EMI/RFI sensitivity of the configuration, a 1 V p-p CM signal can be applied to the input resistors, as noted. With a typically used in amp such as the AD620 working at a gain of 1000, the maximum RTI input offset voltage shift observed was 1.5 µV over the 20 MHz range. In the AD620 filter example, the differential bandwidth is about 400 Hz.

Common-mode chokes offer a simple, one-component EMI/RFI protection alternative to the passive RC filters, as shown in Figure 7-114.

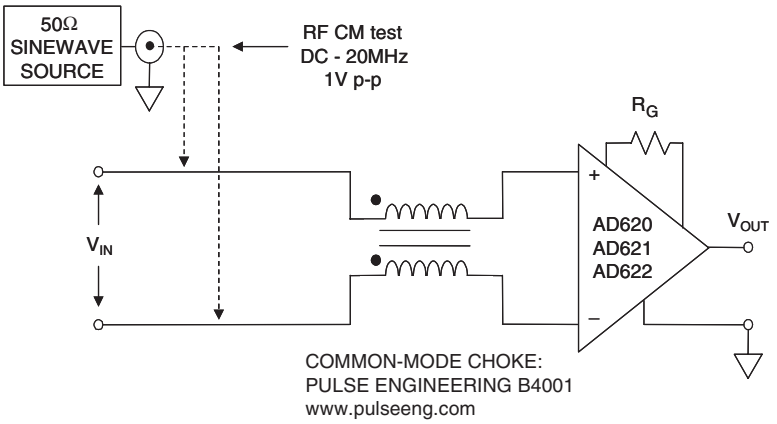


Figure 7-114: For simplicity as well as lowest noise EMI/RFI filter operation, a common-mode choke is useful with the AD620 series in amp devices

In addition to being a low component count approach, choke-based filters offer low noise, by dispensing with the resistances. Selecting the proper common-mode choke is critical, however. The choke used in the circuit of Figure 7-114 is a Pulse Engineering B4001. The maximum RTI offset shift measured from dc to 20 MHz at G = 1000 was 4.5 µV. Either an off-the-shelf choke such as the B4001 can be used for this filter, or, alternately one can be constructed. Since balance of the windings is important, bifilar wire is suggested. The core material must of course operate over the expected frequency band. Note that, unlike the Figure 7-113 family of RC filters, a choke-only filter offers no differential filtration. Differential mode filtering can be optionally added, with a second stage following the choke, by adding the R1-C3-R2 connections of Figure 7-112.

For further information on in amp EMI/RFI filtering, see References 10, and 12 – 15.

Amplifier Outputs and EMI/RFI

In addition to filtering the input and power pins, amplifier *outputs* also need to be protected from EMI/RFI, especially if they must drive long lengths of cable, which act as antennas. RF signals received on an output line can couple back into the amplifier input where it is rectified, and appears again on the output as an offset shift.

A resistor and/or ferrite bead, or both, in series with the output is the simplest and least expensive output filter, as shown in Figure 7-115 (upper circuit).

Adding a resistor-capacitor-resistor "T" circuit as shown in Figure 7-115 (lower circuit) improves this filter with just slightly more complexity. The output resistor and capacitor divert most of the high frequency energy away from the amplifier, making this configuration useful even with low power active devices. Of course, the time constant of the filter parts must be chosen carefully, to minimize any degradation of the desired output signal. In this case the RC components are chosen for an approximate 3 MHz signal bandwidth, suitable for instrumentation or other low bandwidth stages.

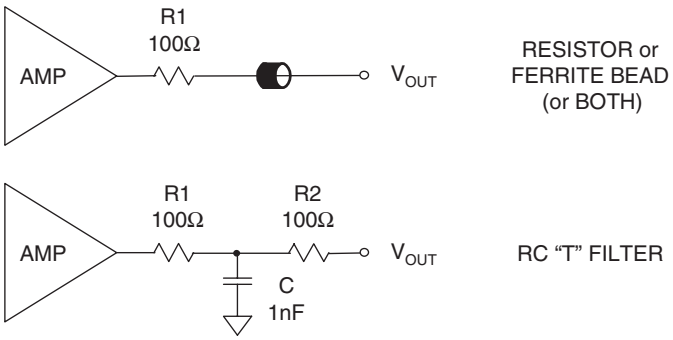


Figure 7-115: Op amp and in amp outputs should be protected against EMI/RFI, particularly if they drive long cables.

Printed Circuit Board Design for EMI/RFI Protection

This section summarizes general points on EMI/RFI with respect to the printed circuit board (PCB) layout. It complements earlier chapter discussions on general PCB design techniques. When a PCB design has not been optimized in terms of EMI/RFI, system performance can be compromised. This is true not only for signal-path performance, but also for the system's susceptibility to EMI, plus the degree of EMI radiated by the system. Failure to implement sound PCB layout techniques will very likely lead to system/instrument EMC failures.

To summarize earlier points of this section, a real-world PCB layout may allow multiple paths through which high-frequency noise can couple/radiate into and/or out of the circuit.

This is especially true for digital circuitry, operating at high *edge rates*. It is the rapid changes of logic state ($1 \Rightarrow 0$ or $0 \Rightarrow 1$), i.e., the edge rate that contains the HF energy which can easily radiate as EMI. While similar points are applicable to precision high-speed analog or mixed analog/digital circuits, logic devices are by far the worst potential EMI offenders. Identifying critical circuits and paths helps in designing the PCB for both low emissions and susceptibility to radiated and conducted external and internal noise sources.

Carefully Choose Logic Devices

Logic-family speaking, a key point in minimizing system noise problems is to *choose devices no faster than actually required by the application*. Many designers assume that faster is always better—fast logic is better than slow, high bandwidth amplifiers better than low bandwidth, and fast DACs and ADCs are better, even if the speed isn't required by the system. Unfortunately, faster is *not* better, and actually may be worse for EMI concerns.

Many fast DACs and ADCs have digital inputs and outputs with edge rates in the 1 ns/V region. Because of this wide bandwidth, the sampling clock and the digital inputs can respond to any form of high frequency noise, even glitches as narrow as 1 ns to 3 ns. These high speed data converters and amplifiers are thus easy prey for the high frequency noise of microprocessors, digital signal processors, motors, switching regulators, hand-held radios, electric jackhammers, and so forth. With some of these high speed devices, a small amount of input/output filtering may be required to desensitize the circuit from its EMI/RFI environment. A ferrite bead just before the local decoupling capacitor is very effective in filtering high frequency noise on supply lines. Of course, with circuits requiring bipolar supplies, this technique should be applied to both positive and negative supply lines.

To help reduce emissions generated by extremely fast moving digital signals at DAC inputs or ADC outputs, a small resistor or ferrite bead may be required at each digital input/output.

Design PCBs Thoughtfully

Once the system's critical paths and circuits have been identified, the next step in implementing sound PCB layout is to partition the printed circuit board according to circuit function. This involves the appropriate use of power, ground, and signal planes. Good PCB layouts also isolate critical analog paths from sources of high interference (I/O lines and connectors, for example). High frequency circuits (analog and digital) should be separated from low frequency ones. Furthermore, automatic signal routing CAD layout software should be used with extreme caution. Critical signal paths should be routed by hand, to avoid undesired coupling and/or emissions.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to RF fields, by a factor of 10 or more, compared to double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with

signal crossovers, and so forth. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes, nor analog and digital power planes.

Designing Controlled Impedances Traces on PCBs

A variety of trace geometries are possible with controlled impedance designs, and they may be either integral to or allied to the PCB pattern. In the discussions below, the basic patterns follow those of the IPC, as described in standard 2141 (see Reference 16).

Note that following figures use the term "ground plane." It should be understood that this plane is in fact a large area, low impedance *reference* plane. In practice it may actually be either a ground plane or a power plane, both of which are assumed to be at zero ac potential.

The first of these is the simple wire-over-a-plane form of transmission line, also called a *wire microstrip*. A cross-sectional view is shown in Figure 7-116. This type of transmission line might be a signal wire used within a breadboard, for example. It is composed simply of a discrete insulated wire spaced a fixed distance over a ground plane. The dielectric would be either the insulation wall of the wire, or a combination of this insulation and air.

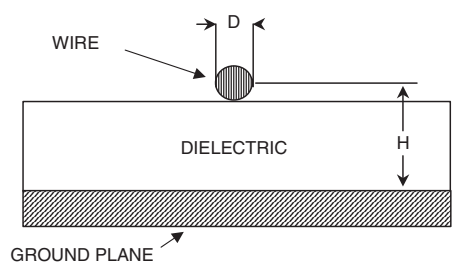


Figure 7-116: A wire microstrip transmission line with defined impedance is formed by an insulated wire spaced from a ground plane

The impedance of this line in ohms can be estimated with Eq. 7-16. Here D is the conductor diameter, H the wire spacing above the plane, and ε_r the dielectric constant.

$$Z_O(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{4H}{D}\right] \qquad \text{Eq. 7-16}$$

For patterns integral to the PCB, there are a variety of geometric models from which to choose, single-ended and differential. These are covered in some detail within IPC standard 2141 (see Reference 16), but information on two popular examples is shown here.

Before beginning any PCB-based transmission line design, it should be understood that there are abundant equations, all claiming to cover such designs. In this context, "Which of these is accurate?" is an extremely pertinent question. The unfortunate answer is, *none is perfectly so.* All of the existing equations are approximations, and thus accurate to varying degrees, depending upon specifics. The best known and most widely quoted equations are those of Reference 16, but even these come with application caveats.

Reference 17 has evaluated the Reference 16 equations for various geometric patterns against test PCB samples, finding that predicted accuracy varies according to target impedance. Reference 18 also evaluates the Reference 16 equations, offering an alternative and even more complex set (see Reference 19). The equations quoted below are from Reference 16, and offered here as a starting point for a design, subject to further analysis, testing, and design verification. The bottom line is, study carefully and take PCB trace impedance equations with a proper dose of salt.

Microstrip PCB transmission lines

For a simple two-sided PCB design where one side is a ground plane, a signal trace on the other side can be designed for controlled impedance. This geometry is known as a *surface microstrip,* or more simply, *microstrip*.

A cross-sectional view of a two-layer PCB illustrates this microstrip geometry as shown in Figure 7-117.

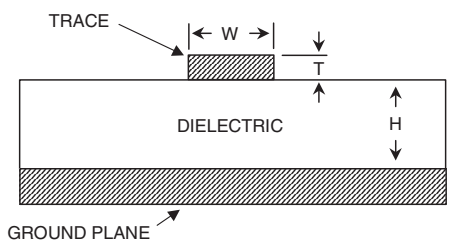


Figure 7-117: A microstrip transmission line with defined impedance is formed by a PCB trace of appropriate geometry, spaced from a ground plane

For a given PCB laminate and copper weight, note that all parameters will be predetermined except for W, the width of the signal trace. Eq. 7-17 can then be used to design a PCB trace to match the impedance required by the circuit. For the signal trace of width W and thickness T, separated by distance H from a ground (or power) plane by a PCB dielectric with dielectric constant ε_r, the characteristic impedance is:

$$Z_O(\Omega) = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left[\frac{5.98H}{(0.8W + T)}\right] \qquad \text{Eq. 7-17}$$

Note that in these expressions, measurements are in common dimensions (mils).

These transmission lines will have not only a characteristic impedance, but also capacitance. This can be calculated in terms of pF/in as shown in Eq. 7-18.

$$C_O(pF/in) = \frac{0.67(\varepsilon_r + 1.41)}{\ln\left[5.98H/(0.8W + T)\right]} \qquad \text{Eq. 7-18}$$

As an example including these calculations, a 2-layer board might use 20 mil wide (W), 1 ounce (T = 1.4) copper traces separated by 10 mil (H) FR-4 (ε_r = 4.0) dielectric material. The resulting impedance for this microstrip would be about 50 Ω. For other standard impedances, for example the 75 Ω video standard, adjust "W" to about 8.3 mils.

Some Microstrip Rules of Thumb

This example touches an interesting and quite handy point. Reference 17 discusses a useful rule of thumb pertaining to microstrip PCB impedance. For a case of dielectric constant of 4.0 (FR-4), it turns out that when W/H is 2/1, the resulting impedance will be close to 50 Ω (as in the first example, with W = 20 mils).

Careful readers will note that Eq. 7-17 predicts Z_o to be about 46 Ω, generally consistent with accuracy quoted in Reference 17 (>5%). The IPC microstrip equation is most accurate between 50 Ω and 100 Ω, but is substantially less so for lower (or higher) impedances. Reference 20 gives tabular results of various PCB industry impedance calculator tools.

The propagation delay of the microstrip line can also be calculated, as per Eq. 7-19. This is the one-way transit time for a microstrip signal trace. Interestingly, for a given geometry model, *the delay constant in ns/ft is a function only of the dielectric constant, and not the trace dimensions* (see Reference 21). Note that this is quite a convenient situation. It means that, with a given PCB laminate (and given ε_r), the propagation delay constant is fixed for various impedance lines.

$$t_{pd}\left(\text{ns/ft}\right) = 1.017\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 7-19}$$

This delay constant can also be expressed in terms of ps/in, a form which will be more practical for smaller PCBs. This is:

$$t_{pd}\left(\text{ps/in}\right) = 85\sqrt{0.475\varepsilon_r + 0.67} \qquad \text{Eq. 7-20}$$

Thus for an example PCB dielectric constant of 4.0, it can be noted that a microstrip's delay constant is about 1.63 ns/ft, or 136 ps/in. These two additional rules of thumb can be useful in designing the timing of signals across PCB trace runs.

Symmetric Stripline PCB Transmission Lines

A method of PCB design preferred from many viewpoints is a multilayer PCB. This arrangement *embeds* the signal trace between a power and a ground plane, as shown in the cross-sectional view of Figure 7-118. The low impedance ac ground planes and the embedded signal trace form a *symmetric stripline* transmission line.

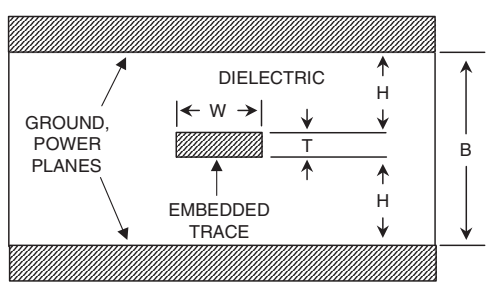


Figure 7-118: A symmetric stripline transmission line with defined impedance is formed by a PCB trace of appropriate geometry embedded between equally spaced ground and/or power planes

As can be noted from the figure, the return current path for a high frequency signal trace is located directly above and below the signal trace on the ground/power planes. The high frequency signal is thus contained entirely inside the PCB, minimizing emissions, and providing natural shielding against incoming spurious signals.

The characteristic impedance of this arrangement is again dependent upon geometry and the ε_r of the PCB dielectric. An expression for Z_O of the stripline transmission line is:

$$Z_O(\Omega) = \frac{60}{\sqrt{\varepsilon_r}} \ln\left[\frac{1.9(B)}{(0.8W + T)}\right] \qquad \text{Eq. 7-21}$$

Here, all dimensions are again in mils, and B is the spacing between the two planes. In this symmetric geometry, note that B is also equal to 2H + T. Reference 17 indicates that the accuracy of this Reference 16 equation is typically on the order of 6%.

Another handy rule of thumb for the symmetric stripline in an $\varepsilon_r = 4.0$ case is to make B a multiple of W, in the range of 2 to 2.2. This will result in an stripline impedance of about 50 Ω. Of course this rule is based on a further approximation, by neglecting T. Nevertheless, it is still useful for ballpark estimates.

The symmetric stripline also has a characteristic capacitance, which can be calculated in terms of pF/in as shown in Eq. 7-22.

$$C_O(pF/in) = \frac{1.41(\varepsilon_r)}{\ln\left[3.81H/(0.8W + T)\right]} \qquad \text{Eq. 7-22}$$

The propagation delay of the symmetric stripline is shown in eq. 7-23.

$$t_{pd}(ns/ft) = 1.017\sqrt{\varepsilon_r} \qquad \text{Eq. 7-23}$$

or, in terms of ps:

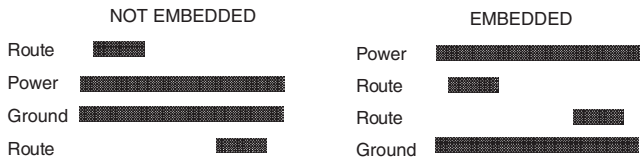
$$t_{pd}(ps/in) = 85\sqrt{\varepsilon_r} \qquad \text{Eq. 7-24}$$

For a PCB dielectric constant of 4.0, it can be noted that the symmetric stripline's delay constant is almost exactly 2 ns/ft, or 170 ps/in.

Some Pros and Cons of Embedding Traces

The above discussions allow the design of PCB traces of defined impedance, either on a surface layer or embedded between layers. There are, of course, many other considerations beyond these impedance issues.

Embedded signals do have one major and obvious disadvantage—the debugging of the hidden circuit traces is difficult to impossible. Some of the pros and cons of embedded signal traces are summarized in Figure 7-119.



- Advantages
  - Signal traces shielded and protected
  - Lower impedance, thus lower emissions and crosstalk
  - Significant improvement > 50MHz
- Disadvantages
  - Difficult prototyping and troubleshooting
  - Decoupling may be more difficult
  - Impedance may be too low for easy matching

Figure 7-119: The pros and cons of not embedding versus the embedding of signal traces in multilayer PCB designs

Multilayer PCBs can be designed *without* the use of embedded traces, as shown in the left cross-sectional example. This embedded case could be considered as a doubled two-layer PCB design (i.e., four copper layers overall). The routed traces at the top form a microstrip with the power plane, while the traces at the bottom form a microstrip with the ground plane. In this example, the signal traces of both outer layers are readily accessible for measurement and troubleshooting purposes. But, the arrangement does nothing to take advantage of the shielding properties of the planes.

This nonembedded arrangement will have greater emissions and susceptibility to external signals, vis-à-vis the embedded case at the right, which uses the embedding, and does take full advantage of the planes. As in many other engineering efforts, the decision of embedded versus not-embedded for the PCB design becomes a trade-off, in this case one of reduced emissions versus ease of testing.

Transmission Line Termination Rule of Thumb

Much has been written about terminating PCB traces in their characteristic impedance, to avoid signal reflections. A good rule of thumb to determine when this is necessary is as follows: *Terminate the transmission line in its characteristic impedance when the one-way propagation delay of the PCB track is equal to or greater than one-half the applied signal rise/fall time (whichever edge is faster*). For example, a 2-inch microstrip line over an $E_r = 4.0$ dielectric would have a delay of ~270 ps. Using the above rule strictly, termination would be appropriate whenever the signal rise time is < ~500 ps. A more conservative rule is to use a 2-inch (PCB track length)/nanosecond (rise/fall time) rule. If the signal trace exceeds this trace-length/speed criterion, termination should be used.

For example, PCB tracks for high-speed logic with rise/fall time of 5 ns should be terminated in their characteristic impedance if the track length is equal to or greater than 10 inches (where measured length *includes* meanders).

In the analog domain, it is important to note that this same 2-inch/nanosecond rule of thumb should also be used with op amps and other circuits, to determine the need for transmission line techniques. For instance, if an amplifier must output a maximum frequency of f_{max}, then the equivalent risetime t_r is related to this f_{max}. This limiting risetime, t_r, can be calculated as:

$$t_r = 0.35/f_{max} \qquad \text{Eq. 7-25}$$

The maximum PCB track length is then calculated by multiplying t_r by 2-inch/nanosecond. For example, a maximum frequency of 100 MHz corresponds to a risetime of 3.5 ns, so a 7-inch or more track carrying this signal should be treated as a transmission line.

The best ways to keep sensitive analog circuits from being affected by fast logic are to physically separate the two by the PCB layout, and to use no faster logic family than is dictated by system requirements. In some cases, this may require the use of several logic families in a system. An alternative is to use series resistance or ferrite beads to slow down the logic transitions where highest speed isn't required.

A general method of doing this is to use a series R at a logic driver output, and a shunt C at a CMOS gate input. The series resistance and the net input capacitance of the gate form a lowpass filter. Typical CMOS input capacitance is 10 pF. Locate the series resistor close to the driving gate, adding an additional small capacitance, as needed. The resistor minimizes transient switching currents, and may also eliminate the necessity for transmission line techniques. The value of the resistor should be chosen such that the rise and fall times at the receiving gate are fast enough to meet system requirement, but no faster. Also, make sure that the resistor is not so large that the logic levels at the receiver are out of specification because of the source and sink current which must flow through the resistor. Use of CMOS logic will simplify this, since the input currents are so low.

References: EMI/RFI Considerations

1. Tim Williams, **EMC for Product Designers, 2nd Ed.**, Newnes, Oxford, 1996, ISBN: 0-7506-2466-3.
2. Henry Ott, **Noise Reduction Techniques In Electronic Systems**, **2nd Ed.**, John Wiley & Sons, New York, 1988, ISBN 0-471-85068-3.
3. Mark Montrose, **EMC and the Printed Circuit Board**, IEEE Press, 1999, ISBN 0-7803-4703-X.
4. Ralph Morrison, **Grounding And Shielding Techniques in Instrumentation, 3rd Ed.**, John Wiley & Sons, New York, 1986, ISBN 0-471-83805-5.
5. Daryl Gerke and William Kimmel, "Designer's Guide to Electromagnetic Compatibility," **EDN**, January 20, 1994.
6. **Designing for EMC** (Workshop Notes), Kimmel Gerke Associates, Ltd., 1994.
7. Daryl Gerke and William Kimmel, "EMI and Circuit Components," **EDN**, September 1, 2000.
8. Alan Rich, "Understanding Interference-Type Noise," **Analog Dialogue**, Vol. 16, No. 3, 1982, pp. 16–19 (also available as application note AN346).
9. Alan Rich, "Shielding and Guarding," **Analog Dialogue**, Vol. 17, No. 1, 1983, pp. 8–13 (also available as application note AN347).
10. James Wong, Joe Buxton, Adolfo Garcia, James Bryant**,** "Filtering and Protection Against EMI/RFI" and "Input Stage RFI Rectification Sensitivity," Chapter 1, pp. 21–55 of **Systems Application Guide**, 1993, Analog Devices, Inc., Norwood, MA, ISBN 0-916550-13-3.
11. Adolfo Garcia**,** "EMI/RFI Considerations," Chapter 7, pp. 69–88 of **High Speed Design Techniques**, 1996, Analog Devices, Inc., Norwood, MA, 1993, ISBN 0-916550-17-6.
12. Walt Kester, Walt Jung, Chuck Kitchen, "Preventing RFI Rectification," Chapter 10, pp. 10.39–10.43 of **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, Inc., Norwood, MA, 1999, ISBN 0-916550-20-6.
13. Charles Kitchen, Lew Counts, **A Designer's Guide to Instrumentation Amplifiers**, Analog Devices, Inc., 2000.
14. **B4001 and B4003 Common-Mode Chokes**, Pulse Engineering, Inc., 12220 World Trade Drive, San Diego, CA, 92128, 619-674-8100, www.pulseeng.com.
15. **Understanding Common-Mode Noise**, Pulse Engineering, Inc., 12220 World Trade Drive, San Diego, CA, 92128, 619-674-8100, www.pulseeng.com.
16. Standard IPC-2141, "Controlled Impedance Circuit Boards and High Speed Logic Design," 1996, Institute for Interconnection and Packaging Electronic Circuits, 2215 Sanders Road, Northbrook, IL, 60062-6135, 847-509-9700, www.ipc.org.
17. Eric Bogatin, "Verifying the Accuracy of 2D Field Solvers for Characteristic Impedance Calculation," Ansoft Seminar, October 11, 2000, www.bogatinenterprises.com.
18. Andrew Burkhardt, Christopher Gregg, Alan Staniforth, "Calculation of PCB Track Impedance," Technical Paper S-19-5, presented at the IPC Printed Circuits Expo '99 Conference, March 14–18, 1999.
19. Brian C. Wadell, **Transmission Line Design Handbook,** Artech House, Norwood, MA, 1991, ISBN: 0-89006-436-9.
20. Eric Bogatin, "No Myths Allowed," "Impedance Calculations," "A Chip Center Column," November 1, 1999, www.chipcenter.com/signalintegrity.

21. William R. Blood, Jr., **MECL System Design Handbook** (HB205/D, Rev. 1A May 1988), ON Semiconductor, August, 2000.
22. Paul Brokaw, "An IC Amplifier User Guide To Decoupling, Grounding, And Making Things Go Right For A Change," **Analog Devices AN202**.

Some useful EMC and signal integrity related URLs:

Eric Bogatin website, www.bogatinenterprises.com

Chip Center's "Signal Integrity" page, www.chipcenter.com/signalintegrity

Kimmel Gerke Associates website, www.emiguru.com

Henry Ott website, www.hottconsultants.com

IEEE EMC website, www.ewh.ieee.org/soc/emcs

Mark Montrose website, www.montrosecompliance.com/index.html

Tim Williams website, www.elmac.co.uk

This page intentionally left blank

SECTION 7-7

Simulation, Breadboarding and Prototyping

Joe Buxton, Walt Kester, James Bryant, Walt Jung

In this final section of the chapter, the practical aspects of assembling hardware for op amp and other analog functions are brought to play. Various experimental techniques are useful towards verifying the integrity of a design. These include electronic *analog circuit simulation* programs, to be used with (but not to the exclusion of) the allied lab processes of *breadboarding* and *prototyping*.

Analog Circuit Simulation

In the past decade, circuit simulation has taken on an increasingly important role within analog circuit design. The most popular simulation tool for this is SPICE, which is available in multiple forms for various computer platforms (see References 1 and 2). However, to achieve meaningful simulation results, designers need accurate models of many system components. The most critical of these are realistic models for ICs, the active devices that drive modern designs. In the early 1990s, Analog Devices developed an advanced op amp SPICE model, which is, in fact, still in use today (see References 3 and 4). Within this innovative open amplifier architecture, gain and phase response can be fully modeled, enabling designers to accurately predict ac, dc, and transient performance behavior. This modeling methodology has also been extended to include other devices such as in amps, voltage references, and analog multipliers.

Figure 7-120 lists some major SPICE simulation objectives. The popularity of SPICE simulation has led to many op amp macromodel releases, which (ideally) software-mimic amplifier electrical performance. With numerous models available, several confusions are possible. There may be uncertainty as to what is/isn't modeled, plus a basic question of *model accuracy*. All of these points are important, in order to place confidence in simulation results. So, *verification* of a model is important, checking it by comparison to the actual device performance conditions, before trusting it for serious designs.

- Understand Realistic Simulation Goals
- Evaluate Available Models Accordingly
- Know the Capabilities for Each Competing Op Amp Model
- Following Simulation, *Breadboarding is Always Desirable and Necessary*

Figure 7-120: Used wisely, simulation is a powerful design tool

Of course, a successful first design step using an accurate op amp model by itself doesn't necessarily guarantee totally valid simulations. A simulation based on incomplete information has limited value. All parts of a target circuit should be modeled, including the surrounding passive components, various parasitic effects, and temperature changes. Then, the circuit needs to be verified in the lab by breadboarding and prototyping. A breadboard circuit is a quickly executed mockup of a circuit design using a semi-permanent lab platform, i.e., one that is in less than final physical form. It is intended to show real performance, but without the total physical environment. A good breadboard can often reveal behavior not predicted by SPICE, either because

of an incomplete model, external circuit parasitics, or numerous other reasons. However, by using SPICE along with intelligent breadboarding techniques, a circuit can be efficiently and quickly designed with reasonably good assurance of working properly on a prototype version, or even a final PCB. The following prototype phase is just one step removed from a final PCB, and may in fact be an actual test PCB, with nearly all design components incorporated, and with close to full performance.

The breadboard/prototype design steps are closely allied to simulation, usually following it in the overall design process. These are more fully discussed in subsequent sections.

Macromodel versus Micromodel

The distinction between *macromodel* and *micromodel* is often unclear. A micromodel uses the actual *transistor level* and other SPICE models of an IC device, with all active and passive parts fully characterized according to the manufacturing process. In differentiating this type of model from a macromodel, some authors use the term *device level model* to describe the resulting overall op amp model (see Reference 5). Typically, a micromodel is used in the actual design process of an IC.

A macromodel takes another route in emulating op amp performance. Taking into consideration final device performance, it uses ideal native SPICE elements to model observed behavior—as many as necessary. In developing a macromodel, a real device is measured in terms of lab and data sheet performance, and the macromodel is adjusted to match this behavior. Some aspects of performance may be sacrificed in doing this. Figure 7-121 compares the major pros and cons between macromodels and micromodels.

	METHODOLOGY	ADVANTAGES	DISADVANTAGES
MACROMODEL	Ideal Elements Model Device Behavior	Fast Simulation Time, Easily Modified	May Not Model All Characteristics
MICROMODEL	Fully Characterized Transistor Level Circuit	Most Complete Model	Slow Simulation, Convergence Difficulty, Nonavailability

Figure 7-121: Differentiating the Macromodel and Micromodel

There are advantages and disadvantages to both approaches. A micromodel can give a complete and accurate model of op amp circuit behavior under almost all conditions. But, because of a large number of transistors and diodes with nonlinear junctions, simulation time is very long. Of course, manufacturers are also reluctant to release such models, since they contain proprietary information. And, even though all transistors may be included, this isn't a guarantee of total accuracy, as the transistor models themselves don't cover all operational regions precisely. Furthermore, with a high node count, SPICE can have convergence difficulties, causing a failed simulation. This point would make a micromodel virtually useless for multiple amplifier active filters, for example.

On the other hand, a carefully developed macromodel can produce both accurate results and simulation time savings. In more advanced macromodels such as the ADSpice model described, transient and ac device performance can be closely replicated. Op amp nonlinear behavior can also be included, such as output voltage and current swing limits.

However, because these macromodels are still simplifications of real devices, all nonlinearities aren't modeled. For example, not all ADSpice models include common-mode input voltage range, or noise (while

more recent ones do). Typically, in model development parameters are optimized as may be critical to the intended application; for example, ac and transient response. Including every possible characteristic could lead to cumbersome macromodels that may even have convergence problems. Thus, ADSpice macromodels include those op amp behavior characteristics critical to intended performance for normal operating conditions, but not necessarily all nonlinear behavior.

The ADSpice Op Amp Macromodels

The basic ADSpice model was developed as an op amp macromodeling advance, and as an improved design tool for more accurate application circuit simulations. Since being introduced in 1990, it has become a standard op amp macromodel topology, as evidenced by industry adoption of the frequency shaping concepts (see References 6 and 7).

Prior to about 1990, a dominant op amp model architecture was the Boyle model (see Reference 8). This macromodel, developed in the early 70s, cannot accurately model higher speed amplifiers. The primary reason for this is that it has limited frequency shaping ability—only two poles and no zeroes. In contrast, the ADSpice model topology has a flexible and open architecture, allowing virtually unlimited pole and zero frequency shaping stages to be cascaded. This key difference provides much more accurate ac and transient response, vis-à-vis the more simplistic Boyle model topology.

An ADSpice model is comprised of three main portions, described as follows. The first of these is a combined input and gain stage, which will include transistor models as appropriate to the device being modeled (NPN or PNP bipolar, JFET, MOSFET, and so forth). Next are the synthetic pole and zero stages, which are comprised of ideal SPICE native elements. There may be only a few of these or there may be many, dependent on the complexity of the op amp's frequency response. Finally, there is an output stage, which couples the first two sections to the outside world.

Before describing these sections in detail, it is important to realize that many variations upon what is shown do in fact exist. This is due to not just differences from one op amp model to another, but also to evolutionary topology developments in op amp hardware, which in turn has led to corresponding modeling changes. For example, modern op amps often include either rail-rail output or input stages, or both. Consequently more recent developments in the ADSpice models have addressed these issues, along with corresponding model developments.

Furthermore, although the Boyle model and the original ADSpice models were designed to support *voltage feedback* op amp topologies, subsequent additions have added *current feedback* amplifier topologies. In fact, Reference 9 describes an ADSpice current feedback macromodel which appeared just shortly after the voltage feedback model of Reference 3. These current feedback macromodels are discussed in more detail next.

Input and Gain/Pole Stages

A basic ADSpice voltage feedback op amp macromodel input stage is shown in Figure 7-122. As noted, it uses what are (typically) the only transistors in the entire model, in this example the Q1-Q2 NPN pair, to the left on the diagram. These are needed to properly model an op amp's differential input stage characteristics. A basic tenet of this model topology is that this stage is designed for unity gain, by the proper choice of Q1-Q2 operating current and gain-setting resistors R3-R4 and R5-R6.

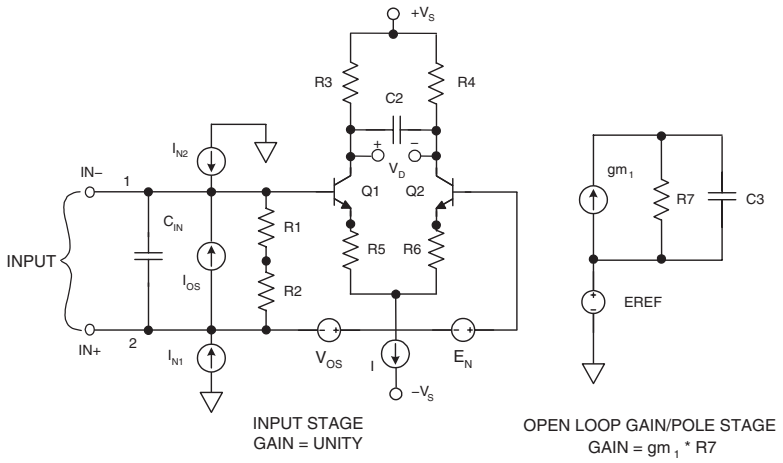


Figure 7-122: Input and gain/pole stages of ADSpice macromodel

Although this example uses NPN transistors, the input stage is easily modified to use PNP bipolars, JFET, or MOSFET devices. The rest of the input stage uses simple SPICE elements such as resistors, capacitors, and controlled sources.

The open-loop gain versus frequency characteristics of the modeled op amp is provided by the gain stage, to the right in the diagram. Here controlled source gm_1 senses the differential collector voltage V_D from the input stage, converting this voltage to a proportional current. The gm_1 output current flows in load resistor R_7, producing a single ended voltage referenced to an internal voltage, EREF. Typically, this voltage is derived as a supply voltage midpoint, and is used throughout the model.

By simply making the gm_1–R_7 product equal to the specified gain of the op amp, this stage produces the entire open-loop gain of the macromodel. This design factor means that all other model stages operate at unity gain, a feature leading to significant flexibility in adding and deleting subsequent stages. This approach allows the quick synthesis of the complex ac characteristics typical of high performance, high speed op amps. In addition, this stage also provides the dominant pole of the amplifier's ac response. The open-loop pole frequency is set by selection of capacitor C3, as noted in the diagram.

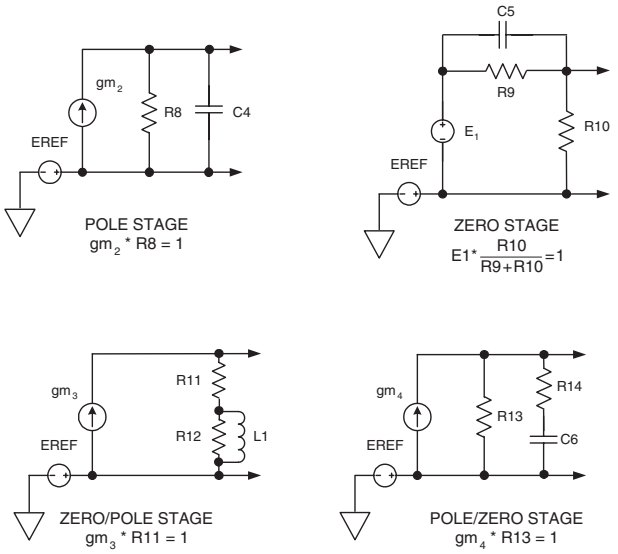


Figure 7-123: The frequency-shaping stages possible within the ADSpice model

Frequency-Shaping Stages

Following the gain stage of the macromodel is a variable but unlimited number of pole and/or zero stages which, in combination, provide frequency response shaping. Typical topologies for these stages are as shown in the Figure 7-123 diagram. The stages can be either a single pole or a single zero, or combined pole/zero or zero/pole stages. All such stages have a dc transfer gain of unity, and a given amplifier type can have all or just a few of these stages, as may be require to synthesize its response.

The pole or zero frequency is set by the combination of the resistor(s) and capacitor, or resistor(s) and inductor, as may be the case. Because an infinite number of values are possible in SPICE, choice of RC values is somewhat arbitrary, and a wide range work. Early ADSpice models used relatively high values, while later ones employ lower values to reduce noise (described in more detail later). In all instances, it is assumed that each stage provides zero loading to the driving stage. The stages shown reflect no particular op amp, but example principles can be found within the OP27 model (see Reference 10).

Because all of these frequency-shaping stages are dc-coupled and have unity gain, any number of them can be added or deleted, with no affect on the model's low frequency response. Most importantly, the high frequency gain and phase response can be precisely tailored to match a real amplifier's response. The benefits of this frequency-shaping flexibility are especially apparent in performance comparisons of the ADSpice model closed loop pulse response and stability analysis, versus that of a more simplistic model. This point is demonstrated by a later example.

Macromodel Output Stages

A general form of the output stage for the ADSpice model, shown in Figure 7-124, models a number of important op amp characteristics. The Thevenin equivalent resistance of R_{O1} and R_{O2} mimics the op amp's dc open-loop output impedance, while inductor L_O models the rise in impedance at high frequencies. A unity gain characteristic for the stage is set by the g_7–R_{O1} and g_8–R_{O2} products.

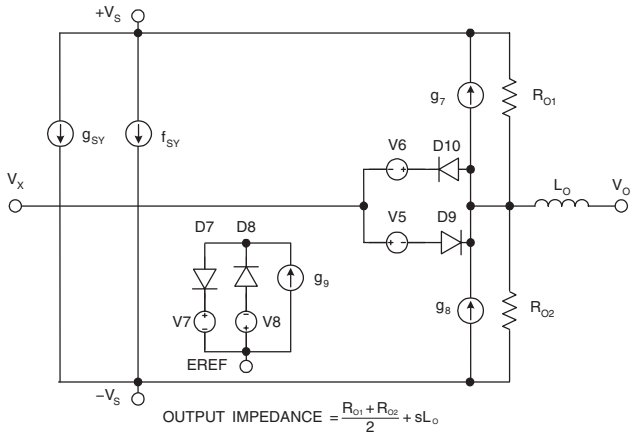


Figure 7-124: General-purpose macromodel output stage

Additionally, output load current is correctly reflected in the supply currents. This feature is a significant improvement over the Boyle model, because the power consumption of the loaded circuit can be analyzed accurately. Furthermore, circuits using the op amp supply currents as part of the signal path can also be correctly simulated. The output stage shown is not intended to reflect any particular op amp, but close similarity is found within the AD817 model (see Reference 11).

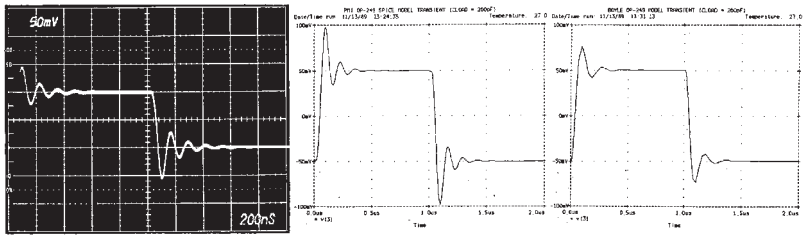
With the recent advent of numerous rail-rail output stage op amps, a number of customized model topologies have been developed. This expands the ADSpice library to include rail-rail model behavior, matching op amp architectures using P and N MOSFET devices, as well as bipolar devices. Characteristically, a rail-rail output stage includes several key differentiating performance points. First and foremost is the ability to swing the op amp output to within a few mV of both supplies. A second point is the fact that such an output stage has a voltage gain greater than one, and a third is the relatively high output impedance (high as contrasted to traditional emitter follower outputs).

Examples of several modeling approaches to rail-rail output stages are found in the ADI SPICE macromodel library. Reference 12 employs CMOS devices to realize a rail-rail output, while Reference 13 uses bipolar devices to the same end. The macromodels of References 14 and 15 use synthesis techniques to model rail-rail outputs. References 16–18 utilize combinations of selected discrete device models and synthesis techniques, to realize rail-rail output operation for both op amp and in amp devices.

In addition to rail-rail output operation, many modern op amps also feature rail-rail *input stages*. Such stages essentially duplicate, for example, an NPN-based differential stage with a complementary PNP stage, both stages operating in parallel. This allows the op amp to provide a CM range that includes both supply rails. This performance feature can also be accomplished within CMOS op amps, using both a P and N type MOS differential pairs. Model examples reflecting rail-rail input stages include References 13, 14, and 17.

Model Transient Response

The performance advantage of the multiple pole/zero stages is readily demonstrated in a transient pulse response test, as in Figure 7-125. This figure compares an actual OP249 op amp, the ADSpice model, and the Boyle model. It reveals the improved execution resulting from the unlimited number of poles and zeros in this model.



VERTICAL SCALE: 50mV / div.
HORIZONTAL SCALE: 200ns / div.

LOAD = 260pF

Figure 7-125: A pulse response comparison of an OP249 follower (left) model favors the ADSpice model in terms of fidelity (center), but not the Boyle (right)

The difference is easily apparent from this transient analysis plot for a unity gain follower circuit. An OP249 amplifier was used, with the output connected to the inverting input, and a 260 pF capacitive load.

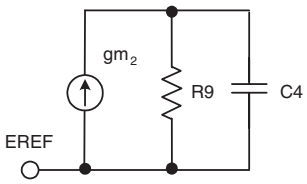
This results in ringing, as seen in the op amp response (left). Note that the ADSpice model accurately predicts the amount of overshoot and frequency of the damped ringing (center). In contrast, the Boyle model (right) predicts about half the overshoot and significantly less ringing.

The Noise Model

An important enhancement to the ADSpice model is the ability to realistically model noise performance of an op amp. The capability to model a circuit's noise in SPICE can be appreciated by anyone who has tried to analyze noise by hand. A complete analysis is an involved and tedious task that involves adding all the individual noise contributions from all active devices and all resistors, and referring them to the input.

To aid this task, the ADSpice model was enhanced to include noise generators that accurately mimic the broadband and 1/f noise of an actual op amp. Conceptually, this involves first making an existing model noiseless, and then adding discrete noise generators, so as to emulate the target device. As noted earlier, all ADI models aren't necessarily designed for this noise-accurate performance. Selected device models are designed for noise however, when their typical uses include low noise applications.

The first step is an exercise in scaling down the model internal impedances. For example, by reducing the resistances in the pole/zero stages from a base resistance of 1E6 Ω to 1 Ω, total noise is reduced dramatically, as figure 7-126 illustrates.



	CASE	
	"Noisy"	"Noiseless"
R9	$1x10^6\Omega$	1Ω
gm_2	$1x10^{-6}$	1.0
C4	$159x10^{-15}F$	$159x10^{-9}F$
Noise	129nV/ √Hz	129pV/√Hz

Figure 7-126: Towards achieving low noise operation, a first design step is the reduction of pole/zero cell impedances to low values

For the "Noisy" column of the table, the noise from the pole stage shown with a large R9 resistor value is $129\ \mathrm{nV}/\sqrt{\mathrm{Hz}}$. But when this resistor is scaled down by a factor of 10^6, to 1 Ω, as in the "Noiseless" column, stage noise is $129\ \mathrm{pV}/\sqrt{\mathrm{Hz}}$. Note also that transconductance and capacitance values are also scaled by the same factor, maintaining the same gain and pole frequency. To make the model's input stage noiseless, it is operated at a high current and with reduced load resistances, making noise contributions negligible. Extending these techniques to the entire model renders it essentially noiseless.

Once global noise reduction is achieved, independent noise sources are added, one for voltage noise and two for current noise. The basic noise source topology used is like Figure 7-127, and it can be set up to produce both voltage and current noise outputs.

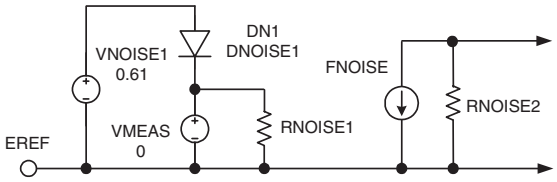


Figure 7-127: A basic SPICE noise generator is formed with diodes, resistors, and controlled sources

Note that, within SPICE, semiconductor models can generate 1/f (flicker) noise. The noise generators use diodes such as DN1 to produce this portion of the noise, modeling the 1/f noise of the op amp. By properly specifying diode model parameters and bias voltage VNOISE1, the 1/f noise is tailored to match the op amp. The noise current from DN1 passes through a zero voltage source. Here VMEAS is being used as a measurement device, combining the 1/f noise from DN1 and the broadband noise from RNOISE1.

RNOISE1 is selected for a value providing an appropriate broadband noise. The combined noise current in VMEAS is monitored by FNOISE, and appears as a voltage across RNOISE2. This voltage is then injected in series with one amplifier input via a controlled voltage source, such as E_N of Figure 7-122. Either FNOISE or a controlled voltage source coefficient can be used for overall noise voltage scaling.

Current noise generation is similar to the above, except that the RNOISE2 voltage producing resistor isn't used, and two current-controlled sources drive the amplifier inputs. With all noise generators symmetrical about ground, dc errors aren't introduced.

Current Feedback Amplifier Models

As noted previously, a new model topology was developed for current feedback amplifiers, to accommodate their unique input stage structure (see Reference 9). The model uses a topology as shown in Figure 7-128 for the input and gain stages. The remaining model portions (not shown) contain multiple pole/zero stages and the output stage, and are essentially the same as voltage feedback amplifiers, described above.

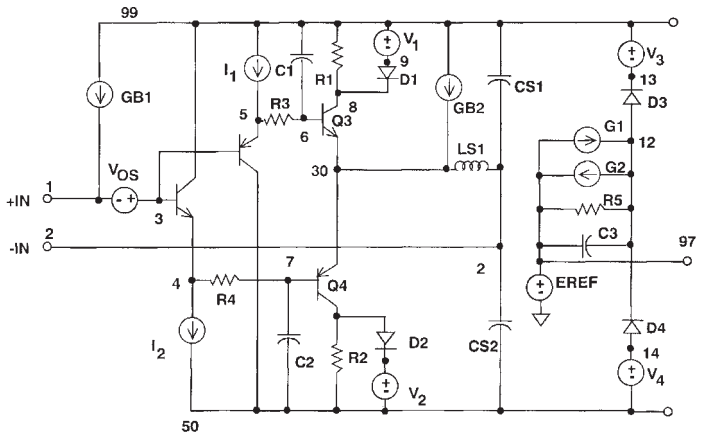


Figure 7-128: Input and gain stages of current feedback op amp macromodel

The four bipolar transistor input stage resembles actual current feedback amplifiers, with a high impedance noninverting input (+IN) and a low impedance inverting input (–IN). In current feedback amplifiers, the maximum slew rate is very high, because dynamic slew current isn't limited to a differential pair tail current (as in voltage feedback op amps). In current feedback op amp designs, much larger amounts of error current can flow in the inverting input, as developed by the feedback network. Internally, this current flows in either Q3 or Q4, and charges compensation capacitor C3 via current mirrors.

The current mirrors of the ADSpice model are actually voltage controlled current sources in the gain stage, G1 and G2. They sense voltage drops across input stage resistors R1 and R2, and translating this into a C3 charging current. By making the value of G1 and G2 equal to the R1-R2 reciprocal, the slew currents will be identical. By clamping the R1-R2 voltage drops via D1–V1 and D2–V2, the maximum current is limited, which thus sets the highest slew rate. Open loop gain or transresistance of the model is set by R5, and the open loop pole frequency by C3–R5 (as described previously, Figure 7-122). The output from across R5–C3 (node 12) drives the model's succeeding frequency-shaping stages, and EREF is again an internal reference voltage.

One of the unique properties of current feedback amplifiers is that bandwidth is a function of the feedback resistor and the internal compensation capacitor, C3. The lower the feedback resistor, the greater the bandwidth, until a practical lower limit is reached, i.e., the value at which the part oscillates. As the model includes a low impedance inverting input, it accurately mimics real part behavior as R_F is altered. Figure 7-129 compares the ADSpice model to the actual device for an AD811 video amplifier. As shown, the model accurately predicts the gain roll-off at the much lower frequency for the 1 kΩ feedback resistor as opposed to the 500 Ω resistor.

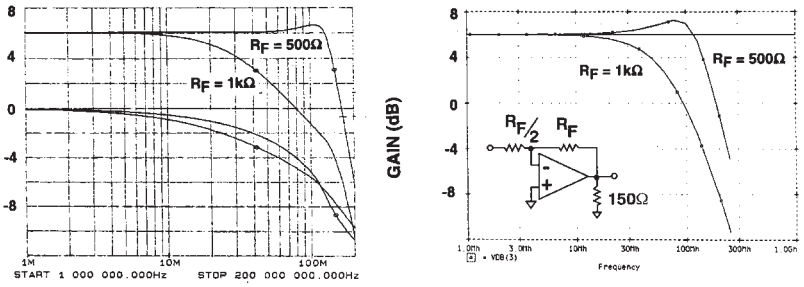


Figure 7-129: Comparison of a real AD811 current feedback op amp (left) with macromodel (right) shows similar characteristics as feedback resistance is varied

The current feedback amplifier input and gain stage is an enhancement to the ADSpice model that increases flexibility in modeling different op amp devices, and provides a net increase in design cycle speed.

Simulation Must Not Replace Breadboarding

No matter how accurate the models, or how much confidence you have with simulations, *SPICE analysis alone should never totally replace breadboarding*. As part of a layout and the actual devices existing within a real world PCB assembly, there are second and third order effects that can easily become relevant to performance. By and large, SPICE will never "know" of such things, unless explicitly entered into the SPICE netlist. However, this may be either difficult or outright impossible. The user may not be aware of some things before a PCB is built and tested within the final system—spurious signal coupling, the effects of crosstalk, the inevitable parasitic capacitance, inductance, and resistance—on and on goes the list. It is virtually impossible to include all of these effects in a simulation. Without actually building a PCB, and operating it under the intended conditions, the user will not have any data whatsoever on the magnitudes involved.

Furthermore, remember the fact that no macromodel includes all op amp characteristics. For example, exceeding the input voltage range can cause nonlinear behavior in an op amp, which is not necessarily included in its model. Because of such effects that a simulation might not predict, it is necessary to breadboard the circuit.

Even with models as comprehensive as those of the ADSpice library, external effects can easily cause a circuit to work improperly. As noted, PCB parasitics can significantly alter the frequency performance in high speed designs. Such parasitics are easily overlooked in a SPICE simulation, but a breadboard will reveal the problems.

Ultimately, simulation and breadboarding should be used together to maximize the design efficiency. Figure 7-130 summarizes these pro and con points of analog simulations.

- Understand What's Real (Hardware), and What Isn't (SPICE)
- Use Breadboarding/Prototyping as Final Design Verification
- Be Aware of Non-Modeled Op Amp Characteristics
- Pay Attention to PCB Parasitics Impacting Circuit Behavior

Figure 7-130: Some analog simulation caveats

Obviously, the designer needs to be wary of what SPICE can/cannot do, and the necessity of closely allying simulations with breadboarding and prototyping.

Simulation is a Tool to be Used "Wisely"

It must be remembered that while simulation is an extremely powerful tool, it must be used wisely to realize its full benefits. This includes knowing models well, understanding PCB and other parasitic effects, and anticipating the results. For example, consider a simple differential amplifier comprised of an op amp and four equal resistors, to be analyzed for common-mode rejection ratio (CMRR) performance. At low frequencies, CMRR will be dominated by resistor mismatch, while at higher frequencies it is dominated by op amp CMRR performance. However, a SPICE simulation will only show this if the external resistors are realistically mismatched, and the op amp model used also properly treats not only dc CMRR, but also CMRR reduction at higher frequencies. If these critically important points are overlooked in the analysis, then an optimistic result will shows excellent CMRR performance over the entire circuit bandwidth. Unfortunately, this is simply wrong. Alternatively, substituting into the netlist resistors mismatched by their specified tolerances as well as an ADSpice model (which *does* have CMRR frequency effects modeled) the end results will be quite different. CMRR performance at low frequencies will be limited by resistor mismatch errors, and will degrade at higher frequencies, as would a real op amp device with CMRR versus frequency effects.

Know the Models

Using various dc and ac tests, any op amp macromodel can be checked for accuracy and functional completeness. Specialized test simulations can also be devised for other op amp parameters important for a particular analysis. All this is critically important, as knowing a model's capabilities ahead of time can help prevent many headaches later.

Understand PCB Parasitics

Even if the model passes all preliminary tests, caution still should be exercised. As noted, PCB parasitics can have significant impact on a circuit's performance. This is especially true for high speed circuits. A few picofarads of capacitance on the input node can make the difference between a stable circuit and one that oscillates. Thus, these effects need to be carefully considered when simulating the circuit to achieve meaningful results.

To illustrate the impact of PCB parasitics, the simple voltage follower circuit of Figure 7-131 (left) was built twice. The first time this was on a carefully laid out PCB, and the second time on a component plug-in type of prototype board. An AD847 op amp is used because of its 50 MHz bandwidth, which makes the parasitic effects much more critical (smaller C values will have a greater effect on results).

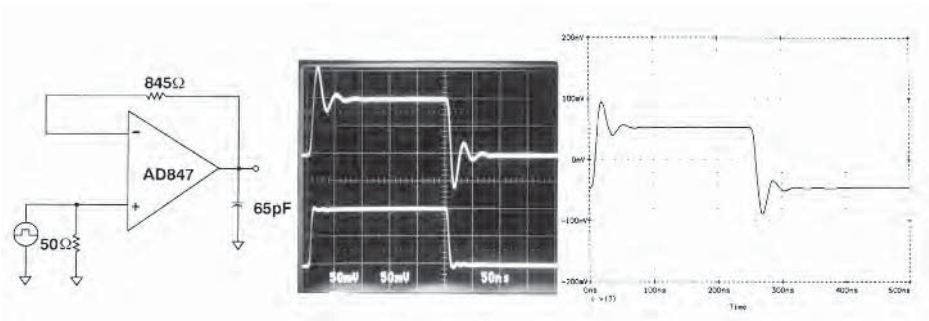


Figure 7-131: With care and low parasitic effects in the PCB layout, results of lab testing (center) and simulation (right) can converge

As the results above indicate, this circuit executed on a properly laid out PCB has a clean response with minor overshoot and ringing (center picture). The SPICE model results also closely agree with the real part, showing a corresponding simulation (right picture).

On the other hand, the same circuit built on the plug-in prototype board shows distinctly different results. In general, it shows much worse performance, due to the relatively high nodal capacitances around the op amp inputs, which degrade the square wave response to severe ringing, much less than full capability of the part.

This is shown in Figure 7-132 in the center and right pictures, respectively. The voltage follower circuit on the left shows the additional capacitances as inherent to the prototype board. With this test circuit and corre-

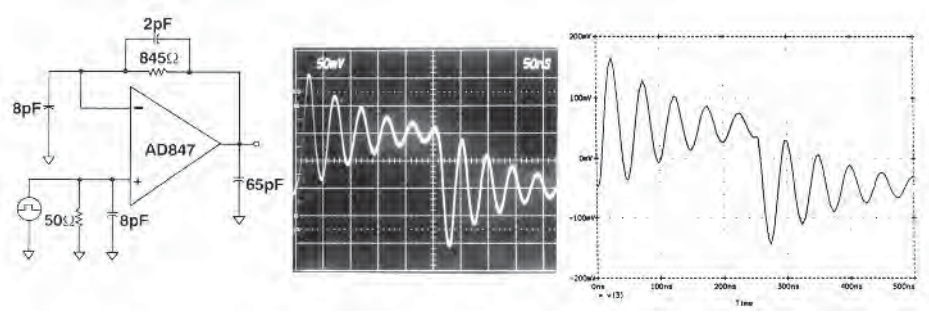


Figure 7-132: Without low parasitics, lab testing results (center) and parallel simulation (right) still show convergence—with a poorly damped response

sponding analysis, there was (initially) no agreement between the poor lab test, and the parallel SPICE test. However, when the relevant PCB parasitic capacitances are included in the SPICE file, then the simulation results do agree with the real circuit, as noted in the right picture.

This example illustrates several key points. One, PCB parasitics can easily make a high speed circuit behave much differently from a simplistic SPICE analysis. Secondly, when the SPICE netlist is adjusted to more reasonably reflect the parasitic elements of a PCB, the simulation results do compare with the actual lab test. Finally, a point that should be obvious, a clean PCB layout with minimal parasitics is critically important to high speed designs. To put this in a broader perspective, op amps of today are capable of operating to 1 GHz or more.

Another interesting point is that the simulation can be used as a rough measure of the PCB layout design. If the simulation, without any parasitics, agrees with the PCB, there is a reasonable assurance that PCB is laid out well.

Parasitic PCB elements are not the only area that may cause differences between the simulation and the breadboard. A circuit may exhibit nonlinear behavior during power-on that will cause a device to lock up. Or, a device may oscillate due to insufficient power supply decoupling or lead inductance. SPICE circuits need *no* bypassing, *but real world ones always do*. It is, practically speaking, impossible to anticipate all normal or abnormal operating conditions to which an amplifier might be subjected.

Thus, it is always important that circuits be breadboarded and thoroughly checked in the lab. Careful forethought in these stages of design helps minimize any unknown problems from showing up when the final PCBs are manufactured.

Simulation Speeds the Design Cycle

Simulation is very effective in the initial design phase, to try out different ideas and circuit configurations. When a circuit topology has been decided upon and tested in SPICE, a breadboard can be built. If the simulation was done carefully, the breadboard has good likelihood of working correctly without significant modifications.

When the simulation and the actual results correlate, the circuit can easily be altered in SPICE to perform many different types of analysis. For example, it is much easier to try to optimize the circuit while working within SPICE, as opposed to repeatedly modifying a breadboard. Quick substitutions of the op amps and components can be made in SPICE and the results immediately viewed.

Worst-case and sensitivity analyses are also done in SPICE much easier than on paper, and with multiple SPICE runs, the sensitivity to a certain parameter can be determined. Consider for example an analysis of a multistage active filter, for all possible combinations of component values. This is a nightmare, if not impossible, either by hand or in the lab, but valid results for response extremes can be obtained relatively easily via a SPICE Monte Carlo option, providing greater design confidence.

Some general SPICE-related points are useful towards an overall healthy perspective on this, as shown in Figure 7-133.

- Quickly Check Circuit Ideas
- Eases Circuit Optimization
- Allows Component Alteration for Worst Case and Sensitivity Analyses
- Allows Quick Comparison of Different Op Amps

Figure 7-133: Some useful points on using SPICE simulations

While simulation cannot reasonably be allowed to replace breadboarding, the two can and should be used together, to increase the efficiency of a design cycle.

SPICE Support

A variety of industry vendors offer SPICE analysis packages for various computer platforms, including the PC. The first of these and among the most popular is PSpice®, a commercial program that now includes allied packages for both schematic capture and PCB layout (see Reference 19). In addition, many vendors also offer low or no cost limited capability student versions of their SPICE programs.

Model Support

The ADSpice model library is available in several different forms. Included within it are models of several IC device types, in addition to the op amps discussed above. These are for in amps, analog multipliers, voltage references, analog switches, analog multiplexers, matched transistors, and buffers. Individual op amp models are available as listings on many data sheets. Electronic ASCII text files of the model library are found from either the ADI website (see References), the Analog Devices Literature Center via 1-800-ANALOGD (1-800-262-5643), or on the ADI support CD.

Acknowledgments:

There have been numerous model authors of SPICE macromodels for the ADI library. These include Derek Bowers, Eberhard Brunner, Joe Buxton, Vic Chang, Bob Day, Wes Freeman, Adolfo Garcia, Antonio Germano, John Hayes, John McDonald, Troy Murphy, Al Neves, Steve Reine, Bill Tolley, Tim Watkins, and James Wong.

Breadboard and Prototyping Techniques

A basic principle of a breadboard or a prototype structure is that it is a *temporary* one, designed to test the performance of an electronic circuit or system. By definition it must therefore be easy to modify, particularly so for a breadboard.

There are many commercial prototyping systems, but unfortunately for the analog designer, almost all of them are designed for prototyping *digital* systems. In such environments, noise immunities are hundreds of millivolts or more. Prototyping methods commonly used include noncopper-clad Matrix board, Vectorboard, wire-wrap, and plug-in breadboard systems. Quite simply, these all are unsuitable for high performance or high frequency analog prototyping, because of their excessively high parasitic resistance, inductance, and capacitance levels. Even the use of standard IC sockets is inadvisable in many prototyping applications (more on this below).

Figure 7-134 summarizes a number of key points on selecting a useful analog breadboard and/or prototyping system, which follows.

- Always Use a Ground Plane for Precision or High Frequency Circuits
- Minimize Parasitic Resistance, Capacitance, and Inductance
- If Sockets Are Required, Use “Pin Sockets” (“Cage Jacks”)
- Pay Equal Attention to Signal Routing, Component Placement, Grounding, and Decoupling in Both the Prototype and the Final Design
- Popular Prototyping Techniques:
  - Freehand “Deadbug” Using Point-to-Point Wiring
  - “Solder-mount”
  - Milled PC Board from CAD Layout
  - Multilayer Boards: Double-Sided with Additional Point-to-Point Wiring

Figure 7-134: A summary of analog prototyping system key points

One of the more important considerations in selecting a prototyping method is the requirement for a large-area ground plane. This is required for high frequency circuits as well as low speed precision circuits, especially when prototyping circuits involving ADCs or DACs. The differentiation between *high speed* and *high precision* mixed-signal circuits is difficult to make. For example, 16+-bit ADCs (and DACs) may operate on high speed clocks (>10 MHz) with rise and fall times of less than a few nanoseconds, while the effective throughput rate of the converters may be less than 100 kSPS. Successful prototyping of these circuits requires that equal (and thorough) attention be given to good high speed and high precision circuit techniques.

Deadbug Prototyping

A simple technique for analog prototyping uses a solid copper-clad board as a ground plane (see References 20 and 21). In this method, the ground pins of the ICs are soldered directly to the plane, and the other components are wired together above it. This allows HF decoupling paths to be very short indeed. All lead lengths should be as short as possible, and signal routing should separate high level and low level signals. Connection wires should be located close to the surface of the board to minimize the possibility of stray inductive coupling. In most cases, 18-gauge or larger insulated wire should be used. Parallel runs should not be “bundled” because of possible coupling. Ideally the layout (at least the relative placement of

the components on the board) should be similar to the layout to be used on the final PCB. This approach is often referred to as *deadbug prototyping*, because the ICs are often mounted upside down with their leads up in the air (with the exception of the ground pins, which are bent over and soldered directly to the ground plane). The upside-down ICs look like deceased insects, hence the name.

Figure 7-135 shows a hand-wired "deadbug" analog breadboard. This circuit uses two high speed op amps and, in fact, gives excellent performance in spite of its lack of esthetic appeal. The IC op amps are mounted upside down on the copper board with the leads bent over. The signals are connected with short point-to-point wiring. The characteristic impedance of a wire over a ground plane is about 120 Ω, although this may vary as much as ±40%, depending on the distance from the plane. The decoupling capacitors are connected directly from the op amp power pins to the copper-clad ground plane. When working at frequencies of several hundred MHz, it is a good idea to use only one side of the board for ground. Many people drill holes in the board and connect the sides together by soldering short pieces of wire. If care isn't taken, this may result in unexpected ground loops between the two sides of the board, especially at RF frequencies.

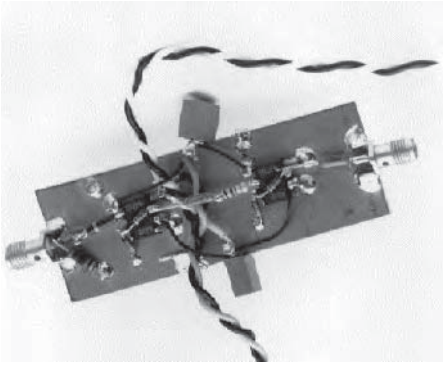


Figure 7-135: A "deadbug" analog breadboard

Pieces of copper-clad board may be soldered at right angles to the main ground plane to provide screening, or circuitry may be constructed on both sides of the board (with through-hole connections) with the board itself providing screening. For this, the board will need corner standoffs to protect underside components from being crushed.

When the components of a breadboard of this type are wired point-to-point in the air (a type of construction strongly advocated by Bob Pease (see Reference 21) and sometimes known as "bird's nest" construction) there is always the risk of the circuitry being crushed and resulting short-circuits. Also, if the circuitry rises high above the ground plane, the screening effect of the ground plane is diminished, and interaction between different parts of the circuit is more likely. Nevertheless, the technique is very practical and widely used because the circuit may easily be modified (this of course assumes the person doing the modifications is adept with soldering techniques).

Another prototype breadboard variation is shown in Figure 7-136. Here the single-sided copper-clad board has pre-drilled holes on 0.1" centers (see Reference 22). Power buses are used at the top and bottom of the board. The decoupling capacitors are used on the power pins of each IC. Because of the loss of copper area due to the predrilled holes, this technique does not provide as low a ground impedance as a completely covered copper-clad board of Figure 7-135, so be forewarned.

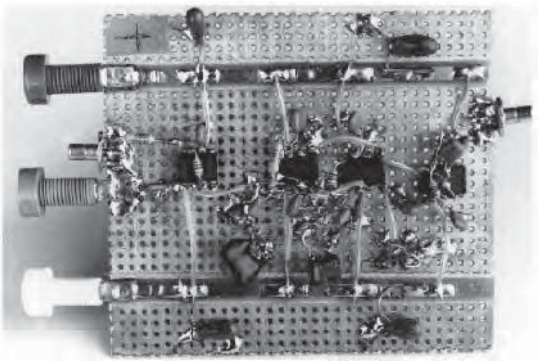


Figure 7-136: A "deadbug" prototype using 0.1" predrilled single-sided, copper-clad printed board material

In a variation of this technique, the ICs and other components are mounted on the noncopper-clad side of the board. The holes are used as vias, and the point-to-point wiring is done on the copper-clad side of the board. Note that the copper surrounding each hole used for a via must be drilled out, to prevent shorting. This approach requires that all IC pins be on 0.1" centers. For low frequency circuits, low profile sockets can be used, and the socket pins then will allow easy point-to-point wiring.

Solder-Mount Prototyping

There is a commercial breadboarding system that has most of the advantages of the above techniques (robust ground, screening, ease of circuit alteration, low capacitance, and low inductance) and several additional advantages: it is rigid, components are close to the ground plane and, where necessary, node capacitances and line impedances can be easily calculated. This system is made by Wainwright Instruments and is available in Europe as "Mini-Mount" and in the USA (where the trademark "Mini-Mount" is the property of another company) as "Solder-Mount" (see References 23 and 24).

Solder-Mount consists of small pieces of PCB with etched patterns on one side and contact adhesive on the other. These pieces are stuck to the ground plane, and components are soldered to them. They are available in a wide variety of patterns, including ready-made pads for IC packages of all sizes from 8-pin SOICs to 64-pin DILs, strips with solder pads at intervals (which intervals range from 0.040" to 0.25", the range includes strips with 0.1" pad spacing which may be used to mount DIL devices), strips with conductors of the correct width to form microstrip transmission lines (50 Ω, 60 Ω, 75 Ω or 100 Ω) when mounted on the ground plane, and a variety of pads for mounting various other components. Self-adhesive tinned copper strips and rectangles (LO-PADS) are also available as tie-points for connections. They have a relatively high capacitance to ground and therefore serve as low inductance decoupling capacitors. They come in sheet form and may be cut with a knife or scissors.

The main advantage of Solder-Mount construction over "bird's nest" or "deadbug" is that the resulting circuit is far more rigid and, if desired, may be made far smaller (the latest Solder-Mounts are for surface-mount devices and allow the construction of breadboards scarcely larger than the final PCB, although it is generally more convenient if the prototype is somewhat larger). Solder-Mount is sufficiently durable that it may be used for small quantity production as well as prototyping.

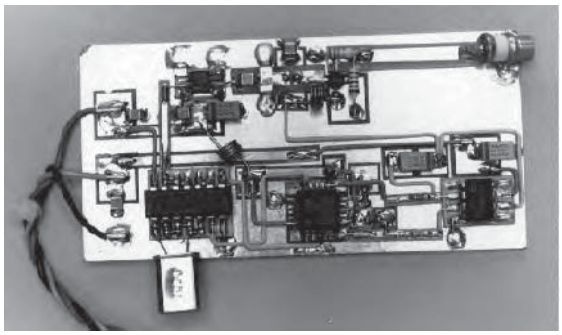


Figure 7-137: A "Solder-Mount" constructed prototype board

Figure 7-137 shows an example of a 2.5 GHz phase-locked-loop prototype, built with Solder-Mount techniques. While this is a high speed circuit, the method is equally suitable for the construction of high resolution low frequency analog circuitry.

A particularly convenient feature of Solder-Mount at VHF is the relative ease with which transmission lines can be formed. As noted earlier, if a conductor runs over a ground plane, it forms a microstrip transmission line. The Solder-Mount components include strips that form microstrip lines when mounted on a ground plane (they are available with impedances of 50 Ω, 60 Ω, 75 Ω, and 100 Ω). These strips may be used as transmission lines for impedance matching or, alternately, more simply as power buses. Note that glass fiber/epoxy PCB is somewhat lossy at VHF/ UHF, but losses will probably be tolerable if microstrip runs are short.

Milled PCB Prototyping

Both "deadbug" and "Solder-Mount" prototypes become tedious for complex analog circuits, and larger circuits are better prototyped using more formal layout techniques.

There is a prototyping approach that is but one step removed from conventional PCB construction, described as follows. This is to actually lay out a double-sided board, using conventional CAD techniques. PC-based software layout packages offer ease of layout as well as schematic capture to verify connections (see References 25 and 26). Although most layout software has some degree of autorouting capability, this feature is best left to digital designs. The analog traces and component placements should be done by hand, following the rules discussed elsewhere in this chapter. After the board layout is complete, the software verifies the connections per the schematic diagram net list.

Many designers find that they can make use of CAD techniques to lay out simple boards. The result is a pattern-generation tape (or Gerber file) which would normally be sent to a PCB manufacturing facility where the final board is made.

Rather than use a PCB manufacturer, however, automatic drilling and milling machines that accept the PG tape directly are available (see References 27 and 28). An example of such a prototype circuit board is shown in Figure 7-138 (top view).

These systems produce either single or double-sided circuit boards directly, by drilling all holes and using a milling technique to remove conductive copper, thus creating the required insulation paths and, finally, the finished prototype circuit board. The result can be a board functionally quite similar to a final manufactured double-sided PCB.

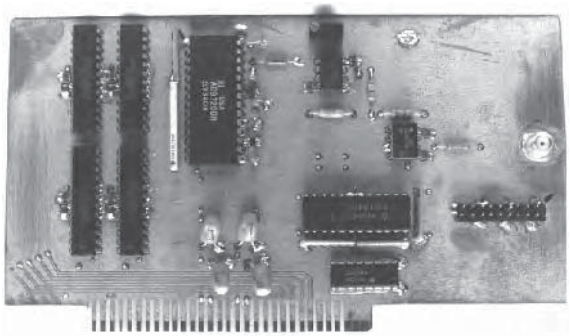


Figure 7-138: A milled circuit construction prototype board (top view)

However, it should be noted that a chief caveat of this method is that there is no "plated-through" hole capability. Because of this, any conductive "vias" required between the two layers of the board must be manually wired and soldered on both sides.

Minimum trace widths of 25 mils (1 mil = 0.001") and 12 mil spacing between traces are standard, although smaller trace widths can be achieved with care. The minimum spacing between lines is dictated by the size of the milling bit used, typically 10 to 12 mils.

A bottom-side view of this same milled prototype circuit board is shown in Figure 7-139. The accessible nature of the copper pattern allows access to the traces for modifications.

Perhaps the greatest single advantage of the milled circuit type of prototype circuit board is that it approaches the format of the final PCB design most closely. By its very nature, however, it is basically limited to only single or double-sided boards.

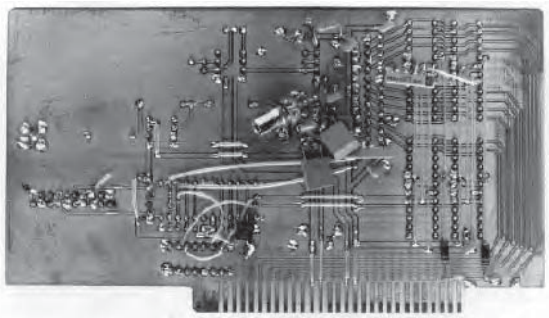


Figure 7-139: A milled circuit construction prototype board (bottom view)

Beware of Sockets

IC sockets can degrade the performance of high speed or high precision analog ICs. Although they make prototyping easier, even *low profile* sockets often introduce enough parasitic capacitance and inductance to degrade the performance of a high speed circuit. If sockets must be used, a socket made of individual *pin sockets* (sometimes called *cage jacks*) mounted in the ground plane board may be acceptable, as in Figure 7-140.

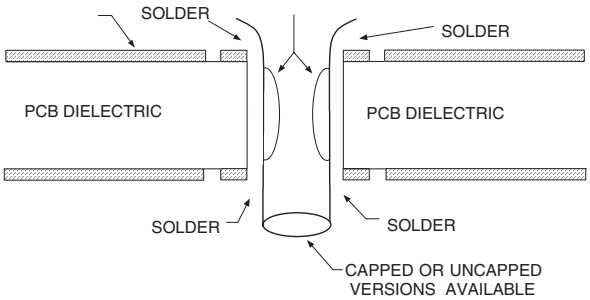


Figure 7-140: When necessary, use pin sockets for minimal parasitic effects

To use this technique, clear the copper (on both sides of the board) for about 0.5 mm around each ungrounded pin socket, Then solder the grounded socket pins to ground, on both sides of the board.

Both capped and uncapped versions of these pin sockets are available (AMP part numbers 5-330808-3, and 5-330808-6, respectively). The pin sockets protrude through the board far enough to allow point-to-point wiring interconnections.

Because of the spring-loaded gold-plated contacts within the pin socket, there is good electrical and mechanical connection to the IC pins. Multiple insertions, however, may degrade the performance of the pin socket, so this factor should be kept in mind.

Note also that the uncapped versions allow the IC pins to extend out the bottom of the socket. This feature leads to an additional useful function. Once a prototype using the pin sockets is working and no further changes are to be made the IC pins can be soldered directly to the bottom of the socket. This establishes a rugged, permanent connection.

Some Additional Prototyping Points

The prototyping techniques discussed so far have been limited to single or double-sided PCBs. Multilayer PCBs do not easily lend themselves to standard prototyping techniques. If multilayer board prototyping is required, one side of a double-sided board can be used for ground and the other side for power and signals. Point-to-point wiring can be used for additional runs which would normally be placed on the additional layers provided by a multilayer board. However, it is difficult to control the impedance of the point-to-point wiring runs, and the high frequency performance of a circuit prototyped in this manner may differ significantly from the final multilayer board.

Other difficulties in prototyping may occur with op amps or other linear devices having bandwidths greater than a few hundred megahertz. Small variations in parasitic capacitance (<1 pF) between the prototype and the final board can cause subtle differences in bandwidth and settling time.

Sometimes, prototyping is done with DIP packages, when the final production package is an SOIC. *This is not recommended.* At high frequencies, small package-related parasitic differences can account for different performance, between prototype and final PCB. To minimize this effect, always prototype with the final packages.

Evaluation Boards

Most manufacturers of analog ICs provide *evaluation boards,* usually at a nominal cost. These boards allow customers to evaluate ICs without constructing their own prototypes. Regardless of the product, the manufacturer has taken proper precautions regarding grounding, layout, and decoupling to ensure optimum device performance. Where applicable, the evaluation PCB artwork is usually made available free of charge, should a customer wish to copy the layout directly or make modifications to suit an application.

General-Purpose Op Amp Evaluation Boards

Evaluation boards can either be dedicated to a particular IC, or they can be general-purpose. With op amps the most universal linear IC, it is logical that evaluation boards be developed for them, to aid easy applications. However, it is also important that a good quality evaluation board avoid the parasitic effects discussed above. An example is the general-purpose dual amplifier evaluation board of in Figure 7-141 (see Reference 29).

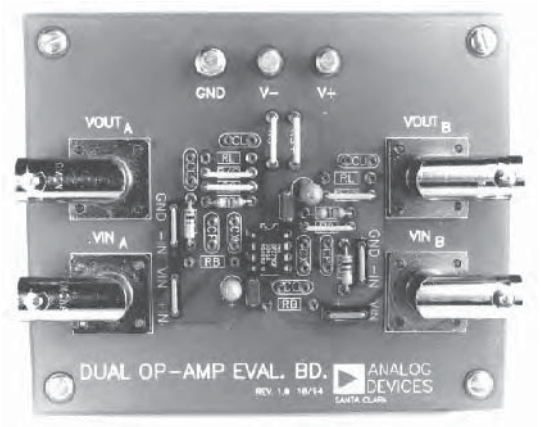


Figure 7-141: A general-purpose op amp evaluation board allows fast, easy configuration of low frequency op amp circuits

This board uses pin sockets for any standard dual op amp pinout device, and a flexible set of component jumper locations allows it to be setup for inverting or noninverting amplifiers. Various gains can be configured by choice of the component values, in either ac- or dc-coupled configurations.

The card design provides signal coupling via BNC connectors at input and output. It also uses external lab power supplies, which are wired to the lug terminals at the top. The card does, however, contain local supply voltage decoupling and bypassing components.

These general-purpose boards are intended for medium to high precision uses at frequencies below 10 MHz, with moderate op amp input currents. For higher operating speeds, a dedicated, device-specific evaluation board is likely to be a better choice.

Dedicated Op Amp Evaluation Boards

In high speed/high precision ICs, special attention must be given to power supply decoupling. For example, fast slewing signals into relatively low impedance loads produce high speed transient currents at the power supply pins of an op amp. The transient currents produce corresponding voltages across any parasitic impedance that may exist in the power supply traces. These voltages, in turn, may couple to the amplifier output, because of the op amp's finite power supply rejection at high frequencies.

The AD8001 high speed current-feedback amplifier is a case in point, and a dedicated evaluation board is available for it. A bottom side view of this SOIC board is shown in Figure 7-142. A triple decoupling scheme was chosen, to ensure a low impedance ground path at all transient frequencies. Highest frequency transients are shunted to ground by dual 1000 pF/0.01 μF ceramic chip capacitors, located as close to the power supply pins as possible to minimize series inductance and resistance. With these surface-mount components, there is minimum stray inductance and resistance in the ground plane path. Lower frequency transient currents are shunted by the larger 10 μF tantalum capacitors.

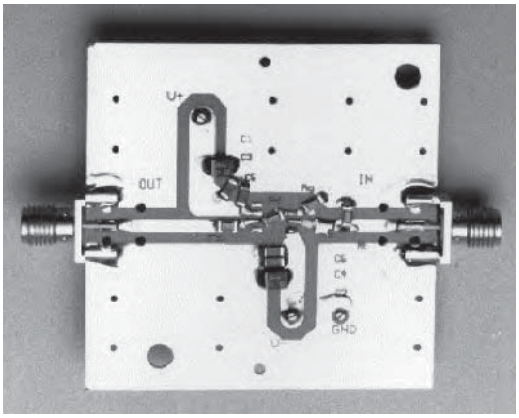


Figure 7-142: A high speed op amp such as the AD8001 requires a dedicated evaluation board with suitable ground planes and decoupling (bottom view)

The input and output signal traces of this board are 50 Ω microstrip transmission lines, as can be noted towards the right and left. Gain-set resistors are chip-style film resistors, which have low parasitic inductance. These can be seen in the center of the photo, mounted at a slight diagonal.

Note also that there is considerable continuous ground plane area on both sides of the PCB. Plated-through holes connect the top and bottom side ground planes at several points, in order to maintain lowest possible impedance and best high frequency ground continuity.

Input and output connections to the card are provided via the SMA connectors as shown, which terminate the input/output signal transmission lines. The board's power connection from external lab supplies is made via solder terminals, which are seen at the ends of the broad supply line traces.

Some of these points are more easily seen in a topside view of the same card, which is shown in Figure 7-143. This AD8001 evaluation board is a noninverting signal gain stage, optimized for lowest parasitic capacitance. The cutaway area around the SOIC outline of the AD8001 provides lowest stray capacitance, as can be noted in this view.

In this view is also seen the virtually continuous ground plane and the multiple vias, connecting the top/bottom planes.

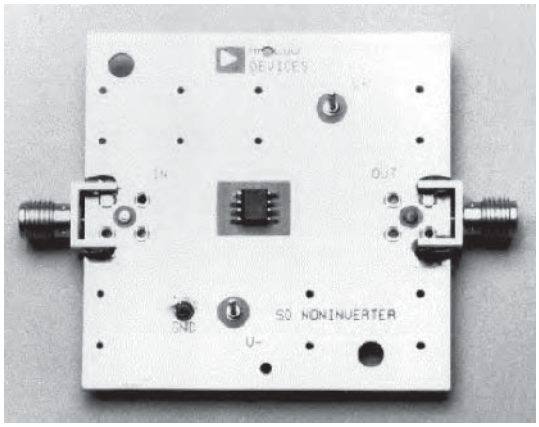


Figure 7-143: The AD8001 evaluation board uses a large area ground plane as well as minimal parasitic capacitance (top view)

Summary

In summary, good analog designers utilize as many tools as possible to ensure that the final system design performs correctly. The first step is the intelligent use of IC op amp and other macromodels, where available, to simulate the circuit. The second step is the construction of a prototype board to further verify the design, and to validate the simulation. The final PCB layout should then be based on the prototype layout as much as possible, with careful attention to parasitic effects.

References: Simulation, Breadboarding and Prototyping

1. L. W. Nagel, "SPICE2: A Computer Program to Simulate Semiconductor Circuits," May 1975, UCB/ERL M75/520, Univ. of California, Berkeley, CA, 94720.
2. A.Vladimirescu, K.Zhang, A.R.Newton, D.O.Pederson, "SPICE Version 2G User's Guide," August 1981, Department of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, CA, 94720.
3. Mark Alexander, Derek Bowers, "SPICE-Compatible Op Amp Macromodels," **EDN**, February 15, 1990 and March 1, 1990 (available as Analog Devices, Inc. AN138).
4. Joe Buxton, "Analog Circuit Simulation," Chapter 13 of **Amplifier Applications Guide**, 1992, Analog Devices, Inc., Norwood, MA, ISBN 0-916550-10-9.
5. Andrei Vladimerescu, **The SPICE Book**, John Wiley & Sons, New York, 1994, ISBN 0-471-60926-9.
6. "Development of an Extensive SPICE Macromodel for "Current-Feedback Amplifiers," National Semiconductor AN-840, July 1992.
7. David Hindi, "A SPICE-Compatible Macromodel for CMOS Operational Amplifiers," National Semiconductor AN-856, September 1992.
8. Boyle, et al, "Macromodelling of Integrated Circuit Operational Amplifiers," **IEEE Journal of Solid-State Circuits**, Vol. SC-9, no.6, December 1974.
9. Derek Bowers, Mark Alexander, Joe Buxton, "A Comprehensive Simulation Macromodel for 'Current Feedback' Operational Amplifiers," **IEE Proceedings**, Vol. 137, Pt. G, # 2, April 1990.
10. Joe Buxton, "OP27 Op Amp Macromodel, Rev B," Analog Devices, Inc., SPICE model library, December 1990, www.analog.com.
11. Antonio Germano, "AD817 Op Amp Macromodel, Rev A," Analog Devices, Inc., SPICE model library, November 1992, www.analog.com.
12. Antonio Germano, "OP295 Op Amp Macromodel, Rev B," Analog Devices, Inc., SPICE model library, February 1995, www.analog.com.
13. Antonio Germano, "OP284 Op Amp Macromodel, Rev B," Analog Devices, Inc., SPICE model library, November 1995, www.analog.com.
14. Steve Reine, "AD8031A Op Amp Macromodel, Rev C," Analog Devices, Inc., SPICE model library, August 1996, www.analog.com.
15. Steve Reine, "AD823AN Op Amp Macromodel, Rev C," Analog Devices, Inc., SPICE model library, April 1997, www.analog.com.
16. John Hayes, "AD8051 Op Amp Macromodel, Rev 0," Analog Devices, Inc., SPICE model library, September 1998, www.analog.com.
17. Troy Murphy, "AD8552 Op Amp Macromodel, Rev 1.0," Analog Devices, Inc., SPICE model library, July, 1999, www.analog.com.
18. John Hayes, Tim Watkins, "AD623 In Amp Macromodel, Rev B," Analog Devices, Inc., SPICE model library, September 2000, www.analog.com.
19. PSpice Simulation software, 1-888-671-9500, www.pspice.com.
20. Jim Williams, "High Speed Amplifier Techniques," Linear Technology AN-47, August, 1991.

21. Robert A. Pease, **Troubleshooting Analog Circuits**, Butterworth-Heinemann, 1991, ISBN 0-7506-9184-0.
22. Vector Electronic Company, 12460 Gladstone Ave., Sylmar, CA 91342, Tel. 818-365-9661.
23. Wainwright Instruments Inc., 69 Madison Ave., Telford, PA, 18969-1829, 215-723-4333.
24. Wainwright Instruments GmbH, Widdersberger Strasse 14, DW-8138 Andechs-Frieding, Germany. +49-8152-3162.
25. PADS Software, Advanced CAM Technologies, Inc., 16450 Los Gatos Blvd., Suite 110, Los Gatos, CA 95032, www.ecam.com/.
26. ACCEL Technologies, Inc., 17140 Bernardo Center Drive, Suite 100, San Diego, CA 92128, www.acceltech.com/.
27. LPKF Laser & Electronics, 28220 SW Boberg Rd., Wilsonville, OR 97020, 800-345-LPKF or 503-454-4200, www.lpkfcadcam.com.
28. T-Tech, Inc., 5591-B New Peachtree Road, Atlanta, GA, 34341, 800-370-1530 or 770-455-0676, www.T-Tech.com.
29. Adolfo Garcia, "Evaluation Boards for Single, Dual and Quad Operational Amplifiers," **Analog Devices AN398**, January 1996.

This page intentionally left blank

CHAPTER 8

Op Amp History

This page intentionally left blank

CHAPTER 8

Op Amp History

Walt Jung

The theme of this chapter is to provide the reader with a more comprehensive *historical background of the operational amplifier* (op amp for short—see below). This story begins back in the vacuum tube era and continues until today (2004). While most of today's op amp users are probably somewhat familiar with integrated circuit (IC) op amp history, considerably fewer are familiar with the non-IC solid-state op amp. Even more likely, very few are familiar with the origins of the op amp in vacuum tube form, even if they are old enough to have used some of those devices in the '50s or '60s. This introduction addresses these issues with a narrative of not only how op amps originated and evolved, but also what key factors gave rise to the op amp's origin in the first place.[1]

A developmental background of the op amp begins early in the twentieth century, starting with certain fundamental beginnings. Of these, there were two key inventions very early in the century. The first was not an amplifier, but a two-element vacuum-tube-based rectifier, the "Fleming diode," by J. A. Fleming, patented in 1904 (see Reference 1). This was an evolutionary step beyond Edison's filament-based lamp, by virtue of the addition of a *plate* electrode, which (when positively biased) captured electrons emitted from the filament (*cathode*). Since this device passed current in one direction only, it performed a rectification function. This patent was the culmination of Fleming's earlier work in the late years of the nineteenth century.

A second development (and one more germane to amplification) was the invention of the three-element triode vacuum tube by Lee De Forest, the "Audion," in 1906. This was the first active device capable of signal amplification (see Reference 2). De Forest added a control grid electrode, between the diode filament and plate, and an amplifier device was born. While these first tubes of the twentieth century had their drawbacks, the world of modern electronics was being born, and more key developments were soon to follow.

For op amps, the invention of the feedback amplifier principle at Bell Telephone Laboratories (Bell Labs) during the late 1920s and early '30s was truly an enabling development. This landmark invention led directly to the first phase of vacuum tube op amps, a general-purpose form of feedback amplifier using vacuum tubes, beginning in the very early 1940s and continuing through the World War II years.

After World War II there was a transition period as vacuum tube op amps were improved and refined, at least in circuit terms. But these amplifiers were fundamentally large, bulky, power-hungry devices. So, after a decade or more, vacuum tube op amps began to be replaced by miniaturized solid-state op amps in the 1950s and 1960s.

A final major transitional phase of op amp history began with the development of the first IC op amp, in the mid 1960s. Once IC technology became widely established, things moved quickly through the latter of the twentieth century years, with milestone after milestone of progress being made in device performance.

---

[1] Note—this chapter of the book is not necessarily required for the use of op amps, and can be optionally skipped. Nevertheless, it should offer interesting background reading, as it provides a greater appreciation of current devices once their beginnings are more fully understood.

A Definition for the Fledgling Op Amp

Although it may seem inappropriate at this point in the book to define what an op amp was in those early days, it is necessary to do so, albeit briefly, because what is commonly known today as an op amp is different in some regards from the very first op amps. The introductory section of Chapter 1, where the discussion is more closely oriented around today's op amp definition, supplements the meaning below.

The very first op amps were not even called such, nor were they even called "operational amplifiers." The naming of the device came after the war years, in 1947.

For this historical discussion, it may be more clear to call one of these first op amps a *general-purpose, dc-coupled, high gain, inverting feedback amplifier*. This of course is a loose definition, but it nevertheless fits what transpired.

- *General-purpose* may be interpreted to mean that such an amplifier (or multiple amplifiers) operates on bipolar power supplies, with input and output signal ranges centered around 0V (ground).
- *Dc-coupled* response implies that the signals handled include steady-state or dc potentials, as well as ac signals.
- *High gain implies* a magnitude of dc gain in excess of 1000 × (60 dB) or more, as may be sufficient to make system errors low when driving a rated load impedance.
- *Inverting mode operation* means that this feedback amplifier had, in effect, one signal input node, with the signal return being understood as ground or common. Multiple signals were summed at this input through resistors, along with the feedback signal, via another resistor. *Note that this single-ended operating mode is a major distinction from today's differential input op amps*. Operation of these first feedback amplifiers in only a single-ended mode was, in fact, destined to continue for many years before differential input operation became more widespread.
- *A feedback amplifier* of this type could be used in a variety of ways, dependent upon the nature of the feedback element used with it. This capability of satisfying a variety of applications was later to give rise to the name.

So, given this background, op amp history can now be explored.

SECTION 8-1

Introduction

Setting the Stage for the Op Amp

Op amps are high gain amplifiers, and are used almost invariably with overall loop feedback. The principle of the feedback amplifier has to rank as one of the more notable developments of the twentieth century—right up there with the automobile or airplane for breadth of utility and general value to engineering. Most importantly, such feedback systems, although originally conceived as a solution to a communications problem, operate today in more diverse situations. This is a clear tribute to the concept's fundamental value.

Today the application of negative feedback is so common that it is often taken for granted. But this wasn't always the case. Working as a young Western Electric Company engineer on telephone channel amplifiers, Harold S. Black first developed feedback amplifier principles. Note that this was far from a brief inspirational effort, or narrow in scope. In fact, it took some nine years after the broadly written 1928 patent application, until the 1937 issuance (see Reference 3). Additionally, Black outlined the concepts in a **Bell System Technical Journal** article, and, much later, in a 50th anniversary piece where he described the overall timeline of these efforts (see References 4 and 5).

Like circumstances surrounding other key inventions, there were others working on negative feedback amplifier applications. One example would be Paul Voigt's mid-1920s work (see References 6 and 7).[1] The prolific British inventor Alan Blumlein did 1930s feedback amplifier work, using it to control amplifier output impedance (see Reference 8).[2] Finally, a research group at N. V. Philips in the Netherlands is said to have been exploring feedback amplifiers within roughly the same time frame as Black (late 20s to early 30s). In 1937 B. D. H. Tellegen published a paper on feedback amplifiers, with attributions to K. Posthumus and Black (see References 9 and 10).[3] In Tellegen's paper are the same equations as those within Black's (substituting A for Black's μ).

It isn't the purpose here to challenge Black's work, rather to note that sometimes overlapping but independent parallel developments occur, even for major inventions. Other examples of this will be seen shortly, in the development of differential amplifier techniques. In the long run, a broad-based, widely accepted body of work tends to be seen as the more significant effort. In the case of Black's feedback amplifier, there is no doubt that it is a most significant effort. It is also both broad-based and widely accepted.

There are also many earlier *positive* feedback uses; a summary is found in Reference 11.

---

[1] Some suggest Paul Voigt as the true feedback amplifier inventor, not Black (see Ref. 6, 7). Examination of Voigt's UK patent 231,972 fails to show a feedback amplifier theory comparable to Black's detailed exposition of Ref. 3 and 4. In fact, there are no equations presented to describe Voigt's system behavior.

[2] Blumlein's UK patent 425,553 is focused on controlling amplifier output impedance through voltage and/or current feedback, not addressing in detail the broader ramifications of feedback.

[3] Examination of UK patent 323,823 fails to find reference to K. Posthumus, apparently a practice with N. V. Philips UK patents of that period. The patent does show a rudimentary feedback amplifier, but unfortunately the overall clarity is marred by various revisions and corrections, to both text and figures.

Black's Feedback Amplifier

The basis of Black's feedback amplifier lies in the application of a portion of the output back to the input, so as to reduce the overall gain. When properly applied, this provides the resultant amplifier with characteristics of enhanced gain stability, greater bandwidth, lower distortion, and usefully modified stage input and output impedance(s).

A block diagram of Black's basic feedback amplifier system is shown in Figure 8-1 below. Note that Black's "μ" for a forward gain symbol is today typically replaced by "A." As so used, the feedback network β defines the overall transfer expression of the amplifier. Thus a few passive components, typically just resistors or sometimes reactive networks, set the gain and frequency response characteristics of this system.

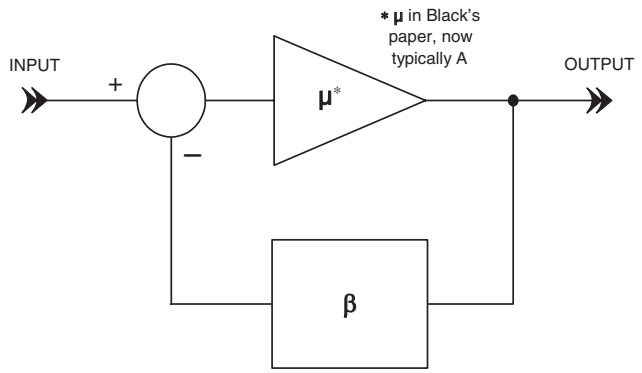


Figure 8-1: A block diagram of Black's feedback amplifier, comprised of a forward gain "μ" and a feedback path of "β"

At the time Black's work was initiated, the problem he faced was how to make practical a series signal connection of hundreds (if not thousands) of telephone system repeater amplifiers using directly heated triode tubes. The magnitude of this problem becomes obvious when it is considered that each amplifier alone couldn't be held more stable to less than 1 dB of gain variation, and even under the best of conditions, the stage distortion was unacceptable.

Black's feedback amplifier invention led not just to better repeater amplifiers for Western Electric, but to countless millions of other widely varying applications. Almost every op amp application ever conceived uses feedback. So, given the fact that modern op amp types number in the dozens (in individual models, many thousands), it isn't hard to appreciate the importance feedback principles take on for today's designs.

A significant reason that Black's feedback concept took root and prospered wasn't simply because it was a useful and sound idea. That it was, but it was also *different*, and many experienced engineers fought the idea of "throwing away gain." However, Black did have help in selling the radically new concept, help that was available to few other inventors. By this help what is meant is that he had the full backing of the

Bell Telephone System, and all that this implied towards forging and promoting a new technical concept. An interesting narrative of the feedback amplifier's development and the interplay of Black and his coworkers can be found in David Mindell's paper, "Opening Black's Box: Rethinking Feedback's Myth of Origin" (see Reference 11).

The 1930s and 1940s at Bell Labs could very well be regarded as golden years. They produced not just Black's feedback amplifier, but also other key technical developments that expanded and supported the

amplifier. This support came from some of the period's finest engineers—not just the finest Bell Labs engineers, but the world's finest.

To quote Black's own words on the Bell Labs support activity related to his landmark invention, *"Within a few years, Harry Nyquist would publish his generalized rule for avoiding instability in a feedback amplifier, and Hendrick W. Bode would spearhead the development of systematic techniques of design whereby one could get the most out of a specified situation and still satisfy Nyquist's criterion."* (see Reference 5).

The feedback amplifier papers and patents of Harry Nyquist and Hendrick Bode (see References 13 and 14), taken along with the body of Black's original work, form solid foundations for modern feedback amplifier design. Bode later published a classic feedback amplifier textbook (see Reference 15). Later on, he also gave a talk summarizing his views on the feedback amplifier's development (see Reference 15).

In addition to his famous stability criteria, Nyquist also supplied circuit-level hardware concepts, such as a patent on direct-coupled amplifier interstage coupling (see Reference 17). This idea was later to become a standard coupling method for vacuum tube op amps.

Outside Bell Labs, other engineers were also working on feedback amplifier applications of their own, affirming the concept in diverse practical applications. Frederick Terman was among the first to publicize the concept for ac feedback amplifiers, in a 1938 article (see Reference 18).

For single-ended signal path dc amplifiers, there were numerous landmark papers during the World War II period. Stewart Miller's 1941 article offered techniques for high and stable gain with response to dc (see Reference 19). This article introduced what later became a standard gain stabilization concept, called "cathode compensation," where a second dual triode section is used for desensitization of heater voltage variations. Ginzton's 1944 amplifier article employed Miller's cathode compensation, as well as Nyquist's level-shifting method (see Reference 20). The level shifter is attributed to Brubaker (who apparently duplicated Nyquist's earlier work). Artzt's 1945 article surveys various dc amplifier techniques, with emphasis on stability (see Reference 20).

After World War II, the MIT Radiation Laboratory textbook series documented many valuable electronic techniques, including a volume dedicated to vacuum tube amplifiers. The classic Valley-Wallman volume number 18 is not only generally devoted to amplifiers, it includes a chapter on dc amplifiers (see Reference 22). While this book doesn't discuss op amps by name, it does include dc feedback circuitry examples. Op amps did exist, and had even been named as of 1947, just prior to the book's publication.

References: Introduction

(Note: Appended annotations indicate relevance to op amp history.)

Early Vacuum Tube and Feedback Amplifier Developments

1. J. A. Fleming, "Instrument for Converting Alternating Electric Currents into Continuous Currents," **US Patent 803,684**, filed April 19, 1905, issued Nov. 7, 1905. See also UK Patent 24,850, filed Nov. 16, 1904. *(The 'Fleming diode' or the first vacuum tube rectifier.)*
2. Lee de Forest, "Device for Amplifying Feeble Electrical Currents," **US Patent 841,387**, filed October 25, 1906, issued January 15, 1907. *(The triode vacuum tube, or 'Audion,' the first amplifying device.)*
3. H. S. Black, "Wave Translation System," **US Patent 2,102,671**, filed August 8, 1928, issued December 21, 1937. *(The basis of feedback amplifier systems.)*
4. H. S. Black, "Stabilized Feedback Amplifiers," **Bell System Technical Journal**, Vol. 13, No. 1, January 1934, pp. 1–18. *(A practical summary of feedback amplifier systems.)*
5. Harold S. Black, "Inventing the Negative Feedback Amplifier," **IEEE Spectrum**, December, 1977. *(Inventor's 50th anniversary story on the invention of the feedback amplifier.)*
6. Geoffrey Horn, "Voigt, not Black," **Stereophile**, Letters, April 1998, pp. 18, 21.
7. Paul G. A. H. Voigt, "Improvements in or Relating to Thermionic Amplifying Circuits for Telephony," **UK Patent 231,972**, filed January 29, 1924, issued April 16, 1925. *(A motional feedback loudspeaker/amplifier system.)*
8. A. D. Blumlein, "Improvements in and relating to Thermionic Valve Amplifiers," **UK Patent 425,553**, filed Sept. 8, 1933, issued March 18, 1935. *(Use of feedback to control amplifier output impedance.)*
9. B. D. H. Tellegen, "Inverse Feedback," **Philips Technical Review**, Vol. 2, No. 10, October, 1937. *(Another feedback amplifier development, generally paralleling Black's.)*
10. "Improvements in or Relating to Arrangements for Amplifying Electrical Oscillations," **UK Patent 323,823**, filed October 18, 1928, issued January 16, 1930 (original filing), filed July 18, 1929, final approval January 1938 and February 1939 (amended filing). *(A simple one stage feedback amplifier system.)*
11. D. G. Tucker, "The History of Positive Feedback," **Radio and Electronic Engineer**, Vol. 42, No. 2, February 1972, pp. 69–80.
12. David A. Mindell, "Opening Black's Box: Rethinking Feedback's Myth of Origin," **Technology and Culture**, Vol. 41, July, 2000, pp. 405–434. *(A perspective discussion of the inter-related events and cultures surrounding the feedback amplifier's invention.)*
13. Harry Nyquist, "Regeneration Theory," **Bell System Technical Journal**, Vol. 11, No. 3, July, 1932, pp. 126–147. See also: "Regenerative Amplifier," **US Patent 1,915,440**, filed May 1, 1930, issued June 27, 1933 *(The prediction of feedback amplifier stability by means of circular gain-phase plots.)*
14. Hendrick Bode, "Relations Between Attenuation and Phase In Feedback Amplifier Design," **Bell System Technical Journal**, Vol. 19, No. 3, July, 1940. See also: "Amplifier," **US Patent 2,123,178**, filed June 22, 1937, issued July 12, 1938. *(The prediction of feedback amplifier stability by means of semi-log gain-phase plots.)*
15. Hendrick Bode, **Network Analysis and Feedback Amplifier Design**, Van Nostrand, 1945. *(Bode's classic text on network analysis, as it relates to the design of feedback amplifiers.)*

16. Hendrick Bode, "Feedback—the History of an Idea," **Proceedings of the Symposium on Active Networks and Feedback Systems**, Polytechnic Press, 1960. Reprinted within **Selected Papers on Mathematical Trends in Control Theory**, Dover Books, 1964. *(A perspective historical summary of the author's thoughts on the development of the feedback amplifier.)*
17. Harry Nyquist, "Distortionless Amplifying System," **US Patent 1,751,527**, filed November 24, 1926, issued March 25, 1930. *(A means of direct-coupling multiple amplifier stages via resistance networks for interstage coupling.)*
18. F. E. Terman, "Feedback Amplifier Design," **Electronics**, January 1937, pp. 12–15, 50. *(Some practical ac-coupled topologies for implementing feedback amplifiers.)*
19. Stewart E. Miller, "Sensitive DC Amplifier with AC Operation," **Electronics**, November, 1941, pp. 27–31, 106–109. *(Design example of a stable, high-gain direct-coupled amplifier including 'cathode-compensation' against variations in filament voltage, use of glow tube inter-stage coupling, and a stable line-operated DC supply.)*
20. Edward L. Ginzton, "DC Amplifier Design Techniques," **Electronics**, March 1944, pp. 98–102. *(Various design means for improving direct-coupled amplifiers.)*
21. Maurice Artzt, "Survey of DC Amplifiers," **Electronics**, August, 1945, pp. 112–118. *(Survey of direct-coupled amplifier designs, both single-ended and differential, with emphasis on high stability.)*
22. George E. Valley, Jr., Henry Wallman, **Vacuum Tube Amplifiers**, MIT Radiation Labs Series No. 18, McGraw-Hill, 1948. *(A classic WWII Radiation Lab development team textbook. Chapter 11, by John W. Gray, deals with direct-coupled amplifiers.)*

This page intentionally left blank

SECTION 8-2

Vacuum Tube Op Amps

Development of Differential Amplifier Techniques

While amplifiers using both feedback and nonfeedback topologies were being refined in the late 1930s and throughout the 1940s, there were some very interesting developments within the realm of differential amplifiers.

Today's op amps utilize differential topologies to a high degree, but the reader should understand that this wasn't universally so back in the days of vacuum tube amplifiers. In fact, vacuum tube op amp topologies that fully utilized differential techniques never really became well established before the breed began dying off. Nevertheless, it is still a useful thing to examine some key differential amplifier publications up through about 1950, at which point it represented a maturing of the art. The fully differential, defined gain precision dc amplifier was, of course, the forerunner of what we know today as the *instrumentation amplifier* (see Chapter 2 of this book).

The earliest vacuum tube differential amplifiers were reported well back in the 1930s, and evolved steadily over the next 15–20 years. Many of these authors addressed the problems of low level instrumentation amplifier circuitry used in obtaining signals from living tissue, thus the apparatus involved was often called a "biological amplifier."

One of the early authors in this field was B. H. C. Matthews, writing on a special differential input amplifier in 1934 (see Reference 1). Matthews' amplifier did indeed have differential inputs, but since the common cathodes were tied directly to the power supply common, it wasn't optimized towards minimizing response to common-mode (CM) inputs. Note that in those days CM signals were often referred to as *push-push* signals, to denote signals in-phase at both inputs.

Alan Blumlein's UK patent 482,470 of 1936 went a step further in this regard, by biasing the common-cathodes of a differential pair through a common resistance to ground (see dual triodes within Figure 2 of Reference 2). Blumlein's patent was concerned with wideband signals, not biological ones, using ac-coupling. Nevertheless, it was a distinct improvement over the Matthews amplifier, since it provided bias conditions more amenable to CM signal rejection.

In 1937 Franklin Offner discussed a variety of differential amplifiers, and among them is found one similar to Blumlein's configuration (see Figure 3 of Reference 3). Like those of Blumlein, Offner's circuits also used ac-coupling. A useful technique that appears in this paper is the use of *common-mode feedback* to increase CM rejection (Figure 4 of Reference 3). To enable this, a CM sample from a downstream stage is feedback to an earlier stage. This feedback decreases the CM gain, and thus improves CM rejection.

Otto Schmitt discussed a common cathode, cathodes-to-common dual pentode circuit in 1937 (see Reference 4). This circuit, while novel in the operation of the pentode screens, didn't minimize response to CM input signals (similar to the Matthews circuit, above).

In 1938 J. F. Toennies discussed what might be the first form of what has subsequently come to be known as the *long-tailed pair* (see Reference 5). In this form of differential input amplifier, the push-pull input signals are applied to the dual grids of the stage, and the common cathodes are returned to a high negative

voltage, through a high value common resistance. Toennies' fundamental circuit (Figure 1 of Reference 5) used dual triodes with a plate supply of 135 V, and a cathode bias supply of –90 V.

The action of the large value cathode resistance biased to a high negative voltage acts to optimize the differential coupling of the stage, while at the same time minimizing the CM response, as noted in Figure 8-2 below. This may intuitively be appreciated by considering the effect of the large cathode resistance to a high negative voltage $-V_S$, as in B, versus the simple cathode-coupled pair as in A. In A, the cathode resistance R_K is returned to ground, the same point common to the grids (the return for the $+V_S$ supply).

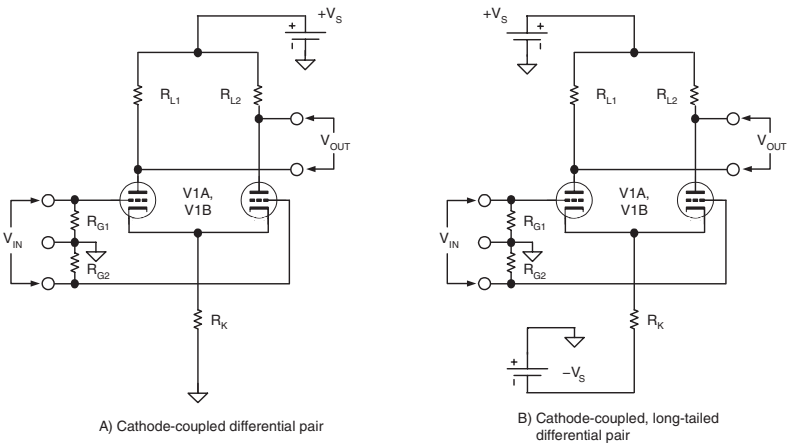


Figure 8-2: A comparison of simple differential pair biasing in A (left) and long-tailed biasing as in B (right)

The constant current action of the long-tailed biasing shown in 8-2B tends to minimize response to CM inputs (while not impairing differential response). Later on, some more advanced designs were even to go as far as using a pentode tube for the "long tail" common-cathode bias, capitalizing on a pentode's high incremental resistance.

In 1938 Otto Schmitt also discussed a long-tailed pair form of amplifier (see Reference 6). The context of his discussion was not so much aimed towards optimizing CM rejection, but rather using such a stage as a phase inverter. With one input grid of such a stage grounded, and the opposite grid driven in single-ended fashion, out-of-phase signals result with equal plate load resistors. Schmitt was a prolific inventor, and was to return later on (below).

Lionel Jofeh, within UK patent 529,044 in 1939, offered a complete catalog of eight forms of cathode-coupled amplifiers (see Reference 7).

Harold Goldberg presented a complete multistage, direct-coupled differential amplifier in 1940 (see Reference 8). Using power pentodes within a unique low voltage differential input stage, Goldberg reported an equivalent input noise of 2 μV for the circuit. This work parallels some of the earlier work mentioned above, apparently developed independently.

In 1941, Otto Schmitt published another work on the differential amplifier topic, going into some detail of analysis (see Reference 9). In this work he clearly outlines the advantages of the long-tailed pair, in terms of the stage's phase-inversion properties. He also covers the case of a degenerated long-tailed pair, where a

common cathode-cathode resistance is used for gain adjustment, and the individual cathodes are biased to a negative voltage with resistors of values twice that of a single cathode-coupled stage.

Walther Richter wrote on cathode follower and differential circuits in 1943 (see Reference 10). While primarily focused on single-ended cathode followers, this article also does an analysis of the long-tailed pair.

Harold Goldberg wrote again on his multistage differential amplifier, in 1944 (see Reference 11). The 1944 version still used batteries for most of the power, but did add a pentode to supply the bias current of the first stage long-tailed pair.

Writing in 1944, G. Robert Mezger offered a differential amplifier design with a new method of interstage level-shift coupling (see Reference 12). Previous designs had used either a resistive level-shift like Nyquist, or the more recent glow-tube technique of Miller. Mezger's design used a 12J5 triode as the bottom level-shift element, which acts as constant current source. Working against a fixed resistance at the top, this allows a wideband level shift. Good overall stability was reported in a design that used both differential and CM feedback. Regulation was used for plate and critical heater circuits.

Franklin Offner wrote a letter to the editor in 1945, expressing dissatisfaction with other differential amplifier authors (see Reference 13). In this work he comments on the work of Toennies (Reference 5, again), "…merely an application of in-phase degeneration by the use of a large cathode resistor,…" Offner also overlooked Blumlein's patent.

D. H. Parnum published a two-part survey of differential amplifier techniques in 1945 (see Reference 14). This work analyzed some previously published designs, and presented two differential-throughout amplifier examples, both dc- and ac-coupled.

In a comprehensive study of differential amplifier designs from 1947, Denis L. Johnston presented a three-part article on design techniques, with a finished design example (see Reference 15). This article is notable not only for the wealth of detailed information, but it also contains a bibliography of 61 references to related works.

The input stage of Johnston's design example amplifier used an input long-tailed pair based on the 6CS7 dual triode, with the cathode current supplied by a 6J7G pentode (see Figure 10a of Reference 15). The second stage was also a long-tailed pair, directly coupled to the first stage, with CM feedback. Multiple stages of supply regulation are used.

D. H. Parnum also published another work on differential amplifiers, in 1950 (see Reference 16). In this paper he presented a critique of the input stage design of the Johnston design (Reference 15), pointing out necessary conditions for optimizing CM rejection for multiple stage amplifiers.

The P. O. Bishop and E. J. Harris design paper of 1950 is similar in overall scope to the Johnston work noted above (see Reference 17). It reviews the work of many other designers in the biological area, and presents a sophisticated example design. In this circuit (Figure 3 of Reference 17) a 954 pentode pair is used for input cathode followers, driving a 6J6 dual triode long-tailed pair. Both the input stages as well as the next two stages used 12SH7 pentodes for the tail current sources. Highly stabilized power supplies are used for the plate supplies, with critical heaters also stabilized.

In 1950 Richard McFee published some modifications useful to improve the CM rejection of a single dual triode stage (see Reference 18).

One of the better overview papers for this body of work appeared in 1950, authored by Harry Grundfest (see Reference 19). This paper also gives greater insight into how the biological amplifiers were being used at this time, and offers many references to other differential amplifier work.

It is notable that Grundfest credits Offner (Reference 3, again) with the invention of the long-tailed pair. However, it can be argued that it isn't apparent from Offner's schematics that a true long-tailed pair is actually being used (there being no negative supply for the cathode resistance). The type of biasing that Offner (and Blumlein) use is a simple resistor from the common cathodes to circuit common, which would typically have just a few volts of bias across it, and, more importantly, would have a value roughly comparable in magnitude to the cathode impedance.

Unfortunately, Grundfest also overlooks Blumlein (Reference 2), who preceded Offner with a similar circuit. This similarity is apparent if one compares Blumlein's Figure 2 against Offner's Figure 3, in terms of how the biasing is established.

One of the deepest technical discussions on the topic of DC differential amplifiers can be found in C. M.Verhagen's paper of 1953 (see Reference 20). Verhagen goes into the electron physics of the vacuum tube itself, as well as the detailed circuitry around it, as to how they both effect stability of operation. This paper includes detailed mathematical expressions and critiques of prior work. Many other topical papers are referenced, including some of those above.

The above discussion is meant as a prefacing overview of dc differential amplifiers, as this technology may impact op amp designs. It isn't totally comprehensive, so there are likely other useful papers on the topic. Nevertheless, this discussion should serve to orient readers on many of the general design practices for stable dc differential amplifiers.

Op Amp and Analog Computing Developments

Some of the differential amplifier work described above did find its way into op amps. But, there was also much other significant amplifier work being done, at Bell Labs and elsewhere in the US, as well around the world. The narrative of op amp development now focuses on the thread of *analog computing*, which was the first op amp application.

In the late 1930s George A. Philbrick, at Foxboro Corporation, was developing analog process control simulation circuits with vacuum tubes and passive parts. Philbrick developed many interesting circuits, and some were op amp forebears (see Reference 21).

In fact, within this article, he describes a single tube circuit that performs some op amp functions (Figure 3A). This directly coupled circuit develops an operating relationship between input and output voltages, producing a voltage output proportional to the ratio of two impedances. While this circuit (using floating batteries for power) can't be termed a general-purpose op amp circuit, it nevertheless demonstrates some of the working principles. In Reference 22, Per Holst further describes this early Philbrick work. Within a decade Philbrick was to start his own company supplying vacuum tube op amps and other components used within analog simulation schemes (see below).

The very first vacuum tube amplifiers fitting the introductory section op amp definition came about early in the 1940s wartime period. The overall context was the use of this amplifier as a building block within the Bell Labs-designed M9 gun director system used by WWII Allied Forces. These op amp circuits were general-purpose, using bipolar supply voltages for power, handling bipolar input/output signals with respect to a common voltage (ground). As true to the definition, the overall transfer function was defined by the externally connected input and feedback impedances (more on this follows).

These early amplifiers were part of a specialized analog computer system that was designed to calculate proper gun aiming for fire upon enemy targets. The work on this project started in 1940, and was pioneered by Clarence A. Lovell, David Parkinson, and many other engineers of the Bell Labs staff. Their efforts have been chronicled in great detail by Higgins, et al, as well by James S. Small (see References 23 and 24).

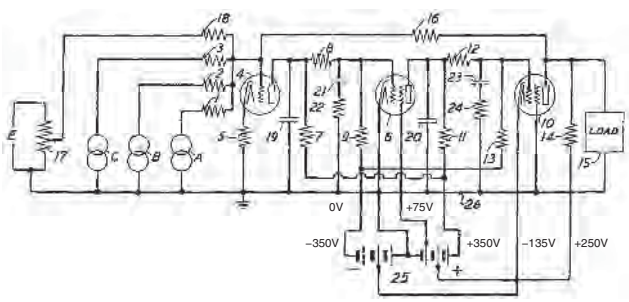
This Bell Labs design project resulted in a prototype gun director system that was called the T10, first tested in December of 1941. While the T10 was the first sample gun director, in later production the gun director was known as the Western Electric M9 (see Reference 25). Further documentation of this work is found in US Patents 2,404,081 and 2,404,387 (see References 26 and 27), plus a related paper by Lovell (see Reference 28). The patents illustrate many common feedback amplifier examples in varied tasks.

However, in terms of an overall technical view of the M9, perhaps the most definitive discussion can be found within "Artillery Director," US Patent 2,493,183, by William Boghosian, Sidney Darlington, and Henry Och of Bell Labs (see Reference 29). This key document breaks down the design of the analog computation scheme into the numerous subsystems involved. Op amps can be found throughout the patent figures, performing functions of buffers, summers, differentiators, inverters, and so forth.

Karl Swartzel's Op Amp

In terms of op amp details, the Boghosian et al patent references another crucial patent document. Many other Bell Labs M9-related patents, underscoring its seminal nature, also referenced this latter work. The patent in question here is US Patent 2,401,779, "Summing Amplifier" by Karl D. Swartzel Jr. of Bell Labs (see Reference 30), and a design that could well be the genesis of op amps. Ironically, Swartzel's work was never given due publicity by Bell Labs.[1] Filed May 1, 1941, it languished within the system during the war, finally being issued in 1946. Of course, the same could be said about many wartime patents—in fact many other Bell Labs patents met similar fates.

A schematic diagram for Swartzel's op amp is shown in Figure 8-3, which includes a table of values taken from the patent text. Although the context of the patent is an application as a summing amplifier, it is also obvious that this is a general-purpose, high-gain amplifier, externally configured for a variety of tasks by the use of suitable feedback components—the crux of the matter regarding the op amp function.



A) Schematic diagram

R1, R2, R3, R13, R16	1megΩ
R5	1.5kΩ
R7	0.5megΩ
R8	0.75megΩ
R9	2megΩ
R11	0.25megΩ
R12	1.25megΩ
R14, R15 (load)	6kΩ
R18	3megΩ
R22, R24	100kΩ
C19	0.25μF
C20	100pF
C21	1000pF
C23	0.03μF
V4	6SC7
V6	6SJ7
V10	6Y6G

B) Component values

Figure 8-3: Schematic diagram and component values for "Summing Amplifier" (US Patent 2,401,779, assigned to Bell Telephone Laboratories, Inc.)

[1] Bell Labs documented virtually everything on the M9 in its **Bell Laboratories Record**, as can be noted by the section references. But no op amp schematics were included in this long string of articles.

In the schematic of this "summing amplifier" there can be noted a number of key points. Three directly coupled tubes provided a high overall gain, with a net sign inversion with respect to the grid of input tube 4. Positive and negative power supplies are provided by the tapped battery, 25. The amplifier output swing at the load 15 is bipolar with respect to the common terminal, 26. In this instance of use, resistor R16 applies the feedback, and three signals are being summed via input resistors R1, R2, R3, with the input common to terminal 26. The input via resistor R18 was used for offset control.

The amplifier gain quoted in the patent was 60,000 (95 dB), and as noted, the circuit could drive loads of 6 kΩ, which is quite an achievement. It operated from supplies of ±350 V, with intermediate voltages as noted. The inter-stage level shift networks are the form described by Nyquist, and there are several RC networks used for stabilization purposes.

Over time, changes changes were made to this basic design, which will be described later in this section. The Swartzel op amp was truly a seminal work, as it allowed the creation of a complete, highly sophisticated analog computer system critical to WWII defense. It also spawned numerous other amplifier designs derived from its basic topology.

The M9 From A Bell Labs View

Because of a general embargo on the publication of defense-related technical information during WWII, a great deal of work came to light quite some time after the original development. Many M9 project details on its various components fell into this category, which included op amp diagrams.

Nonetheless, Bell Labs did begin documenting some of the M9 work, even before the war ended. The **Bell Laboratories Record** of December 1943, published a tribute to Harold Black, for his work on the feedback amplifier (see Reference 31). In the same and subsequent issues, there were published two stories on a public demonstration of the M9 system, as well as its development (see Reference 32).

Several key developments in electrical components were also documented in the **Bell Laboratories Record,** on capacitors, resistor networks, resistors, and precision potentiometers (see References 33–36).

There was also fitting recognition of M9 designers Lovell, Parkinson and Kuhn within the **Bell Laboratories Record**, on the occasion of their Medal for Merit award in April of 1947 (see Reference 37). The importance of this work in the view of Bell labs is underscored by some of the distinguished names associated with the project. Contributors beyond those mentioned above also included Hendrick Bode, Claude Shannon, and other notables of the Bell Labs staff. Finally, there was a then-unrecognized importance: It established the utility of the (yet-to-be-named) op amp concept—op amps were born!

The M9 From A World View

Viewed historically, the work of Lovell, Parkinson and other Bell Labs designers assumes broad significance, since it was war-needs driven, and the outcome literally affected millions of lives. The work provided an analog control computer for a gun director system instrumental to the war effort, achieving high hit rates against incoming targets—up to 90% by some accounts. The work of the M9 system teamed with the SCR584 radar system was highly successful at its mission—indeed fortunate for world freedom.

Robert Buderi wrote a detailed narrative of WWII radar developments, and his book contains an interesting account of the M9's role (see Reference 38). A broad, single-source computing, control, and historical perspective is found in David Mindell's thesis, "**Datum for its Own Annihilation: "Feedback, Control and Computing, 1916–1945**, (see Reference 39). In Chapter 8, Mindell also has an account of the M9/SCR584 success.

Naming the Op Amp

Further wartime op amp development work was carried out in the labs of Columbia University of New York, and was documented in 1947 by the program's research head, Professor John Ragazzini (see Reference 40). This often-cited key paper is perhaps best known for coining the term *operational amplifier,* which, of course, we now shorten to the more simple *op amp*. Quoting from this paper on the naming:

> "*As an amplifier so connected can perform the mathematical operations of arithmetic and calculus on the voltages applied to its input, it is hereafter termed an 'operational amplifier'.*"

The Ragazzini paper outlines a variety of ways that op amps can be used, along with their defining mathematical relationships. This paper also references the Bell Labs work on what became the M9 gun director, specifically mentioning the op amp circuits used.

The work that gave rise to the above paper was a late WWII NDRC Division 7 contract with Columbia University.[1] At that time, Loebe Julie was a bright young research engineer in the Columbia University Labs. Julie did work on these early op amps, which were aimed at improvements to the M9 gun director system, stated contractually as "Fire Control Electronics."

Reportedly working against the wishes of Ragazzini, Julie was engaged to do this work at the behest of analog computer engineer George A. Philbrick, part of the Division 7 team (see References 41 and 42). Julie completed a two-tube op amp design, using a pair of 6SL7 dual triodes in a full differential-in/differential-out arrangement (see Reference 41, again). For whatever the reason, his lab boss Ragazzini gave Julie's amplifier work but a minor acknowledgment at the very end of the paper.

The op amp schematic shown in the Ragazzini paper (Figure 1 of Reference 40) doesn't match the schematic attributed to Julie (Reference 41). Ragazzini doesn't cite any specifications for this circuit, so the origins and intent aren't clear, unless it was intended as a modest performance example. It doesn't seem as if it could be an M9 system candidate, for a couple of reasons.

For example, briefly analyzing the Figure 1 Ragazzini op amp, it seems doubtful that this particular design was really intended to operate in the same environment as the original M9 op amp (Reference 30, or Figure 8-3). Swartzel's three-stage circuit used a triode and two pentodes, with one of the latter a power output stage. So, Ragazzini's circuit wouldn't appear to match the gain characteristics of Swartzel's design, as it used three cascaded triodes. It also wouldn't be capable of the same output drive, by virtue of its use of a 6SL7 output stage, loaded with 300 kΩ.

Evolution of the Vacuum Tube Op Amp

Nevertheless, Julie's op amp design was notable in some regards. It had a better input stage—due to the use of a long-tailed 6SL7 dual triode pair, with balanced loads. This feature would inherently improve drift over previous single-ended triodes or pentodes.

A truly key feature that Julie's circuit held over previous single-ended input designs was the basic fact that it offered *two signal inputs* (inverting and noninverting) as opposed to the single inverting input (Figure 8-3). The active use of both op amp inputs allows much greater signal interface freedom. In fact, this feature is today a hallmark of what can be called a functionally complete op amp—nearly 60 years later. The differential input stage not only improved the drift performance, but it made the op amp immeasurably

[1] Mindell (reference 39) lists in his Table 6-1, a contract No.76 for "Fire Control Electronics," with Ragazzini as investigator, running from November 15, 1943 to September 30, 1945, at a cost of $85,000. The Division 7 supervisor for this Columbia University project is listed as SHC, for Samuel H. Caldwell.

easier to apply. Ironically, however, some time passed before the application of op amps caught up with the availability of that second input.

Much other work was also done on the improvement of direct-coupled amplifiers during the war years and shortly afterwards. Stewart Miller, Edward Ginzton, and Maurice Artzt wrote papers on the improvement of direct-coupled amplifiers, addressing such concerns as input stage drift stabilization against heater voltage variations, interstage coupling and level-shifting schemes, and control of supply impedance interactions (see References 43–45). Some additional examples of improved dc amplifiers can be found in the Valley-Wallman book (see Reference 46).

Before the 1940s ended, companies were already beginning to capitalize on op amp and analog computing technology. Seymour Frost wrote about an analog computer developed at Reeves Instrument Corporation, called REAC (see Reference 47). This computer used as its nucleus an op amp circuit similar to the Swartzel M9 design. In the Reeves circuit the first stage was changed to a 6SL7 dual triode, used in a Miller-compensated low drift setup (Reference 43).

Chopper Stabilization of the Vacuum Tube Op Amp

Even with the use of balanced dual triode input stages, drift was still a continuing problem of early vacuum tube op amps. Many users sought means to hold the input-referred offset to a sub mV level, as opposed to the tens to hundreds of mV typically encountered. The drift had two components, warm-up related, and random or longer term, both of which necessitated frequent rezeroing of amplifiers. This problem was at least partially solved in 1949, with Edwin A. Goldberg's invention of the *chopper-stabilized* op amp (see Reference 48).

The chopper-stabilized op amp employs a second, high gain, ac-coupled amplifier. It is arranged as a side-path to the main amplifier. The chopper channel is arranged with the input signal path AC-coupled to the inverting input of the main DC-coupled amplifier, and a 60 Hz or 400 Hz switch periodically commutating to ground. The switching action chops the small dc input signal to ac, which is greatly amplified (1000 or more). The ac output of the chopper path is synchronously rectified, filtered, and applied to the main amplifier second input. In the resulting composite amplifier, main amplifier drift is reduced by a factor roughly equal to the chopper gain.

With chopper stabilization, op amps could have offset voltages stable to a few μV, and long term drift sufficiently low that manual zeroing wasn't required. Another key benefit was that the dc and low frequency gain was also boosted, by an amount equal to the additional gain factor provided by the chopper channel. By this means, the dc open-loop gain of a chopper amplifier could easily exceed 100,000 times (100 dB). Goldberg's amplifier of Ref. 48 for example, had a dc gain of 150,000,000, or 163 dB.

As a consequence of the above, the dc gain-related precision of a chopper amplifier is much higher than that of a conventional op amp, due to the additional open-loop gain. This basic point, combined with the "zero offset, zero drift" operating feature, made chopper-stabilized vacuum tube op amps a standard choice for precision analog work. This point is one that, generally speaking, is also essentially true even today, with IC chopper op amps readily available. *Note—although today's chopper amplifiers operate by a different method, the net effect is still big improvements in dc offset, drift, and gain.*

There were, however, some serious downsides to these early chopper amplifiers. The basic chopper architecture described above essentially "uses up" the noninverting second op amp input of a dual triode pair, to apply the dc offset correction signal. Thus all of the early chopper op amps operated in an *inverting-only* mode. In time, improved chopper architectures were developed to overcome this limitation, and the very high dc precision was made available for all modes of use.

A second limitation was the fact that the first chopping devices used were mechanical switches (vibrators). As such, they were failure-prone, often before the tubes used alongside. In time all solid-state chopping devices were to be developed, but this didn't impact vacuum tube chopper amps.

Frank Bradley and Rawley McCoy of the Reeves Instrument Corporation discussed yet another variation on the M9 op amp design in 1952 (see Reference 49). In the Bradley-McCoy circuit, a circuit similar to the M9 topology (but with a dual triode front end) was augmented by the addition of a chopper side path. The resulting amplifier had a DC gain of 30,000,00 (150 dB), and very low drift and offset voltage.

By the mid to late fifties many companies began offering solutions to analog computing using chopper-stabilized op amps. However, this wasn't true right after the chopper amplifier became available in the early 1950s—it came about later on.

Shortly after 1950 Granino and Theresa Korn published the first of their textbooks on analog computing, **Electronic Analog Computers** (see Reference 50). This book, along with the second edition in 1956, became the early op amp user's standard reference work. The op amp example fifth chapter of the first edition shows a few chopper-stabilized examples, and Goldberg's work is mentioned. By the time the second edition came out in 1956, chopper amplifiers dominated the examples.

Among the circuits presented in the Korn and Korn **Electronic Analog Computers**, first edition was a later version of the Bell Labs-designed op amp for the M9. A distinct evolutionary path can be noted in this schematic, shown in Figure 8-4.

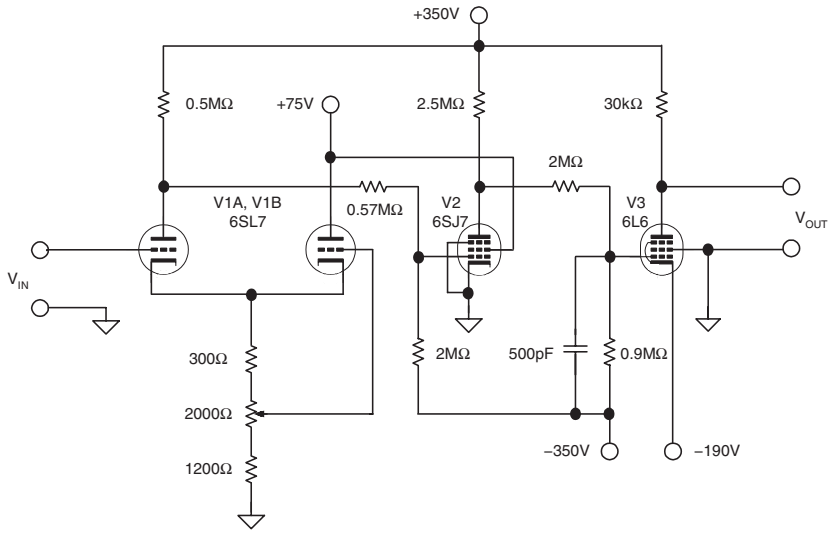


Figure 8-4: Schematic diagram of late M9 system op amp designed at Bell Telephone Laboratories

This version changes the input stage from a single pentode to a dual triode, with Miller compensation added for improved stability (adjustable by the 2 kΩ potentiometer). A close comparison finds that the Frost amplifier (Reference 47) is topologically almost identical with this M9 op amp version. And, vis-à-vis the original Swartzel design of Figure 8-3, further subtle changes to be noted are different ad compensation networks.

Use of the Noninverting Op Amp Input

One aspect of things that did not change was the use of the op amp signal input. All of the examples in the Korn and Korn book (Reference 50) use the op amp with the single-input, parallel feedback mode. In fact, although some of the op amp circuit examples shown in the book have balanced, dual triode inputs, engineering practice out in the world was still in the inverting-only mode. A glance at a topology such as Figure 8-4 reveals the difficulty with applying CM inputs—the amplifier simply was not designed to handle such signals. This was to change, but not very rapidly.

There are, of course, sound technical reasons why op amps didn't get much use in a noninverting mode. Probably the biggest single reason would be the fact that it was much more difficult to make an op amp work over a high CM range (such as ±100 V) which was then used with many circuits. This would require a major redesign of the front end and most likely would also have eliminated the use of chopper stabilization.

Despite that, one early reference to the use of the op amp in a noninverting signal manner was by Omar Patterson, in a patent filed in 1951 (see Reference 51). Although Patterson's patent is a broad array of analog computing circuits, it does utilize a common op amp structure, which is detailed as his Figure 1.

In this design Patterson uses a fully balanced dual triode front end, with the long-tailed pair's cathode current being established by a triode tube. With the balanced plate loading and regulated cathode current, the topology would have good CM response, and be capable of handling a fairly wide range of CM voltages. This op amp was reported to have a gain as high as 10,000 (80 dB), so it was capable of reasonable accuracy.

Patterson goes on in the patent to outline a voltage follower gain stage using this op amp (his Figure 10). In the extreme case of 100% feedback, the feedback stage's gain would be unity, with high input impedance. This is quoted for use of the circuit as an improved cathode follower. Quoting directly, "The advantages of this circuit lie in its extremely low output impedance, and its high degree of independence of tube characteristics."

George Philbrick and GAP/R

After WWII, George Philbrick also continued with op amp development work. Shortly thereafter he formed a company bearing his name, George A. Philbrick Researches, Inc., in 1946 (GAP/R). In many regards, Philbrick's work was instrumental in the development of op amp technology. His company was to see growth over the span of the vacuum tube technology days and well into the solid-state era.

Not too long after forming GAP/R, Philbrick introduced the world's first commercially available op amp, known as the K2-W. This modular 8-pin octal plug-in op amp was developed in 1952, and appeared in January 1953 (see Reference 52). A photo and schematic of this $20 op amp are shown in Figure 8-5.

The K2-W used two 12AX7 dual triodes, with one of the two tubes operated as a long-tailed pair input stage, which offered fully differential operation at the input. With the K2-W operating on ±300 V supplies, the input stage's 220 kΩ tail resistor was returned to the –300 V supply, fulfilling the long-tailed pair biasing requirement.

Half of the remaining 12AX7 dual triode was operated as a second gain stage, which in turn drove the remaining section as a cathode follower output, through a level shifter part 8355037 (typically thyrite devices). Overall gain of the K2-W was enhanced by positive feedback through the 150 kΩ resistor, connected back to the cathode of the second stage. Operating from the ±300 V power supplies @ 4.5 mA, the K2-W was able to achieve a ±50 V rated signal range at both input and output. DC gain was typically 15,000, and the entire circuit was packaged in a convenient, plug-in octal tube-based package.

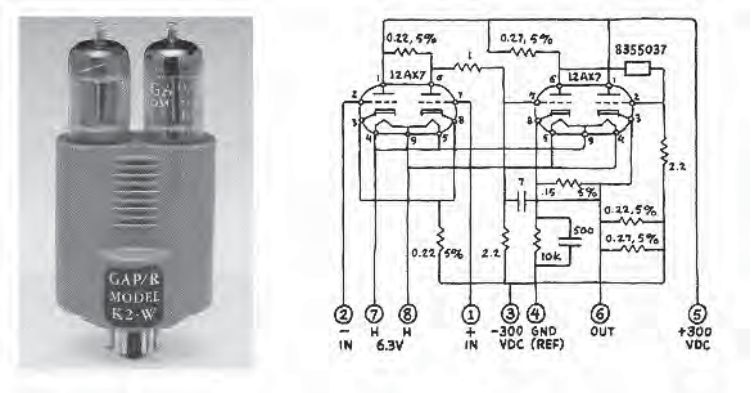


Figure 8-5: The GAP/R K2-W op amp, photo and schematic diagram (courtesy of GAP/R alumnus Dan Sheingold; schematic values in megohms and pF.)

Some vacuum tube op amp manufacturers provided chopper-stabilizer "add-on" units. In the case of GAP/R, this was the GAP/R K2-P. This unit, when used with the K2-W, formed a combination low drift, high gain op amp (see Reference 53).

Early on GAP/R set an excellent standard for application information, publishing a popular 1956 manual for the K2-W and related amplifiers which went through at least 10 printings by 1963 (Reference 53). GAP/R not only made available applications literature for their devices; they published a periodical devoted to analog computation, the **Lightning Empiricist**. It contained technical articles and new product information.

GAP/R also published what is now a classic set of reprints, the "Palimpsest" (see Reference 54). Some researchers see George A. Philbrick as a veritable op amp founding father. For example, Roedel, in his "An Introduction to Analog Computors" (Reference 54, again), gives Philbrick and Lovell credit for being the first op amp users.

It is also undoubtedly true that the GAP/R organization produced some of the best documentation and application support for op amps, both vacuum tube and solid state.

Because of the longevity of so many op amp principles, much of the wisdom imparted in the GAP/R app notes is still as valid today as it was in the 1950s. Although it did not appear until several years later, the best example of this is GAP/R's classic 1965 op amp book edited by Dan Sheingold, **Applications Manual for Computing Amplifiers…** (see Reference 55).

Armed with this book (and perhaps a copy of Korn and Korn's **Electronic Analog Computers**), the op amp user of the late 1960s was well prepared to face op amp circuit hardships. This was not just with analog computation tasks, but also the growing list of diverse applications into which op amps were finding new homes.

The Twilight Years of Vacuum Tube Op Amps

In the late 1950s and early 1960s, vacuum tube op amps had more or less reached their peak of technical sophistication, at least in terms of the circuitry within them. Packaging and size issues of course made a big impact on the overall appeal for the system designer, and work was done in these areas.

An interesting design using three 9-pin miniature dual triodes is shown in Figure 8-6. This compact design was done by Bela (Bel) Losmandy of Op Amp Labs (see Reference 56), then working with Micro-Gee Products, Inc. in 1956 (see Reference 57).

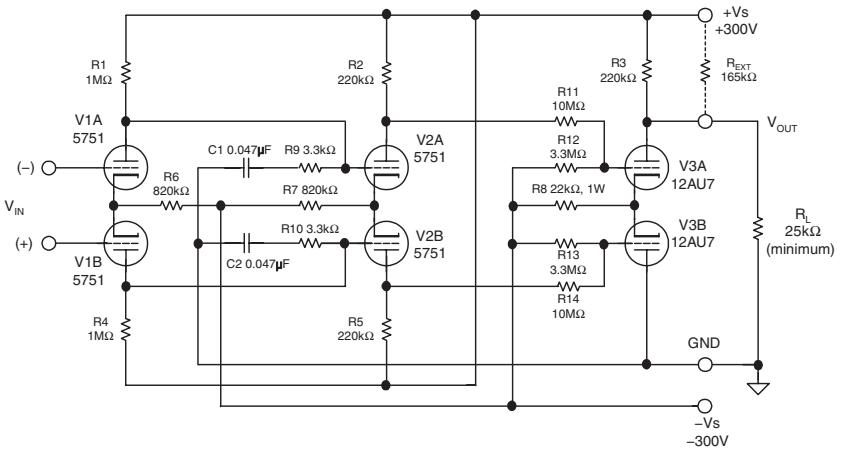


Figure 8-6: A fully differential op amp design by Bela Losmandy, for Micro-Gee Products, Inc.

There are several interesting aspects of this circuit. First, it is entirely differential, right up to the 12AU7 output stage. This allows it to handle CM inputs with lower errors, and improves the drift characteristics. As can also be noted, there is only one (dual) level shift circuit, following the V1–V2 directly coupled differential stages. This minimizes gain loss, and improves the overall performance. The entire amplifier operates on supplies of ±300 V @ 8 mA, and has a gain of more than 10,000 operating into a 25 kΩ load.

In the late 1950's and 1960's, two more publications appeared chronicling op amp developments. One was a long overview paper by Konigsberg, which appeared in 1959 (see Reference 59), the other was the analog and digital oriented computing handbook by Harry Husky and Granino Korn, **Computer Handbook**, in 1962 (see Reference 60). While this book was perhaps one of the last hurrahs for the vacuum tube op amp, it does contain a wealth of detailed design information on them.

By the time the 1960s rolled around, the solid-state era was already in progress. Vacuum tube op amps were on the wane, and smaller, low power, solid-state devices would soon take over op amp applications.

References: Vacuum Tube Op Amps

(Note—appended annotations indicate relevance to op amp history.)

Development of Differential Amplifier Techniques

1. B. H. C. Matthews, "A Special Purpose Amplifier," Proceedings of the Physiological Society, Vol. 81, March 1934, pp. 28, 29. *(A dual-triode differential amplifier, with dual triode common-cathodes biased to ground through a high resistance, ac-coupled at the output.)*
2. A. D. Blumlein, "Improvements in or Relating to Thermionic Valve Amplifying Circuit Arrangements," **UK Patent 482,740**, filed July 4, 1936, issued April 4, 1938. *(A basic common-cathode/resistance-biased-to-common, dual-triode differential amplifier, ac-coupled at input and output.)*
3. Franklin Offner, "Push-Pull Resistance Coupled Amplifiers," **Review of Scientific Instruments**, Vol. 8, January, 1937, pp. 20, 21. (*AC-coupled, cascade differential amplifier circuits, including the use of the dual-triode common-cathodes biased to ground through a high resistance.)*
4. O. H. Schmitt, "A Simple Differential Amplifier," **Review of Scientific Instruments**, Vol. 8, No. 4, April, 1937, pp. 126, 127. *(A basic common-cathode/cathode-to-common, dual-pentode differential amplifier, with plate-screen coupling, single-ended dc-coupling at the output.)*
5. J. F. Toennies, "Differential Amplifier," **Review of Scientific Instruments**, Vol. 9, March, 1938, pp. 95–97. *(A differential amplifier circuit that uses a triode and pentode in a common-cathode configuration, biased to a negative voltage through a high resistance.)*
6. O. H. Schmitt, "Cathode Phase Inversion," **Journal of Scientific Instruments**, Vol. 15, No. 3, 1938, pp. 100, 101. *(A circuit is presented as a single-input phase inverter, but is also a true dc-coupled, differential-input/differential-output amplifier topology. The dual triodes have their common cathodes biased to a negative voltage through a high resistance.)*
7. Lionel Jofeh, "Improvements in Electric Circuits Comprising Electronic Discharge Devices," **UK Patent 529,044**, filed May 9, 1939, issued Nov. 13, 1940. *(A catalog of the various forms of dual triode, dual pentode differential amplifier circuits, with variations in methods of cathode coupling.)*
8. Harold Goldberg, "A High-Gain DC Amplifier for Bio-Electric Recording," **Transactions AIEE**, Vol. 59, January 1940, pp. 60–64. *(A completely differential, multistage, direct-coupled, high gain amplifier for biomedical work. Illustrates the use of common-cathode bias resistance for reducing sensitivity to in-phase inputs.)*
9. O. H. Schmitt, "Cathode Phase Inversion," **Review of Scientific Instruments**, Vol. 12, No. 11, November 1941, p. 548. *(An expansion of previous work of the same name; includes a true dc-coupled, differential-input/differential-output amplifier topology, with the dual-triode common-cathodes biased to a negative voltage through a high resistance.)*
10. Walther Richter, "Cathode Follower Circuits," **Electronics**, November 1943, pp. 112–117, 312. *(Analysis of various cathode follower circuits, including the long-tailed differential pair.)*
11. Harold Goldberg, "Bioelectric-Research Apparatus," **Proceedings of IRE**, Vol. 32, June 1944, pp. 330–336. *(Another differential, multi-stage, direct-coupled, high gain amplifier for biomedical work. Illustrates the use of pentode bias resistance for long-tailed pair; uses battery operated front end.)*
12. G. Robert Mezger, "A Stable Direct-Coupled Amplifier," **Electronics**, July, 1944, pp. 106–110, 352, 353. *(A stable, high gain, differential-input/differential-output, direct-coupled amplifier. Uses novel active device interstage coupling technique.)*

13. Franklin Offner, "Balanced Amplifiers," **Proceedings of IRE**, Vol. 33, March 1945, p. 202. *(A criticism of other differential amplifier circuit papers.)*

14. D. H. Parnum, "Biological Amplifiers, Parts 1 and 2," **Wireless World**, Nov. 1945, pp. 337–340, and Dec. 1945, pp. 373-376. *(A survey of various differential amplifier techniques, with a multistage ac-coupled design example.*)

15. Denis L. Johnston, "Electro-Encephalograph Amplifier, Parts 1–3," **Wireless Engineer**, August 1947, pp. 231–242, Sept. 1947, pp. 271–277, and October 1947, pp. 292–297. *(A comprehensive overview of various biological differential amplifier techniques with many example circuits, both dc- and ac-coupled. Includes 61 references.*)

16. D. H. Parnum, "Transmission Factor of Differential Amplifiers," **Wireless Engineer**, April 1950, pp. 125–129. *(An analysis of the common-mode and differential signal response of differential amplifiers.*)

17. P. O. Bishop, E. J. Harris, "A DC Amplifier for Biological Application," **Review of Scientific Instruments**, Vol. 21, No. 4, April 1950, pp. 366–377. *(A very sophisticated differential amplifier system, employing common-mode feedback, active differential pair current sources, input shield bootstrapping, power supply stabilization, and so forth. Many references cited.)*

18. Richard McFee, "Improving Differential Amplifier Rejection Ratio," **Review of Scientific Instruments**, Vol. 21, No. 8, August 1950, pp. 770–771. *(A feedback modification to a standard dual triode differential stage to improve common-mode rejection.)*

19. Harry Grundfest, "Biological Requirements for the Design of Amplifiers," **Proceedings of the IRE**, Vol. 38, September 1950, pp. 1018–1028. *(An overview of amplifier requirements for biological measurements; includes commentary on the history of differential amplifier development.)*

20. C. M. Verhagen, "A Survey of the Limits in DC Amplification," **Proceedings of the IRE,** Vol. 41, May 1953, pp. 615–630. *(A technical discussion of both tube and circuit parameters which impact DC stability.)*

Op Amp and Analog Computing Developments

21. George A. Philbrick, "Designing Industrial Controllers by Analog," **Electronics**, June 1948. *(Figure 3b example of an early analog computation circuit.)*

22. Per A. Holst, "George A. Philbrick and Polyphemus—The First Electronic Training Simulator," **IEEE Annals of the History of Computing**, Vol. 4, No. 2, April 1982, pp. 143–156. *(George A. Philbrick's analog computing circuitry at Foxboro, late 1930s.)*

23. H. C. Higgins, et al, "Defense Research at Bell Laboratories: Electrical Computers for Fire Control," **IEEE Annals of the History of Computing**, Vol. 4, No. 3, July, 1982, pp. 218–236. See also: M. D. Fagen, Ed. **A History of Engineering and Science in the Bell System**, Vol. 2, "National Service in War and Peace, 1925–1975," Bell Telephone Laboratories, 1978, ISBN 0-0932764-001-2. *(A summary of various Bell Labs fire control analog computer developments, including op amps and feedback components. Note—the IEEE article is reprinted from the broader, more detailed Bell Telephone Laboratories volume.)*

24. James S. Small, "General-Purpose Electronic Analog Computing: 1945–1965," **IEEE Annals of the History of Computing**, Vol. 15, No. 2, 1993, pp. 8–18. *(An overview of analog computing, includes discussion of early operational amplifiers.)*

25. David A. Mindell, "Automation's Finest Hour: Bell Labs and Automatic Control in World War II," **IEEE Control Systems**, December 1995, pp. 72–80. *(Narrative of the T10 computer system and the M9 gun director developments at Bell Labs.)*

26. C. A. Lovell, et al, "Artillery Predictor," **US Patent 2,404,081**, filed May 1, 1941, issued September 24, 1946. *(The mathematics of analog computer system using op amps for functions of repeating, inverting, and summing amplifiers, plus differentiation.)*

27. C. A. Lovell, et al, "Electrical Computing System," **US Patent 2,404,387**, filed May 1, 1941, issued July 23, 1946. *(An analog computer system using op amps for control.)*

28. C. A. Lovell, "Continuous Electrical Computation," **Bell Laboratories Record**, 25, March, 1947, pp. 114–118. *(An overview of various fire-control analog computational circuits of the T10 and M9 systems, many illustrating uses of op amps.)*

29. W. H. Boghosian, et al, "Artillery Director," **US Patent 2,493,183**, filed May 21, 1942, issued Jan. 3, 1950. *(An artillery fire control system using op amps for control.)*

30. K. D. Swartzel, Jr., "Summing Amplifier," **US Patent 2,401,779**, filed May 1, 1941, issued July 11, 1946. *(The first operational amplifier, used as a summing amplifier.)*

31. Recognition of Harold Black, "Historic Firsts: The Negative Feedback Amplifier," **Bell Laboratories Record**, Vol. 22, No. 4, December, 1943, p. 173. *(A Bell Laboratories tribute to the Black negative feedback amplifier invention.)*

32. "Electrical Gun Director Demonstrated," **Bell Laboratories Record**, Vol. 22, No. 4, December 1943, pp. 157–167. See also: "Development of the Electrical Director," **Bell Laboratories Record**, Vol. 22, No. 5, January 1944, pp. 225–230. *(Bell Laboratories narratives of the M9 gun director system demonstration and development.)*

33. J. R. Weeks, "Polystyrene Capacitors," **Bell Laboratories Record**, 24, March, 1946, pp. 111–115. *(Development of a new capacitor film dielectric for electronic analog computer networks.)*

34. E. C. Hageman, "Precision Resistance Networks for Computer Circuits," **Bell Laboratories Record**, 24, December, 1946, pp. 445–449. *(Development of precision resistor networks for electronic analog computers.)*

35. C. Pfister, "Precision Carbon Resistor," **Bell Laboratories Record**, 26, October, 1946, pp. 401–406. *(Development of deposited carbon resistors for electronic analog computers.)*

36. D. G. Blattner, "Precision Potentiometers for Analog Computers," **Bell Laboratories Record**, 32, May, 1954, pp. 171–177. *(Development of precision wire wound potentiometers for use in electronic analog computers.)*

37. Recognition of M9 Designers C. A. Lovell, D. B. Parkinson, and J. J. Kuhn, "Medals for Merit," **Bell Laboratories Record**, Vol. 27, May, 1947, p. 208. *(The Medal for Merit awarded to the M9 designers on April 8, 1947 is the nation's highest civilian award.)*

38. Robert Buderi, **The Invention That Changed the World**, Simon and Schuster, 1996, ISBN: 0-684-81021-2. *(A marvelous account of radar development during WWII, centered largely on the MIT Radiation Lab team—includes a narrative on the integration of the M9 fire control system with the SCR-584 radar, and the system's operational success.)*

39. David A. Mindell, **"Datum for its Own Annihilation:" Feedback, Control and Computing 1916–1945**, PhD thesis, MIT, May 2, 1996. *(Historical survey of computing control systems. Chapter 8 of this work is 'Radar and System Integration,' which covers the Bell Labs work on the T10 and M9 gun director projects.)*

Naming the Op Amp

40. John R. Ragazzini, Robert H. Randall and Frederick A. Russell, "Analysis of Problems in Dynamics by Electronic Circuits," **Proceedings of the IRE**, vol. 35, May 1947, pp. 444–452. *(An overview of operational amplifier uses, and first formal definition of the term.)*
41. George Rostky, "Unsung Hero Pioneered Op Amp," **EE Times**, March 24, 1997, or, www.eetonline.com/anniversary/designclassics/opamp.html. *(A narrative on the op amp work of Loebe Julie at Columbia University during WWII [and footnoted in the Ragazzini paper]. A schematic diagram of the Julie op amp is included.)*
42. Bob Pease, "What's All This Julie Stuff, Anyhow?," **Electronic Design**, May 3, 1999, or, www.elecdesign.com/Articles/ArticleID/6071/6071.html *(Another narrative on the op amp work of Loebe Julie at Columbia University during WWII [and footnoted in the Ragazzini paper].)*

Evolution of the Vacuum Tube Op Amp

43. Stewart E. Miller, "Sensitive DC Amplifier with AC Operation," **Electronics**, November, 1941, pp. 27– 31, 106–109. *(Design example of a stable, high-gain direct-coupled amplifier including 'cathode-compensation' against variations in filament voltage, use of glow tube inter-stage coupling, and a stable line-operated dc supply.)*
44. Edward L. Ginzton, "DC Amplifier Design Techniques," **Electronics**, March 1944, pp. 98–102. *(Various design means for improving direct-coupled amplifiers.)*
45. Maurice Artzt, "Survey of DC Amplifiers," **Electronics**, August, 1945, pp. 112–118. *(Survey of direct-coupled amplifier designs, both single-ended and differential, with emphasis on high stability.)*
46. George E. Valley, Jr., Henry Wallman, **Vacuum Tube Amplifiers**, MIT Radiation Labs Series No. 18, McGraw-Hill, 1948. *(A classic WWII Radiation Lab development team textbook. Chapter 11, by John W. Gray, deals with direct-coupled amplifiers.)*
47. Seymour Frost, "Compact Analog Computer," **Electronics**, July, 1948, pp. 116–120, 122. *(A description of the Reeves Electronic Analog Computer [REAC], which used as the computing amplifier a circuit similar to the M9 op amp. Uses a Miller-compensated triode input stage.)*
48. E. A. Goldberg, "Stabilization of Wide-Band Direct-Current Amplifiers for Zero and Gain," **RCA Review**, June 1950, pp. 296–300. See also: "Stabilized Direct Current Amplifier," **US Patent 2,684,999**, filed April 28, 1949, issued July 27, 1954. *(A system for lowering vacuum tube op amp offset voltage, drift, and gain errors, by means of an ac-coupled parallel-path, with synchronous rectification, and dc signal reinsertion—in short, the* chopper-stabilized *op amp.)*
49. Frank R. Bradley, Rawley McCoy, "Driftless DC Amplifier," **Electronics**, April 1952, pp. 144–148. *(A description of the Reeves A-105 Analog Computer, which used as the computing amplifier a circuit partially similar to the M9 op amp. Adds chopper stabilization for low drift.)*
50. Granino Korn and Theresa Korn, **Electronic Analog Computers,** McGraw-Hill, 1952. *(A classic early work on the uses and methodology of analog computing. In Chapter 5, an op amp circuit attributed to Bell Labs and the M9 project is described, along with many other examples, and design details.)*
51. Omar L. Patterson, "Computing Circuits," **US Patent 2,855,145**, filed July 30, 1951, issued Oct. 7, 1958. *(A catalog of analog computation circuits based on a fully differential input op amp circuit, including use of a voltage follower configuration.)*
52. **Data Sheet For Model K2-W Operational Amplifier**, George A. Philbrick Researches, Inc., Boston, MA, January 1953. See also "40 Years Ago," **Electronic Design**, December 16, 1995, p. 8. *(The George A. Philbrick Research dual triode K2-W, the first commercial vacuum tube op amp.)*

53. Henry Paynter, Ed., **Applications Manual for PHILBRICK OCTAL PLUG-IN Computing Amplifiers**, George A. Philbrick Researches, Inc., Boston, MA, 1956. *(The first op amp application manual.)*

54. Jerry Roedel, "An Introduction to Analog Computors," within **Palimpsest on the Electronic Analog Art**, George A. Philbrick Researches, Inc., Boston, MA,1955. *(Roedel's paper is one of many analog computing papers, [including Ragazzini et al, above].)*

55. Dan Sheingold, Ed., **Applications Manual for Operational Amplifiers for Modeling, Measuring, Manipulating, and Much Else**, George A. Philbrick Researches, Inc., Boston, MA, 1965. *(The classic GAP/R op amp application manual, now a collector's item.)*

56. **Opamp Labs Inc.,** 1033 N Sycamore Avenue, Los Angeles, CA, 90038 (323) 934-3566, www.opamplabs.com/bel.htm.

57. Bela Losmandy, **Three Stage Micro-Gee Products, Inc**.**Op Amp**, 1956.

58. Granino Korn and Theresa Korn, **Electronic Analog Computers, Second Edition** McGraw-Hill, 1956. *(Second edition of the classic work on the uses and methodology of analog computing. Chapter 5 features an increased number of op amp circuits, many chopper-stabilized.)*

59. R. L. Konigsberg, "Operational Amplifiers," **Advances in Electronics and Electron Physics**, Vol. 11, 1959, pp. 225–285. *(An overview of vacuum tube and [some] solid-state op amps, with 75 references.)*

60. Harry Husky, Granino Korn, **Computer Handbook**, McGraw-Hill, 1962. *(An encyclopedic reference work on analog computing. Includes detailed op amp design section by Edward Billinghurst, plus a comprehensive list of op amp circuit examples, with specifications.)*

This page intentionally left blank

SECTION 8-3

Solid-State Modular and Hybrid Op Amps

Vacuum tube op amps continued to flourish for some time into the 1950s and 1960s, but their competition was eventually to arrive from solid-state developments. These took the form of several key innovations, all of which required a presence before effective solid-state op amp designs could be established. This discussion treats *modular and hybrid* solid-state op amps, which preceded and overlapped solid-state IC op amps.

There were three of these key developments, the invention of *the transistor*, the invention of *the integrated circuit* (IC), and the invention of *the planar IC process*. A detailed history of solid-state inventions and related process developments can be found in articles celebrating the transistor's 50th anniversary, within the Autumn 1997 **Bell Labs Technical Journal** (see References 1 and 2).

Birth of the Transistor

John Bardeen, Walter Brattain, and William Shockley of Bell Labs, working with *germanium* semiconductor materials, first discovered the transistor effect in December of 1947. Of course, this first step was a demonstration of gain via a new principle, using a semiconducting material, as opposed to a vacuum tube. But more remained to be done before commercial transistors were to appear. For their achievement, the trio received the 1956 Nobel Prize in physics. In addition to vacuum tubes, circuit designers now had a lower voltage, lower power, miniature amplifying device (see References 3 and 4).

Over the course of the next 10 years or more, various means were explored to improve the germanium transistors. The best germanium transistors were still relatively limited in terms of leakage currents, general stability, maximum junction temperature, and frequency response. Some of these problems were never to be solved. While many performance improvements were made, it was recognized early that *silicon* as a semiconductor material had greater potential, so this occupied many researchers.

In May of 1954, Gordon Teal of Texas Instruments developed a grown-junction *silicon* transistor. These transistors could operate to 150°C, far higher than germanium. They also had lower leakage, and were generally superior amplifying devices. Additional processing refinements were to improve upon the early silicon transistors, and eventually lead a path to the invention of the first integrated circuits in the late fifties.

Birth of the IC

In 1958, Jack Kilby of Texas Instruments invented the *integrated circuit*, now known universally as the IC (see Reference 5). For this effort he was ultimately to become a co-recipient of the 2000 Nobel Prize in physics.

Kilby's work, however, important as it was, could arguably be said to be nonexclusive in terms of first authorship of the integrated circuit. In early 1959, Robert Noyce, an engineer at Fairchild Semiconductor, also developed an IC concept (see Reference 6).

The nucleus of Noyce's concept was actually closer to the concept of today's ICs, as it used interconnecting metal trace layers between transistors and resistors. Kilby's IC, by contrast, used bond wires.

As might be expected from such differences between two key inventions, so closely timed in their origination, there was no instant consensus on the true "IC inventor." Subsequent patent fights between the two inventor's companies persisted into the 1960s. Today, both men are recognized as IC inventors.

The Planar Process

In general parallel with the Noyce's early IC developments, Jean Hoerni (also of Fairchild Semiconductor) had been working on means to protect and stabilize silicon diode and transistor characteristics. Until that time, the junctions of all *mesa* process devices were essentially left exposed. This was a serious limitation of the mesa process.

The mesa process is so named because the areas surrounding the central base-emitter regions are etched away, thus leaving this area exposed on a plateau, or mesa. In practice, this factor makes a semiconductor so constructed susceptible to contaminants, and as a result, inherently less stable. This was the fatal flaw that Hoerni's invention addressed.

Hoerni's solution to the problem was to re-arrange the transistor geometry into a flat, or *planar* surface, thus giving the new process its name (see References 7 and 8). However, the important distinction in terms of device protection is that within the planar process the otherwise exposed regions are left covered with silicon dioxide. This feature reduced the device sensitivity to contaminants; making a much better, more stable, transistor or IC.

With the arrangement of the device terminals on a planar surface, Hoerni's invention was also directly amenable to the flat metal conducting traces that were intrinsic to Noyce's IC invention. Furthermore, the planar process required no additional process steps in its implementation, so it made the higher performance economical as well. As time has now shown, the development of the planar process was another key semiconductor invention. It is now widely used in production of transistors and ICs.

At a time in the early 1960s shortly after the invention of the planar process, the three key developments had been made. They were the (silicon) transistor itself, the IC, and the planar process. The stage was now set for important solid-state developments in op amps. This was to take place in three stages. First, there would be *discrete transistor* and *modular* op amp versions, second there would be *hybrid op amps*, which could be produced in a couple of ways. One hybrid method utilized discrete transistors in chip form(s), interconnected to form an op amp; another was a specially matched transistor pair combined with an IC op amp for improved performance, and thirdly, the op amp finally became a complete, integral, dedicated IC—the *IC op amp*. This latter developmental stage is covered more fully within the next section of this chapter.

Of course, within these developmental stages there were considerable improvements made to device performance. And, as with the vacuum tube/solid-state periods, each stage overlapped the previous and/or the next one to a great extent.

Solid-State Modular and Hybrid Op Amp Designs

There were new as well as old companies involved in early solid-state op amps. GAP/R was already well established as a vacuum tube op amp supplier, so solid-state op amps for them were a new form of the same basic product. With GAP/R and others in the 1960s, the Boston area was to become the first center of the solid-state op amp world. Elsewhere, other companies were formed to meet market demand for the more compact transistor op amps. Burr-Brown Research Corporation in Arizona fell into this category. Formed by Robert Page Burr and Thomas Brown in 1956, Burr-Brown was an early modular op amp supplier, and supported their products with an applications book (see Reference 9). The Burr-Brown product line grew steadily over the years, emerging into a major supplier of precision amplifiers and other instrumentation ICs. Texas Instruments bought Burr-Brown in 2000, merging the product lines of the two companies.

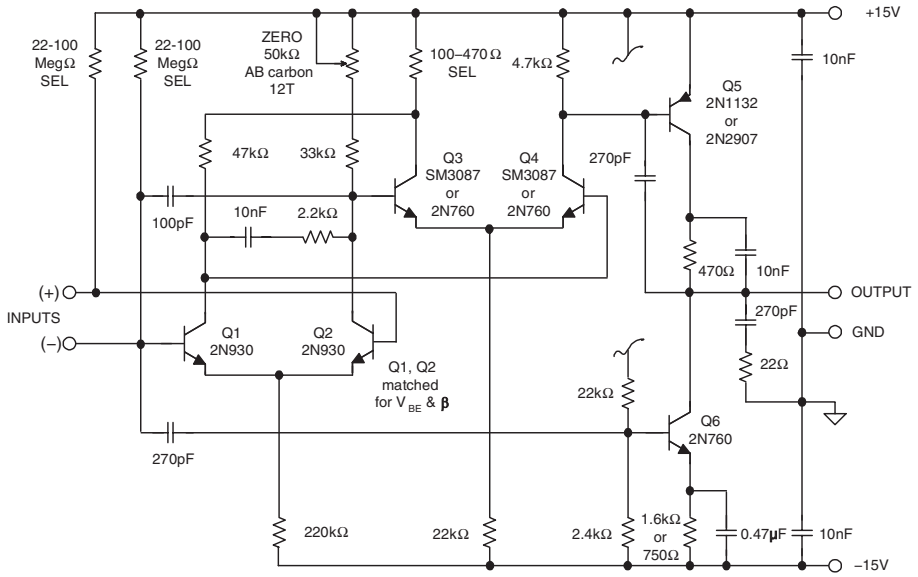


Figure 8-7: The GAP/R model P65 solid-state op amp

On the other hand, in 1960 G—AP/R was a transitioning company, and while they maintained the vacuum tube op amp line for some time, they stayed away from solid-state op amps until quality silicon transistors could be found. GAP/R began to introduce solid-state op amps in the early 1960s. George Philbrick was simply unwilling to produce germanium transistor solid-state op amps, and he also had specific ideas about the optimum amplifier topology that could be used—more on this follows.

The new solid-state op amps were to transition power supply and signal range standards from ±300 V/±100 V down to ±15 V/±10 V, a standard that still exists today. And of course, new packaging for the op amps was to emerge, in several forms.

The GAP/R P65, shown above in Figure 8-7, was a general-purpose device. It was designed by Alan Pearlman, with later revisions by Bob Malter, and was produced from 1961 through 1971. The first stage Q1-Q2 used a pair of matched 2N930s, with a tail current of 66 μA, and had hand-selected bias compensation (the SEL resistors).

The second P65 stage of Q3-Q4 ran at substantially more current, and featured a gain-boosting positive feedback loop via the SEL and 47 kΩ resistors. The common-emitter output stage was PNP Q5, loaded by NPN current source Q6. The two-stage NPN differential pair cascade used in the P65 design was to become a basic part of other GAP/R op amps, such as the P45 (described below).

Small value feedforward capacitors sped up the ac response, and an output RC snubber provided stability, along with phase compensation across the Q1-Q2 collectors. The transistor types shown represented the original P65, but later on the P65A used better transistors (such as the 2N2907), and thus could deliver more output drive.

Another GAP/R solid-state op amp was the P45, shown in Figure 8-8 as a photo of the card-mounted op amp, and the schematic. The P45 was designed by Bob Pease, and was introduced in 1963 (see Reference 10). The edge connector card package shown was used with the P45 and P65, as well as many other GAP/R solid-state amplifiers.

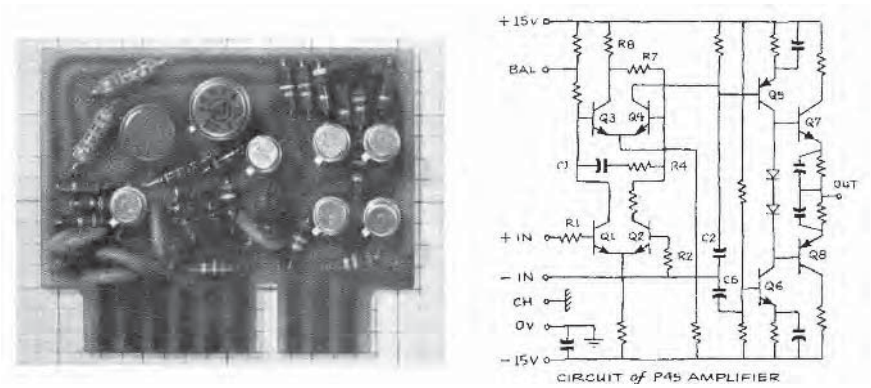


Figure 8-8: The GAP/R model P45 solid-state op amp

The P45 design was aimed at fast, inverting mode applications. With a class AB output stage, the P45A could deliver ±10 V at ±20 mA to the load. Gain was rated a minimum of 50,000 at 25°C into a load of 500 Ω. One of the more outstanding specifications of the P45 was its gain-bandwidth product of 100 MHz. In 1966, a P45A cost $118 in quantities of 1–4 (see Reference 11). Both the P65 and P45 ran on ±15 V, the new power standard, and were intended for input/output signal ranges of ±10 V.

As mentioned, the cascaded NPN differential pair topology used in the P45 and P65 designs was to become a basic part of other GAP/R op amps. A feature of the design was the controlled positive feedback path, from the Q3 collector back to the Q4 base. Offset was controlled by a potentiometer connected between the BAL pin and 15 V in the P45, with a similar arrangement used in the P65 (Figure 8-7).

In the P45, the first two gain stages are followed by PNP common-emitter stage Q5, which provides a great deal of the voltage gain. Emitter followers Q7 and Q8 buffer the high impedance node at Q5's collector, providing a low impedance source to the load.

In 1962 Alan Pearlman and partner Roger R. (Tim) Noble formed their own Boston-area company, Nexus Research Laboratory, Inc. Nexus competed with both GAP/R and Burr-Brown in the growing solid-state op amp field (and ultimately with a third local company). The Nexus mission was to deliver solid-state op amps to customers for printed circuit board mounting, thus the Nexus designs used a rectangular, potted module package. They were so popular that they influenced GAP/R to follow suit with modular designs of their own.

In 1962, George Philbrick himself did the layout of another P65 derivative, the PP65, which was one of the first GAP/R modules. Shown in Figure 8-9, this square outline, 0.2" centered, 7-pin footprint was to become more or less a modular op amp standard. It used five pins for output/power/offset on one side, with the two input pins on the opposite side.

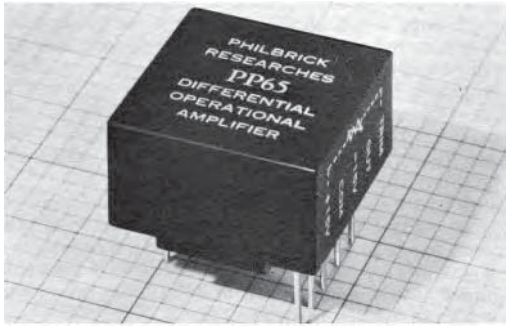


Figure 8-9: The GAP/R model PP65 potted module solid-state op amp

It might be easy for some to dismiss the importance of a package design within a chart of op amp progress. Nevertheless, the modular package format opened up new opportunities and, for the first time, allowed the op amp to be treated *as a component*. This opening of application opportunities enhanced op amp growth significantly.[1]

Varactor Bridge Op Amps

George Philbrick championed a novel op amp type that became a GAP/R profit maker—the *varactor bridge* amplifier. In this circuit, voltage variable capacitors (varactors) are used in an input stage that processes the op amp error voltage as a phase-sensitive ac carrier. By careful bridge component arrangement, the op amp input terminals are forced to see only tiny dc leakage currents, i.e., as small as 1 pA (or in some cases, much less).

As a result, a varactor bridge op amp achieved the lowest input current of any op amp available in the solid-state period. Lower than common tubes, in fact. In addition, since there was no input dc path to common, the allowable input CM voltage of a varactor bridge op amp could go very high—to levels as high as ±200 V.

[1] This pattern was to be repeated again and again with op amps, and continues even today, with miniature SOIC packages displacing DIP and other through-hole packages.

Figure 8-10 illustrates in block diagram form a varactor bridge op amp. There are four main components, the front end composed of the bridge circuit and a high frequency oscillator, an ac amplifier to gain-up the bridge output error voltage, a synchronous phase detector to convert the amplified ac error to a corresponding dc error, and finally an output amplifier, providing additional dc gain and load drive.

The circuit worked as follows: A small dc error voltage V_{IN} applied to the matched varactor diodes D1 and D2 causes an ac bridge imbalance, which is fed into the ac amplifier. This ac voltage will be phase-sensitive, dependent upon the dc error. The remaining parts of the loop amplify and detect the dc error.

To apply the amplifier, an external feedback loop is closed from V_{OUT} back to the inverting input terminal, just as with conventional op amps. The difference in the case of the varactor bridge op amp lies in the fact that two unusual degrees of freedom existed, in terms of both bias current and CM voltage.

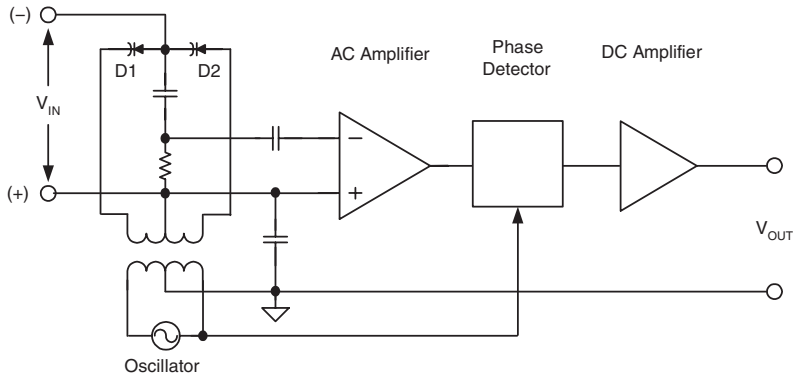


Figure 8-10: Generalized block diagram for a varactor bridge solid-state op amp

The GAP/R varactor bridge op amp model was called the P2. It was a premium part in terms of the dc specifications, but not speed. In fact, the unity-gain frequency was just 75 kHz, but the specification that people keyed on was the ±10 pA input offset current. Also, the CM range of ±200 V very likely enabled a few applications that previously might have required the use of a tube amplifier to address.

In 1966, an SP2A sold for a then astronomical price of $227 (see Reference 11). Bob Pease wrote a fascinating narrative on the P2's collaborative development at GAP/R, which was by engineers George Philbrick and Bob Malter (see Reference 12).

George Philbrick was also issued a patent on a varactor bridge amplifier, in 1968 (see Reference 13). In 1966 GAP/R and Nexus Research Laboratories were purchased by Teledyne Corporation, and the merged product line continued into hybrids and ICs.

Later on there was to be a sad note in this GAP/R history. GAP/R founder and master innovator George Philbrick passed away in late 1974, at a relatively young age of 61. A tribute to George Philbrick was offered by his partner and collaborator, Professor Henry Paynter of MIT (see Reference 14).

The Birth of ADI

The emergence of a third Boston-area op amp company took place in the mid 1960s. In January of 1965 Analog Devices Inc. (ADI) was founded by Matt Lorber and Ray Stata. Operating initially from

Cambridge, MA, op amps were the first product of the new company. Many of the early op amps were modular designs (more on this below).

Dan Sheingold has suggested that the ADI founders may have intentionally left out the word "Research" as part of the ADI name (see Reference 15). This would be to differentiate the new company from all of the (then) three competitors, Burr-Brown, GAP/R, and Nexus Research Laboratories, and thus broaden market appeal for op amps.

And, it seemed to work for the new ADI venture, with sales taking off quite soon. One of the first "products" of the new ADI was application support for op amps (also noted by Sheingold, Reference 15). In the first year, Ray Stata authored a comprehensive guide to op amps (see Reference 16). Examples of this application support were to continue through the early years and afterwards, echoing a successful business practice established by GAP/R.

The first few ADI years resulted in many new op amps, in mostly the modular package style, using both bipolar transistor and FET technologies. A complete list is much more broad than can be covered here, so just some highlights will be sampled.

Model 3xx Series Varactor Bridge Op Amps

To compete with GAP/R and their P2, ADI marketed a number of varactor bridge input op amps. The first varactor bridge op amps were the 301, 302, and 303 models, which were all similar, but differed in detail as to the input mode. They were differential (301), inverting (302), or noninverting (303). The 301 had a max input current of 2 pA, but the others got as low as 0.5 pA. The 301 sold for $198, while the 302 A and 303 A were $110.

Lewis R. Smith designed these amplifiers, as well as their successors, models 310 and 311 (see Reference 17). These latter designs were able to achieve significantly improved input currents, which were ±10 fA for the signal input of both amplifiers (just about three orders of magnitude below the GAP/R P2 series). An input current specification this low was then (and still is) a most impressive achievement. Interestingly, the 310 and 311 models were also sold for lower prices, which was $75 for the J grade.

Lewis Smith also described his varactor bridge designs in a patent (see Reference 18). It is a high tribute to the model 310 and 311 designs that they are still being produced in 2004. The devices are available through Intronics (see Reference 19).

The Many Op Amp Categories

Many of the earliest ADI modular op amps used bipolar transistors for the input stages, and they all used bipolar transistors in later stages. Matched duals of either bipolar or FET types were scarce in the early 1960s, but these were incorporated into designs soon after announcement. An early listing of ADI op amps has five categories: general purpose, low bias current, low drift, wideband, and high voltage/current (see Reference 20). This list was expanded considerably in only a year (see Reference 21).

In the general-purpose types, the models 111 and later the 118 were popular units, due to a combination of good basic specs and attractive prices. The varactor types already mentioned led performance for low bias current types, but there were also FET input types such as the early model 142 with bias currents in the tens of pA range.

In the low drift category, various chopper amplifiers such as the 210, 211, 220, and later the 232 and 233, and the 260 led in performance, There were also low drift chopperless amplifiers such as the 180 and 183, using precision bipolar transistor front ends. There was considerable support for choppers over the next few years (see References 22–24).

Model 121 Op Amp

A design done by Dick Burwen for ADI was the model 121, a fast, fully differential op amp, in 1966. This design demonstrates some useful circuit techniques in Figure 8-11.

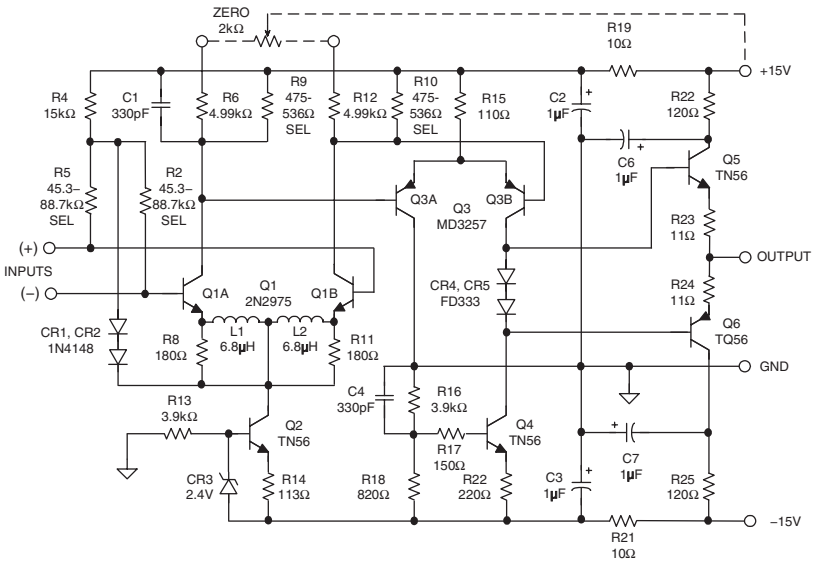


Figure 8-11: The ADI model 121 wideband DC op amp

One of the techniques is how to make a high speed, low noise input stage, which is by means of the L1–L2 chokes. At low frequencies the chokes shunt the otherwise noisy degeneration resistors, R8–R9. It also shows the use of relatively heavy bypassing and decoupling internal to the op amp (a necessary practical step, but possible within the confines of a module).

The model 121 NPN input stage runs at a high tail current, for fast slewing. But, note that the R2 and R5 resistors compensate the input bias current, which would otherwise be high. These (selected) resistors provide a temperature tracking bias from the floating diode source, CR1–CR2. This bias scheme was patented by Burwen, and was also used in other ADI op amps of the period (see Reference 25).

As can be noted, the model 121 used a current source for the 2N2975 matched NPN pair input stage, Q2, to optimize CMR. In critical locations, 1% metal film resistors are also used. The gain-of-five stable model 121 had a gain of 25,000 (or 88 dB), achieved a slew rate of 250 V/µs, and sold for $98 in 1968 (see Reference 20).

Analog Dialogue Magazine is Born

ADI's continuing thread of customer support through applications information was enhanced considerably in 1967, when the magazine **Analog Dialogue** was launched (see Reference 26). The initial charter for the magazine was stated as "A Journal for the Exchange of Operational Amplifier Technology," later on this was broadened to "A Journal for the Exchange of Analog Technology."

But, disseminate op amp info is what the early **Analog Dialogue** did, and also what it did well. The premier issue featured an op amp article by Ray Stata that is still available as an app note (see Reference 27). And, a similar comment can also be made for a subsequent Ray Stata article (see Reference 28).

A milestone in the life of the young magazine was the arrival of Dan Sheingold as editor, in 1969 (see Reference 29). Already highly experienced as a skilled op amp expert and editorial writer from vacuum tube and early solid-state years at GAP/R, Dan Sheingold brought a unique set of skills to the task of editorial guidance for **Analog Dialogue.** Dan's leadership as editor continues today. For more than 35 years his high technical communication standards have been an industry benchmark.

A Family of High Speed FET Op Amp Designs

One of the more illuminating development threads to be found within the ADI op amp portfolio is that of the high-speed FET input modular and hybrid products. This design family began with the model 45 in 1970 (see Reference 30). John Cadigan designed all of these amplifiers, and they continued evolving over the next 10 years or more.

The reasons for this product line's longevity (which extended well into the era of IC op amps) is simply that these amplifiers met difficult technical needs. These needs weren't to be solved by early IC amplifiers, and indeed were not met by ICs at all, until better processes became available. The combination of high speed (meaning here fast settling to a defined narrow error band) and excellent dc accuracy made these igh speed FET amplifiers the best answer for accurately driving A/D converters and other accuracy-critical amplifier needs.

Model 45, 44 and 48 FET Op Amps

The Model 45 was out first, and was targeted for lower cost applications, with under 1μs settling time to 0.01%. The next two models of the series were the 44 and 48, as represented in a simplified schematic shown in Figure 8-12 (see References 31–34). The Model 45 schematic is similar to the 44 and 48, with some simplifications.

All of these amplifiers used FET inputs, based on a high speed matched NFET pair, Q2. For the 44 and 48, a balanced PNP current mirror loaded the input stage. The mirror output signal drove integrator stage Q6 via a Darlington buffer, Q5. The input stage ran at about 1 mA/side, and the 44/48 had slew rates of 75 V/μs and 110 V/μs, respectively.

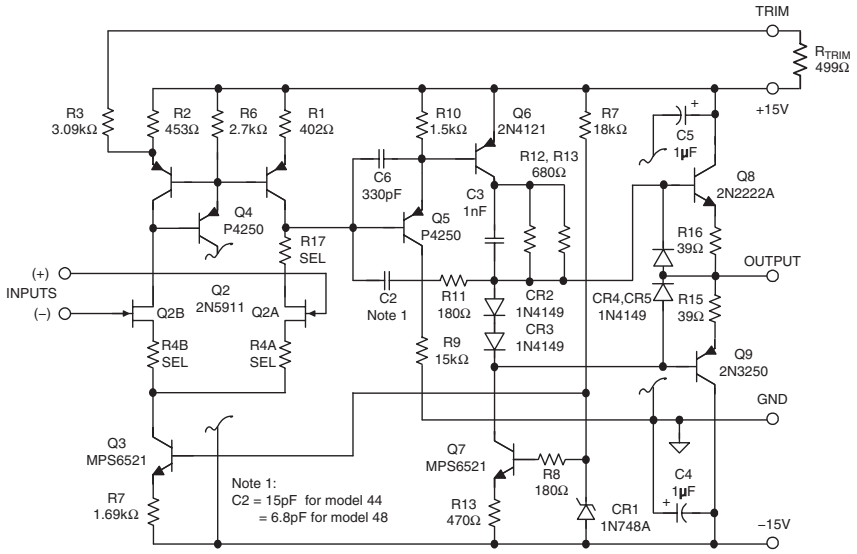


Figure 8-12: The ADI Model 44 and 48 high speed FET-input modular op amps

Like the Model 45, quick settling to a rated error band as low as 0.01% was a key feature of the 44 and 48. These amplifiers achieved 0.01% guaranteed settling of 1000 ns and 500 ns limits respectively, for up to ±10 V of output, in either inverting or noninverting modes.

In addition, these models all had class AB output stages, and were well-suited towards driving coax lines. They used a standard 1.125" square module package, with pinouts as noted. A 499 Ω trim resistor between the trim pin and $+V_S$ provided the rated dc offset without trimming, or, alternately, a 1k Ω pot was used for a more precise trim.

Development of the line continued after Models 44 and 48, and included others in the series, the Model 46, and the 47.

The Model 50 FET Op Amp

The highest speed version of the series came about with the Model 50 modular op amp, which appeared in 1973 (see References 35 and 36). Circuit details of the Model 50 will be more apparent with the discussion of the HOS-050, immediately below.

The HOS-050 FET Op Amp

Prior to being acquired by ADI in 1979, Computer Labs (Greensboro, NC) was in the business of building high speed data acquisition systems. As part of their A/D converter architectures, they routinely used fast op amps to drive the converters, employing amplifiers with characteristics like the Model 50 from ADI.

In 1977 Computer Labs developed a hybrid IC version of the ADI Model 50, calling it the HOS-050 (see Reference 37). An HOS-050 schematic is shown in Figure 8-13.

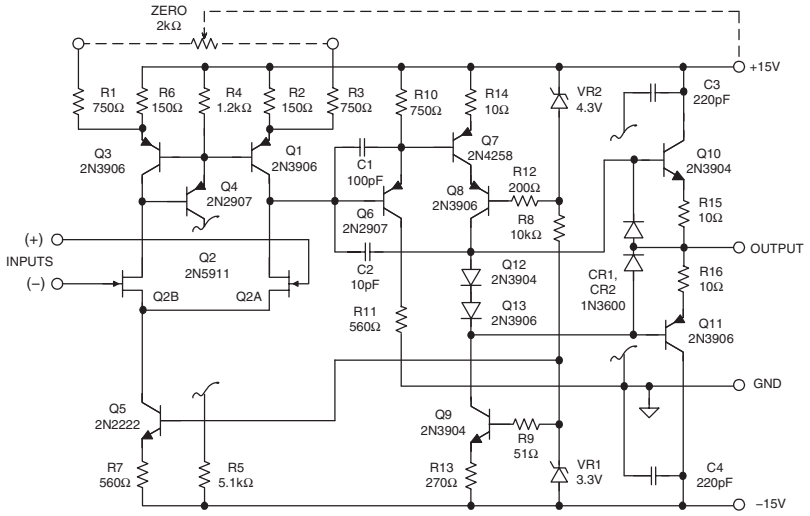


Figure 8-13: The ADI HOS-050 high speed FET-input hybrid op amp schematic

There are many similarities between this and the earlier amplifier shown in Figure 8-12, but the differences are mostly speed-related. As can be noted, the HOS-050 input stage runs at higher current, for higher slew rate and bandwidth. Likewise, the Q7 integrator stage is run at a higher level, and is also cascoded by Q8. The HOS-050 used a balanced form of dc offset trim, which, even if disconnected, allowed the op amp to function well.

The output stage used fast transistors, with a higher threshold level of current limiting. The entire circuit ran on the warm side, dissipating about 600 mW on ±15 V supplies.

The Model 50 and the HOS-050 had rated outputs of ±10 V, and ±100 mA, a 100 MHz bandwidth, and the HOS-050 settled to 0.01% in 200 ns. Both the model 50 and the HOS-050 without doubt achieved the highest levels of performance.

In addition, the HOS-050 represented perhaps one of the more impressive hybrid op amp ICs built at ADI, with its combination of excellent specs, contained within a small TO-8 package. After the acquisition of Computer Labs by ADI, there were two top quality hybrid IC production facilities available to ADI customers. One of these was in the Boston area, with the other at ADI Greensboro, the former Computer Labs site.

There were several other hybrid IC op amps manufactured by ADI in the 1970s and 1980s. Among these were the HOS-060, the ADLH0032, and the AD3554. Hybrid IC construction was the most dense form of circuit packaging available (save for a purely monolithic form of IC). Some appreciation for this high packing density can be gleaned from the photo of the HOS-050 IC op amp in Figure 8-14.

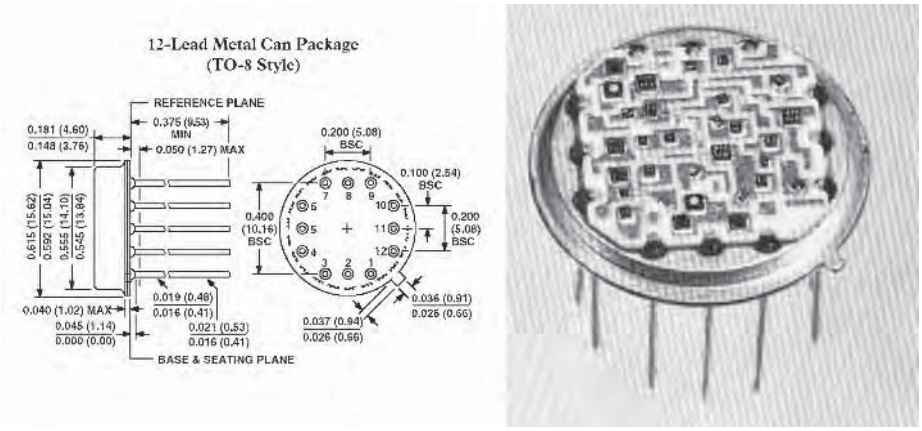


Figure 8-14: The ADI HOS-050 high speed hybrid IC op amp

In this figure, the outline for the hermetically sealed TO-8 package is shown at the left, for size reference. In the right photo of the exposed HOS-050 circuit, it can be noted that virtually 100% of the substrate area is occupied with the conductor traces and the individual circuit components, which included thin film resistors. Further, to maximize circuit area, note that the active substrate area is extended even into the four corners.

While such op amps as the Model 50 and the HOS-050 may have reached pinnacles in terms of the combined circuit performance and their complexity of packaging, this situation didn't last long. Like the fate of modular op amps, hybrid op amp lifetimes were to be relatively short. As soon as IC op amps of comparable electrical performance could be built, the market for the sophisticated but hard-to-produce hybrid ICs shrunk, leaving the hybrids to be sold only into military or other long-lifetime or specialty systems.

References: Solid-state Modular and Hybrid Op Amps

(Note: Appended annotations indicate relevance to op amp history.)

Birth of the Transistor

1. Ian M. Ross, "The Foundation of the Silicon Age," **Bell Labs Technical Journal**, Vol. 2, No. 4, Autumn 1997.
2. C. Mark Melliar-Smith et al, "Key Steps to the Integrated Circuit," **Bell Labs Technical Journal**, Vol. 2, No. 4, Autumn 1997.
3. J. Bardeen, W. H. Brattain, "The Transistor, a Semi-Conductor Triode," **Physical Review**, Vol. 74, No. 2, July 15, 1947 pp. 230–231. *(the invention of the germanium transistor.)*
4. W. Shockley, "The Theory of p-n Junctions in Semiconductors and p-n Junction Transistors," **Bell System Technical Journal**, Vol. 28, No. 4, July 1949, pp. 435–489. *(theory behind the germanium transistor.)*

Birth of the IC

5. J. S. Kilby, "Invention of the Integrated Circuit," **IRE Transactions on Electron Devices**, Vol. ED-23, No. 7, July 1976, pp. 648-654. *(Kilby's IC invention at TI.)*
6. Robert N. Noyce, "Semiconductor Device-and-Lead Structure," **US Patent 2,981,877**, filed July 30, 1959, issued April 25, 1961. *(Noyce's IC invention at Fairchild.)*

The Planar Process

7. Jean A. Hoerni, "Method of Manufacturing Semiconductor Devices," **US Patent 3,025,589**, filed May 1, 1959, issued March 20, 1962. *(the planar process—a manufacturing means of protecting and stabilizing semiconductors.)*
8. Jean Hoerni, "Planar Silicon Diodes and Transistors," **IRE Transactions on Electron Devices**, Vol. 8, March 1961, p. 168 *(technical discussion of planar processed devices).*

Solid-State Modular and Hybrid Op Amp Designs

9. Burr-Brown Applications Staff**, Handbook of Operational Amplifier Applications, First Edition,** Burr-Brown Research Corporation, 1963. *(Burr-Brown's early semiconductor oriented op amp application manual.)*
10. Robert A. Pease, "Design of a Modern High-Performance Operational Amplifier," **GAP/R Lightning Empiricist**, Vol. 11, No. 2, April 1963. *(The designer's description of the P45 op amp. Note—Q8 polarity correction via RAP to WJ email of 5/23/2001.)*
11. **Philbrick Solid-State Operational Amplifiers**, GAP/R bulletin of 3/1/1966.
12. Bob Pease, "Chapter 9, The Story of the P2," within Jim Williams, Ed., **Analog Circuit Design,** Butterworth-Heinemann**,** 1991, ISBN: 0-7506-9166-2.
13. George A. Philbrick, "Electronic Amplifier," **US Patent 3,405,366**, filed June 30, 1965, issued Oct. 8, 1968. *(A varactor bridge amplifier.)*
14. H. M. Paynter, "In Memoriam: George A. Philbrick," **ASME Journal of Systems, Measurement and Control**, June 1975, pp. 213–215.
15. Dan Sheingold, "Analog Dialectic," **Analog Dialogue**, Vol. 30, No. 3, p. 1.
16. Ray Stata, "Operational Amplifiers, Parts I and II," **Electromechanical Design**, September and November, 1965. *(The first ADI op amp application manual.)*

17. Data sheet for **Model 310, 311 Ultra Low Bias Current Varactor Bridge Operational Amplifiers**, Analog Devices, Inc., December 1969.
18. Lewis R. Smith, "Operational Amplifier with Varactor Bridge Input Circuit," **US Patent 3,530,390**, filed Dec. 28, 1966, issued Sept. 22, 1970. *(A varactor bridge amplifier.)*
19. **ADI Modular Products**, www.intronics.com/products/analogproducts**/.**
20. **Capsule Listing of Analog Devices Op Amps**, ADI bulletin of April 1968.
21. **Selection Handbook and Catalog Guide to Operational Amplifiers**, ADI catalog of January 1969.
22. Ray Stata, "Applications Manual 201, 202, 203 & 210 Chopper Stabilized Operational Amplifiers," ADI application note, 1967. *(Use of 200 series modular chopper amplifiers.)*
23. ADI Staff, "Circuit Advantages of Chopper Stabilized Operational Amplifiers," ADI application note, September 1970. *(Operation and use of inverting-type modular chopper stabilized op amps.)*
24. Peter Zicko, "Designing with Chopper Stabilized Operational Amplifiers," ADI application note, September 1970. *(Operation and use of noninverting-type modular chopper stabilized op amps.)*
25. Richard S. Burwen, "Input Current Compensation with Temperature for Differential Transistor Amplifier," **US Patent 3,467,908**, filed Feb. 7, 1968, issued Sept. 16, 1969. *(A method of compensating for bias current in a differential pair amplifier.)*
26. **Analog Dialogue**, Vol. 1, No. 1, April 1967. *(The premier issue of **Analog Dialogue—**'A Journal for the Exchange of Operational Amplifier Technology'.)*
27. Ray Stata, "Operational Integrators," **Analog Dialogue**, Vol. 1, No. 1, April, 1967. *(Reprinted as ADI AN357.)*
28. Ray Stata, "User's Guide to Applying and Measuring Operational Amplifier Specifications," **Analog Dialogue**, Vol. 1, No. 3. *(Reprinted as ADI AN356.)*
29. **Analog Dialogue**, Vol. 3, No. 1, March 1969. *(The first issue of **Analog Dialogue** under the editorial guidance of Dan Sheingold.)*
30. Data sheet for **Model 45 Fast Settling FET Operational Amplifier**, Analog Devices, Inc., May, 1970.
31. "New Modular Op Amps," **Analog Dialogue**, Vol. 5, No. 2, pp. 12 *(Model 43 and 44 op amps).*
32. "Op Amp Settles to 0.01% in 300 ns," **Analog Dialogue**, Vol. 6, No. 2, pp. 11 *(Model 48 op amp).*
33. Data sheet for **Model 48 Fast Settling Differential FET Op Amp**, Analog Devices, Inc., June 1972.
34. Data sheet for **Model 44 Fast Settling High Accuracy Op Amp**, Analog Devices, Inc., August 1972.
35. Data sheet for **Model 50 Fast Settling 100 mA Output Differential FET Op Amp**, Analog Devices, Inc., May 1973.
36. "Model 50: Wideband, Fast Settling Op Amp," **Analog Dialogue***,* Vol. 7, No. 2, pp. 13. *(The Model 50* modular *op amp.)*
37. Low-Cost HOS-050C is Internally Compensated, Settles to 0.1% in 80 ns, 0.01% in 200 ns," **Analog Dialogue***,* Vol. 16, No. 2, p. 24. *(The HOS-050C* hybrid *op amp, first introduced by Computer Labs in 1977.)*

This page intentionally left blank

SECTION 8-4

IC Op Amps

Birth of the Monolithic IC Op Amp

The first generally recognized monolithic IC op amp was from Fairchild Semiconductor Corporation (FSC), the µ*A702*. The µA702 was designed by a young engineer, Robert J. (Bob) Widlar. As will be seen, Bob Widlar was a man who was shortly to make an indelible mark on the IC world. But, his 1963 µA702 didn't exactly take the world by storm. It wasn't well received, due to quirky characteristics—odd supply voltages, low input/output swings, low gain, and so forth. Nevertheless, and despite these shortcomings, the µA702 established some important IC design trends. As pioneered by Bob Widlar, these concepts were to carry over to future op amps (see Reference 1). In fact, they are standard linear IC design concepts today. While the µA702 isn't covered in detail here, information on it can be found in Reference 2.

The µA709

Not long after the µA702 a major IC op amp landmark came about, specifically the introduction of another Bob Widlar op amp for Fairchild in 1965, the µ*A709,* (see Reference 3). The 709[1] improved markedly on the 702; it had higher gain (45,000 or ~94 dB), greater input/output ranges (±10 V), lower input current (200 nA) and higher output current, and operated from symmetrical power supplies (±15 V). The 709 quickly became a standard, and was produced for decades. Figure 8-15 is a 709 schematic.

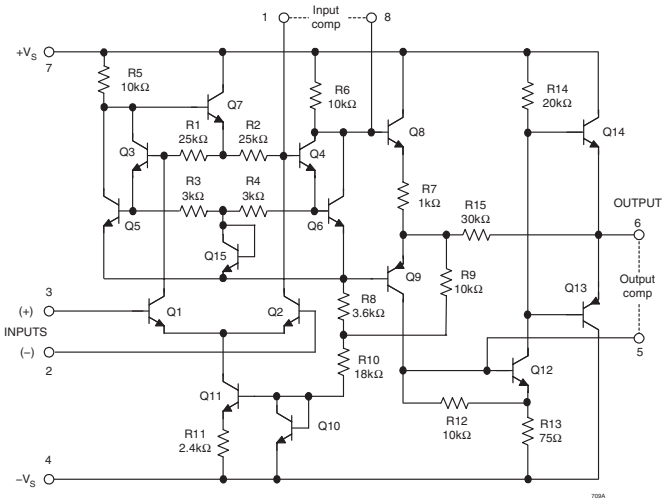


Figure 8-15: The µA709 monolithic IC op amp

[1] Although the original Fairchild designation was "µA709," the design was broadly second-sourced. The widely-used generic name became simply "709." Likewise, the µA702 is known as the "702."

So universal was the 709 that it can be regarded as an IC op amp classic. Although the individual specifications were surpassed by many subsequent designs, the 709 remains a milestone, as the first widely used monolithic IC op amp.

Many design principles from the 702 were used again in the 709, such as the use of matched transistors, for the first and second stages, and the logarithmic biased (delta-V_{BE}) current source, Q10–Q11. There were also new wrinkles added. Because the 709 used what was basically an NPN IC process, Widlar resorted to some clever tricks to create PNP functions. He used a modified NPN structure for two PNPs, the level shifter Q9 and the output PNP, Q13. The output stage operated class-B, with no Q13–Q14 bias. Local feedback around this stage via R15 minimized deadzone.

Frequency compensation for the 709 was achieved with two RC networks, between pins 1–8, and pins 6–5. The associated network values could be changed for optimum ac response, using four networks for gains of 0 dB to 60 dB.

Although the 709 was a vast improvement over the 702, it still had quirks of its own, and these gave rise to application problems. For example, without some user-added series resistance, the output stage could blow out for sustained shorts. Many saw the frequency compensation scheme as difficult, plus it took up board space. Also, the 709 could latch up whenever the input CM voltage rose high enough to saturate the input stage. And, excessive differential input voltages could blow out the input transistors. Although savvy users could work around these 709 application quirks, it sometimes took extra parts to do it. So, in one sense the above use-related issues served as a general lesson towards the necessity of bullet-proofing an IC op amp against various application stresses.

The LM101

Not content to rest on his 702 and 709 laurels, Bob Widlar moved on to another company, National Semiconductor Corporation (NSC). His next IC op amp design, the *LM101*, was introduced in 1967 (see Reference 4). This began a second IC op amp generation (the 709 is generally regarded as the first generation of IC op amps).

The LM101 family[1] used a simpler two-stage topology, one that addressed the application problems of the 709. It was also an op amp design that influenced a great many ones to follow. A simplified circuit of the 101 is shown in Figure 8-16.

The LM101 design objectives were to eliminate such 709 problems as:

- No short-circuit protection.
- Complex frequency compensation.
- Latchup with high CM inputs.
- Sensitivity to excessive differential input voltage.
- Excessive power dissipation and limited power supply range.
- Sensitivity to capacitive loads.

For the same reasons that the 709 has historical importance, so does the LM101, as it represents the next op amp technology level. In fact, the all-purpose topology used is the basis for a range of many other general-purpose devices, variants of the LM101 design.

[1] The LM101 family included three temperature ranges, LM101, LM201, and LM301, for military, industrial, and commercial ranges, respectively. Also known generically as 101, and so forth. Similarly, the following LM101A series devices became know as 101A, 201A, 301A, and so forth.

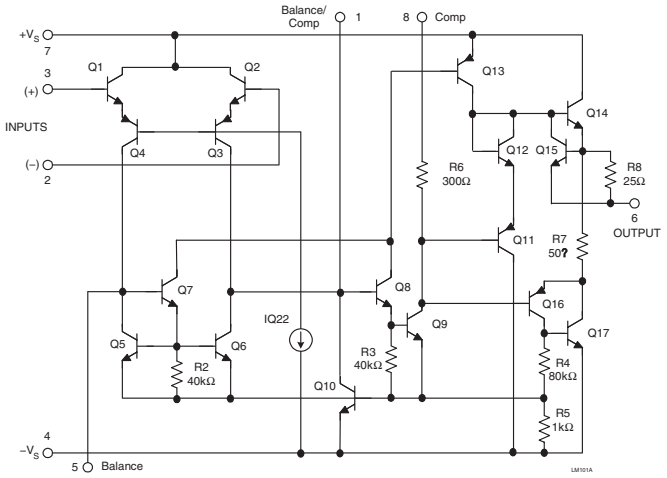


Figure 8-16: The LM101 monolithic IC op amp

The new 101 design did solve the 709's problems, and it added some further refinements. Gain was 160,000 (~104 dB), and the useful supply range increased from ±5 V to ±20 V. For easy upgrading, the 101 used the same pins as 709 for inputs, output, and power.

A major goal of the 101 design was simpler frequency compensation. To enable this, the 101 uses a *two-stage* amplifier design, as fewer stages are easier to compensate. But, to retain high voltage gain, the two stages needed the gain of the three 709 stages. In the 101, the high gain per stage is done using active loads, which increase the available gain per stage to a maximum. An example is Q13, which provides the collector load for Q9.

In the first stage of the 101, active loading is also used, Q5–Q6. Q1–Q4 and Q2–Q3 here form an equivalent PNP differential pair. Although the PNPs have low gains, they are buffered by high-gain NPNs, Q1–Q2. The net resulting input current was 120 nA.

Note that the CM input range of this stage is quite high, as Q1–Q2 can swing positive to $+V_S$. The negative CM limit is about four V_{BE} above the $-V_S$ rail. This wide CM range prevents input stage saturation and latch-up. Another feature of this composite input stage is a very high differential voltage rating, due to the PNP high base-emitter breakdowns. The input stage can safely tolerate inputs of ±30 V.

The second stage of the 101 is the common-emitter amplifier, Q9. With the above mentioned loading of Q13, this stage achieved a voltage gain of about 60 dB, and the overall gain of the op amp was typically over 100 dB. A class AB output stage is used, consisting of NPN Q14, and the equivalent PNP, Q16–Q17. These transistors were biased by Q11–Q12. Sensing resistors R7, R8, and Q15, along with an elaborate loop comprising Q16 and Q9–Q10, provided current limiting.

An important differentiation of the 101 versus the 709 was the much simpler frequency compensation. In the 101, this was accomplished by a single external 30 pF capacitor, connected between pins 1 and 8. As can be noted from the 101 internal connections, this capacitor makes the second gain stage Q9 an integrator, forcing overall gain to roll off from its maximum value of 104 dB at 10 Hz at a rate of 6 dB per octave, crossing unity gain at about 1 MHz. This compensation made a 101 device stable in any feedback configuration, down to the unity gain.

Viewed analytically, the 101 op amp topology can be seen as a two-stage voltage amplifier, formed by an input g_m stage consisting of Q1–Q6, which drives an integrator stage Q9 and the compensation capacitor, and a unity gain output buffer, Q11–Q17. This type of topology is discussed further in Chapter 1 of this book.

But, a salient point to be noted is the fact that this form of compensation takes advantage of *pole splitting* in the second stage, which results in the multiplied capacitance of the compensation capacitor to provide a stable –6 dB/octave roll-off (see Reference 5). This was a critically important point at the time, as it allowed a single small (30 pF) capacitor to provide the entire compensation. Many two-stage IC op amp architectures introduced since the original 101 use a similar signal path and compensation method.

The µA741

In less than a year's time after the 101's introduction, Fairchild introduced their answer to it, which was the µ*A741* op amp. Designed by Dave Fullagar and introduced in 1968, the µA741 used a similar signal path to the LM101 (see Reference 6). A simplified schematic of the µA741 is shown in Figure 8-17.

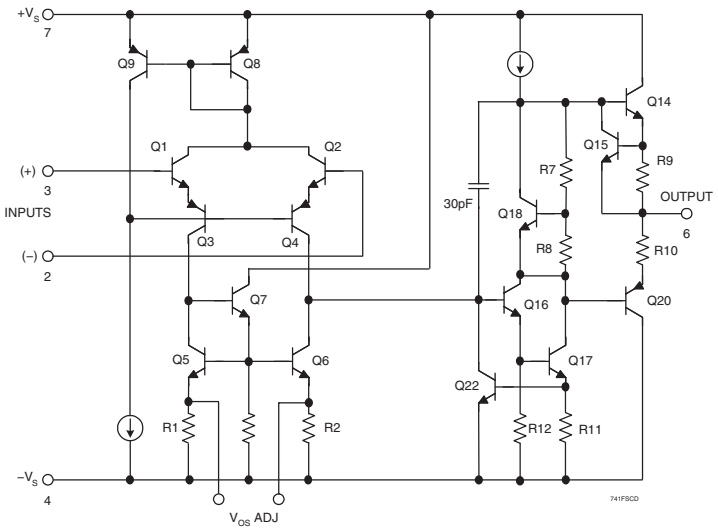


Figure 8-17: The µA741 monolithic IC op amp

Although there are obvious biasing differences, the 741 signal path is essentially equivalent to the 101, and it provides similar features in terms of short-circuit and input over voltage protection, and has a comparable bandwidth. Nevertheless, for the reason that the 741 had the 30 pF compensation capacitor *on the chip*, it became the standard.[2]

[2] George Erdi told an interesting story of the µA741's genesis while working at Fairchild and sharing an office with the designer, Dave Fullagar. It seems that shortly after the LM101 appeared, the two were discussing the reason why the required compensation cap was external. Fullagar's conclusion was that the National process in use at the time simply couldn't accommodate the internal capacitor. He said, "*Well, we can do that!*" and so, shortly afterwards, the internally compensated µA741 was born.

The moral here seems to be that ease-of-use is more valuable to users than flexibility. The 101, with the user-added capacitor, was functionally equivalent to the 741. In fact, National Semiconductor had introduced the *LH101*, a hybrid package of an LM101 chip plus a 30 pF capacitor, in early 1968. Nevertheless, the 741 became a greater standard.

The LM101A

Bob Widlar updated his basic LM101 design with the *LM101A*, which was introduced by National Semiconductor in late 1968. This was a more refined version of the 101 op amp architecture, featuring lower and more stable input bias current (see Reference 7).

At about the same time, they also introduced the *LM107*, which was an LM101A with the 30 pF compensation capacitor on the same monolithic chip. The 107 and 741 could be said to be comparable for ac specifications, but the 107 had an edge for dc parameters.

The µA748

The µ*A748*, an externally compensated derivative of the µA741, was introduced by Fairchild in 1969. It was Fairchild's answer to the National LM101/LM101A series. The 748 functioned just like the 101/101A types, with an external capacitor between pins 1–8.

Multiple 741 Types, General-Purpose Single-Supply Types

With the 741 being such a popular device, it readily lent itself to dual and quad versions. Space doesn't permit discussion of all, but among the more popular were the Motorola *MC1558/1458*, a pair of 741s in an 8-pin DIP pinout. Almost since the beginning dual versions have been the more popular for IC op amps. Quad 741 types also became available, such as the Motorola *MC4741*, and the National Semiconductor *LM148*.

In 1972, Russell and Frederiksen of National Semiconductor introduced an amplifier technique suitable for operation in a single-supply environment at low voltages (see Reference 8). This amplifier, which was to become the *LM324*, became the low cost industry standard general=purpose quad op amp. It was followed by a similar dual, the *LM358*. One of the key concepts used in the paper was an input stage g^m reduction method, credited to James Solomon (Reference 5).

Since this is a historical discussion of IC op amps, one would assume that all of the above general-purpose IC op amps would have long since disappeared, being 30-odd years old. But such isn't the case—many of them are still available even now, in 2004!

The AD741—A Precision 741

Neither the 741 nor the 101A were designed as true high precision amplifiers. In the years following the development of the 741 and 101A op amps, other IC manufacturers looked into refining the performance of these popular products for the precision analog marketplace. In 1971 ADI took a key step towards this, and acquired Nova Devices of Wilmington, MA. This added both technology and design capability to the ADI portfolio, which was to be immediately useful for the manufacture of linear ICs.

One of the first ADI ICs to be produced was an enhanced design 741 type op amp, the *AD741* (see Reference 9). A schematic of this circuit is shown in Figure 8-18.

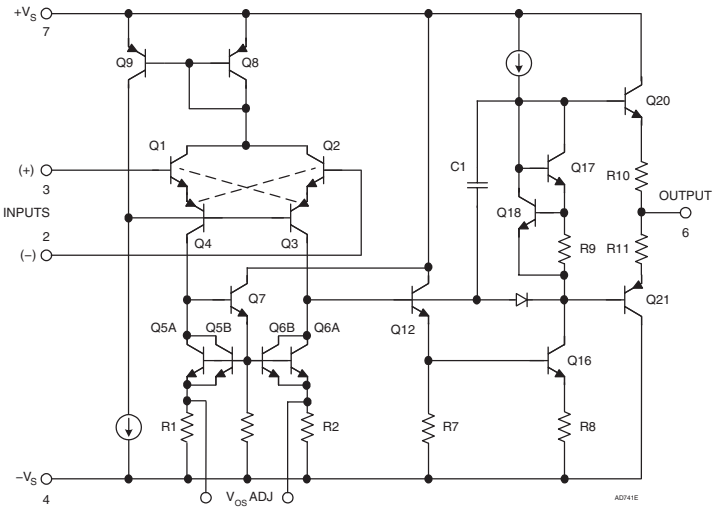


Figure 8-18: The AD741 monolithic IC op amp

Although this circuit looks deceptively like the µA741 of Figure 8-17, it should be understood that there are many subtleties affecting IC performance that don't necessarily appear on the data sheet. In this case, some key differences include a thermally balanced layout, evident from the use of a cross-quad input stage (denoted by the Q1–Q4 cross markings), and the quad operation of the current mirror load transistors, Q5–Q6. In addition, a better output stage was used, with higher efficiency transistors.

The premium version of this design was the AD741L, which achieved an offset of 500 µV (max), a drift of 5 µV/°C (max), a bias current of 50 nA (max), and a minimum gain of 50,000 (94 dB) into a 2 kΩ load. ADI also produced an improved 301A type amplifier, the AD301AL, with dc specifications similar to those of the AD741L above.

In 1973, the AD741L sold for $6.00 in 100 piece lots, while the AD741J could be purchased for just $1.25 in the same quantities.

With the establishment of general-purpose IC op amps a fact, other designers began to focus on greater precision. This was sought through the reduction of various errors; lower bias currents, lower offset voltage, higher gain, and so forth. A couple of the development paths that follow the general thread of higher IC op amp precision will now be discussed.[3]

SuperBeta IC Op Amps—LM108 to OP97

After his release of the 101 op amp, Bob Widlar began to explore the *superbeta* bipolar transistor technique.[4] A superbeta transistor is one subjected to extra diffusion steps, to raise the forward gain from a typical 200, to several thousand or more. Used in the input stage of an IC op amp, a pair of superbeta transistors can potentially reduce input currents by a factor of 10–20 times.

[3] For coherence, this superbeta precision op amp (and other) threads will be presented in a continuous fashion. In actual time of course, each thread paralleled many other concurrent IC op amp developments.

[4] To avoid confusion, the term "superbeta" should really be "super-H_{FE}"—but "superbeta" has stuck.

However, the use of superbeta transistors isn't exactly straightforward, because the super-beta process reduces the breakdown voltage to 5 V or less. This factor requires extra circuitry around the superbeta devices to buffer high voltages normal to an op amp.

The first IC to use super-beta transistors was the LM102 voltage follower of 1967, by Bob Widlar (see Reference 10), followed by the upgraded LM110 in 1970. Widlar also published a more general description of superbeta transistor operation, in Reference 11.

The 102 and 110 voltage follower ICs were somewhat specialized parts. Internally configured as unity-gain buffers, there was no user configuration needed (or possible). Nevertheless, the use of the superbeta devices at the input established their viability, at least in one context of application.

Meanwhile, in these very early years of the technology, Bob Widlar wasn't the only designer working on superbeta concepts as applied to op amps. At Motorola Semiconductor, Solomon, Davis, and Lee developed the *MC1556* op amp, reporting on it in early 1969 (see Reference 12).[5]

This two-stage op amp design used a combination super-beta NPN pair, combined with a PNP pair as the input stage. With a quoted super-beta transistor gain of 4,000, the design had a 2 nA input current. It was also known for a slew rate appreciably higher than the 741 or other devices available at the time.

In late 1969, Bob Widlar contributed another IC op amp design, the *LM108* (see Reference 13). The LM108 was the first of what turn out to be a long line of precision IC op amps with low input currents, by virtue of a super-beta input transistor front end. A simplified schematic of the LM108 is shown in Figure 8-19.

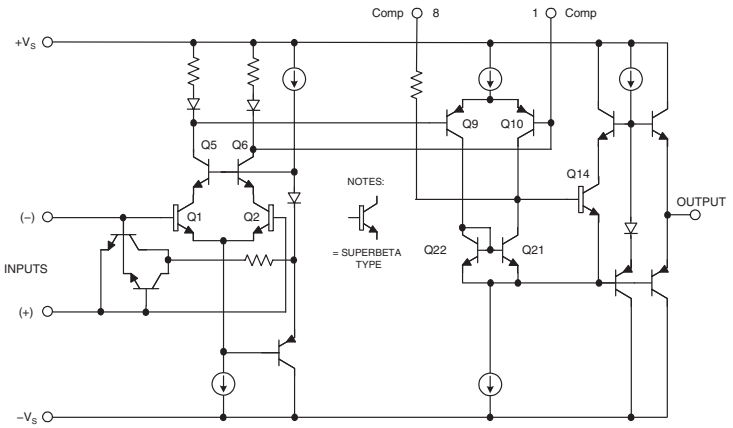


Figure 8-19: The LM108 superbeta input monolithic IC op amp

In this circuit the superbeta NPN devices are indicated by a wider base in the symbol, and the remaining transistors are high voltage types. Q1–Q2 make up the super-beta input differential pair, and are cascoded by Q5–Q6. The diode drops biasing this cascode are arranged so that Q1–Q2 see a 0 V V_{CE}. The second stage on the 108 is a PNP differential pair, Q9–Q10, with a balanced load, Q21–Q22. The output voltage is developed at the emitter of Q14, and buffered by a class AB output stage.

[5] Ironically, the 1556 op amp may not have gotten all the credit due, as perhaps the earliest use of super-beta devices, within a general-purpose op amp. A second irony is that the paper itself is better known (and often quoted) for the establishment of input stage g_m reduction as a means of raising slew rate.

The 108 design achieved a notably low bias current, typically under 1 nA at room temperature. Offset voltage was typically 700 µV and 2 mV (max), and gain was 300,000 (or 110 dB). It had very wide input and output ranges, typically ±14 V operating from ±15 V supplies, and it consumed 300 µA of quiescent current. Further, it could operate down to supplies of ±2 V, making it useful on 5 V rails. A point worth noting here is that the 108 differed from Widlar's previous LM101/101A designs with a load rating of 10 kΩ (whereas the 101/101A could drive 2 kΩ at rated gain). This was obviously a byproduct of the low power nature of the 108 design.

The basic LM108 design was later upgraded by National, to the *LM108A*. This was a 500 µV(max) offset voltage version of the part. An internally compensated version was also offered, the *LM112*.

Later, many other companies brought out their own competitive versions of the 108 and 112 op amps, with similar sounding names, and some with much improved performance. In the 1970s, ADI was one such company, offering the AD108 and AD108A, with specifications like the originals.

In 1969 Marv Rudin and Garth Wilson formed Precision Monolithics Incorporated (PMI), a brand new company with a charter of precision linear ICs. PMI introduced their counter to the 108A, the *OP08*, in 1976. This wasn't simply a second source to the 108A, but a revised and upgraded design by George Erdi and Larry Farnsley. Erdi was known as the father of the Fairchild µA725 (and the SSS725, at PMI). Erdi came to PMI in 1969, from Fairchild, where he had already established some key op amp design concepts (see narrative on 725 to OP07).

The new OP08 design added a thermally balanced layout, to reduce offset voltage and to increase gain. This was reflected in an offset voltage of 150 µV (max) for the best grade, a minimum gain spec of 50,000 (94 dB) into a 2 kΩ load (other specs were comparable to the 108A). At the same time the PMI *OP12* was introduced. This was a device similar to the OP08, but with internal compensation, and one which competed with the 112.

Another IC company to introduce 108/112 style designs was Linear Technology Corporation (LTC). Formed in 1981 by former National and Precision Monolithics engineers, Linear Technology introduced their own superbeta op amps, the *LT1008* and *LT1012* in 1983 (see Reference 14). Designed by a team headed by former PMI op amp designer George Erdi, the LT1008 featured trimmed offset voltage of 120 µV (max), a drift of 1.5 µV/°C (max), and a minimum gain of 120,000 (~102 dB) driving 2 kΩ. A notable feature of these amplifiers versus the earlier 108A types was the use of *input bias current cancellation*, allowing an LT1008 bias current as low as ±100 pA(max).

Precision Monolithics followed up on the OP08 and OP12 designs with the *PM1008* and *PM1012*, released in 1987. These were designed by Peter Gaussen of the Twickenham UK design center. The PM1008 had specs comparable to the LT1008, and the PM1012, to the LT1012. Also in 1987, the performance bar was raised a bit higher by the introduction of the even more tightly specified PMI *OP97*, an internally compensated super-beta input op amp functionally like the 112 or 1012. A simplified schematic of the OP97 family is shown in Figure 8-20.

The OP97 best grade (A, E) offers an offset voltage of 25 µV (max), a drift of 0.6 µV/°C (max), a bias current of ±100 pA (max), and a minimum gain of 200,000 (106 dB) driving a 2 kΩ load. It is notable that the OP97 was marketed as a "low power OP07," which of course technically speaking it isn't.[6] The OP97 uses a two-stage topology, the OP07 a three-stage. Not at all the same inside—but to many users, lower power with precision can be very important, rendering the internal differences moot.

[6] Former PMI and ADI op amp product line director Jerry Zis relates that while the OP97 may have been marketed with a focus on the OP07 users looking for a lower power device, this niche was nevertheless a real need. Of course, it also helps to have great specs, plus a family of dual and quad devices, which the standard OP07 never did have—but which the OP97/OP297/OP497 family eventually provided.

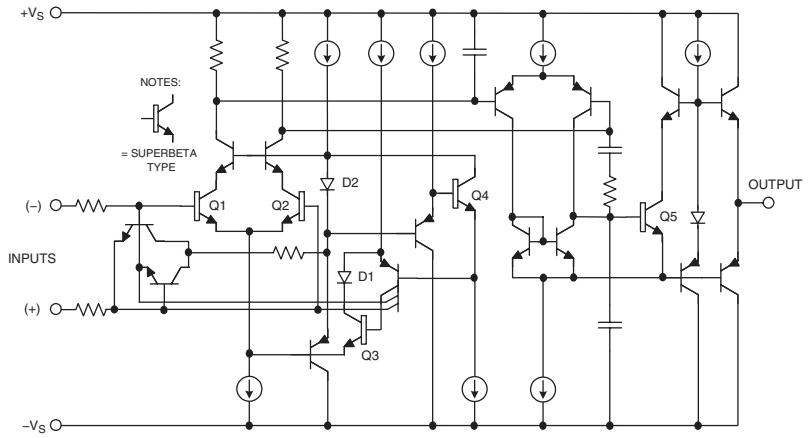


Figure 8-20: The OP97/OP297/OP497 super-beta input monolithic IC op amp

The OP97 is still available today, as are the other dual and quad family members, the OP297 (dual) and OP497 (quad) devices. The latter devices were designed by Derek Bowers, adding laser trimming (as opposed to the use of zener-zap trim on earlier family devices), and were released in 1990 and 1991.

The AD508 and AD517

ADI entered the super-beta op amp game at an early point, with their own super-beta input part, the *AD508*, an externally compensated precision device (see Reference 15). Designed by Modesto "Mitch" Maidique who came to ADI from Nova Devices, the AD508 released in 1972. It was an upgrade of his 1971 ADI precision op amp design, the *AD504*, which was a very high precision op amp in its own right (see Reference 16).

Quite unlike the 108 series of op amps topologically, the AD508 could be said to be an inherently high precision design. It featured the use of thin-film resistors, a super-beta input stage with balanced active loading, and a thermally balanced layout. The design used a two-stage double-integrator topology, with a triple buffered output, for very high load and thermal immunity. The AD508K typically achieved an open-loop gain of ~138 dB while driving 2 kΩ (much higher than any 108 or 112 topology amplifier), a bias current under 10 nA, and a low drift of 0.5 μV/°C (max) (see Reference 17).

An internally compensated version of the AD508 was introduced in 1978, the *AD517* (see Reference 18). This amplifier also used a superbeta input stage, and added the important feature of laser wafer trimming (see Reference 19). This trimming allowed offset voltage to be held as low as 25 μV (max), and drift as low as 0.5 μV/°C (max), both for the highest grade, the AD517L.

Much later on, ADI also introduced its own series of internally compensated super-beta op amps, styled along the lines of the OP97 series of devices. These were the AD705 (single), AD706 (dual) and AD704 (quad) series of op amps (see References 20–22). Designed by Reed Snyder, these op amps were introduced in 1990 and 1991.

Precision Monolithics was purchased by ADI in 1990, and the op amp product lines of the two companies were merged. Today, the product catalog of ADI includes many ADI originated (ADxxx) as well as many original PMI products (OPxxx).

Precision Bipolar IC Op Amps—μA725 to the OP07 Families

A second thread of development for precision op amps started at roughly the same time as the LM108 design, in 1969. Working then for Fairchild Semiconductor, George Erdi developed the μ*A725*, the first IC op amp to be designed from the ground up with very high precision in mind.

In a rather complete technical paper on the 725 circuit and precision op amp design in general, Erdi laid down some rules that have become gospel in many terms (see Reference 23). A simplified schematic of the 725 is shown in Figure 8-21.

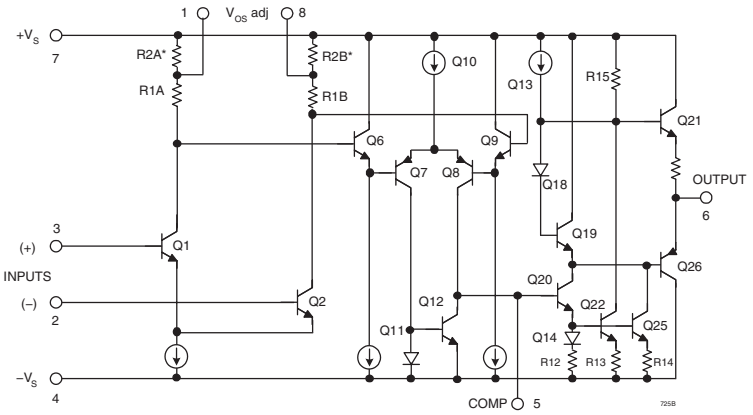


Figure 8-21: The μA725 monolithic IC op amp

The 725 is basically a three-stage design, consisting of a differential NPN input pair Q1– Q2, followed by a second differential stage, Q7–Q8, and a final single-ended output stage Q22, which is buffered by class AB emitter followers Q21 and Q26. The circuit was externally compensated by a four-component RC network at Pin 5. The three stages yielded much higher gain than previous two-stage amplifiers, but at the expense of more complex compensation.

Optional trimming of input offset voltage took place at pins 1–8, where an external 100 kΩ pot with the wiper to $+V_S$ was adjusted for lowest offset. When done in this manner, this also gave lowest drift.

Some circuit subtleties are belied by the schematic's simplicity, but yet important. Q1 and Q2 are actually a quad set (dual pairs), with the paralleled pairs straddling the chip's axis of thermal symmetry. The idea behind this was that thermal changes due to output stage dissipation would be seen as equal thermally-induced offsets by the two input stage halves, and thus be rejected. This principle, first established in the 725 design, has since become a basic precision design principle (see Reference 15, and within Reference 23, the Figure 2 chip photograph).

Another key point of 725 performance optimization concerns offset nulling for a condition of zero input offset and lowest drift, described in some detail by Erdi within References 23 and 24. The 725 had a typical offset voltage spec of 600 μV, and with the offset nulled as recommended, the resulting drift was 0.6 μV/°C. The bias current was typically 45 nA, and open-loop gain was 132 dB.

George Erdi left Fairchild in 1969, to join the newly formed PMI. At PMI, he continued with the 725 precision amplifier concept, designing the SSS725 version.[7] This op amp was identical to the original in functionality, but offered improved performance. There was also an OP06 produced at PMI later on. The OP06 was like the 725, but with the addition of differential input protection.

Not too long after the SS725 at PMI came the *OP05* op amp, in 1972 (see Reference 25). With the new OP05 design George Erdi considerably simplified application of precision op amps, making it internally compensated, adding input bias current cancellation, and differential overvoltage protection. Topologically, with these enhancements the OP05 can be said to be identical to the 725's three-stage architecture.

Precision op amp users now had a simple-to-apply device. A major system error was still left to the user to deal with: offset voltage. The OP05 used a manual trimming scheme similar to the 725 for offset adjustment, via a 20 kΩ pot. The unadjusted maximum offset for the OP05 was 500 µV, and drift was 0.6 µV/°C after null.

The OP05 was successful in its own right, but the offset voltage issue was still there. About this time, other IC companies were turning to active wafer trim schemes, such as the aforementioned ADI laser wafer trimming scheme (Reference 19). The next phase of 725 and OP05 evolution was to address active trimming of op amp offset, to deliver higher accuracy in the finished op amp device.

In 1975, Erdi reported on an offset trim technique that used 300 mA over-current pulses, to progressively short zener diodes in a string. With the zener string arranged strategically in the input stage load resistances of an op amp, this so-called "zener-zapping" could be used to trim the offset of an op amp on the wafer (see Reference 26). The first op amp to utilize this new trim technique was Erdi's *OP07*, which was introduced by PMI in 1975 (see Reference 27).

In the OP07, shown in simplified schematic form in Figure 8-22, the (not shown) zener strings are connected in parallel with segmented load resistances R2A and R2B. A simplified schematic of the scheme is shown in Reference 27, Figure 3, but in essence the series of zener diodes parallel the segmented partial load resistances, the values of which are sized to control progressively larger offsets.

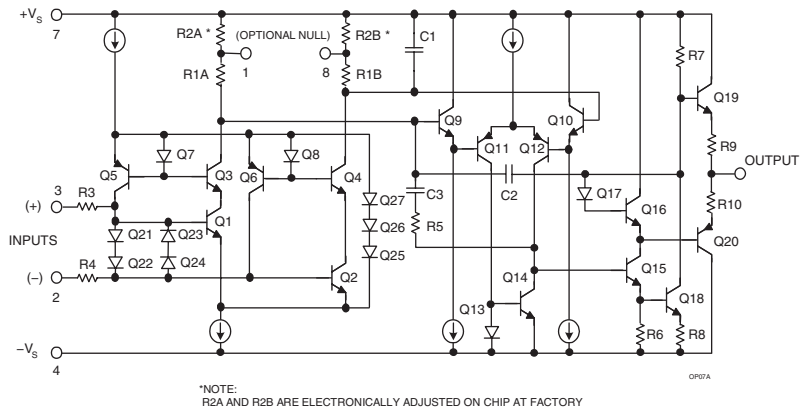


Figure 8-22: The OP07 monolithic IC op amp

[7] The "SSS" prefix was used on early PMI amplifiers, and stood for Superior Second Source. Another example was the PMI SSS741.

At trim time, a computer measures the actual op amp offset, then selects the appropriate zener to reduce it to the next level, and then zaps that zener with a high pulse of current.

This current pulse effectively shorts the zener, and so the section of load resistance in parallel. This process is iterated until the offset cannot be further reduced.

The new OP07 thus created had some impressive offset specifications. It was reported that the entire distribution of parts trimmed had offsets of 150 µV or less, and a prime grade, the OP07A was specified at 25 µV (max) for offset. Importantly, since this trim method also simultaneously reduced drift as the offset is nulled, the trimmed OP07 amplifiers had drift rates of 0.6 µV/°C (max), and typically much less than this.

The zener-zap trim technique was a valuable innovation in its own right, as it could be applied to other devices to reduce errors, and at a low additional cost to the manufacturing process. It is today one of many active trim techniques used with precision op amps (see the more detailed discussions of trimming in Chapter 1).

The OP07 went on to become the "741" of precision op amps, that is the standard device of its precision class. It was (and still is) widely second-sourced, and many spin-off devices followed it in time.

PMI went forward with the OP07 op amp evolution, and introduced the OP77, a higher open-loop gain version of the OP07 in 1988. The best grade OP77A featured a typical gain of ~142 dB, an offset of 25 µV, and a drift of 0.3 µV/°C (max). Later, an additional device was added to the roster, the OP177. This part offered similar performance to the OP77A, as the OP177F, specified over the industrial temperature range.

Prior to the 1990 acquisition of PMI by ADI, the ADI designers turned out some excellent OP07 type amplifiers in their own right. Designed by Moshe Gerstenhaber, the AD707 essentially matched the OP77 and OP177 spec-for-spec, operating over commercial and industrial ranges (see Reference 28). It was introduced in 1988. The AD708 dual was also offered in 1989, providing basically the performance of two AD707s. Moshe Gerstenhaber also designed the AD708 (see Reference 29).

The OP27 and OP37

As noted above, the OP07 lineage also included other related devices. Two such op amps, also designed by George Erdi at PMI, were the OP27 and OP37. These devices were released in 1980 (see References 30 and 31). Figure 8-23 is a simplified schematic of the OP27 and OP37 op amps.

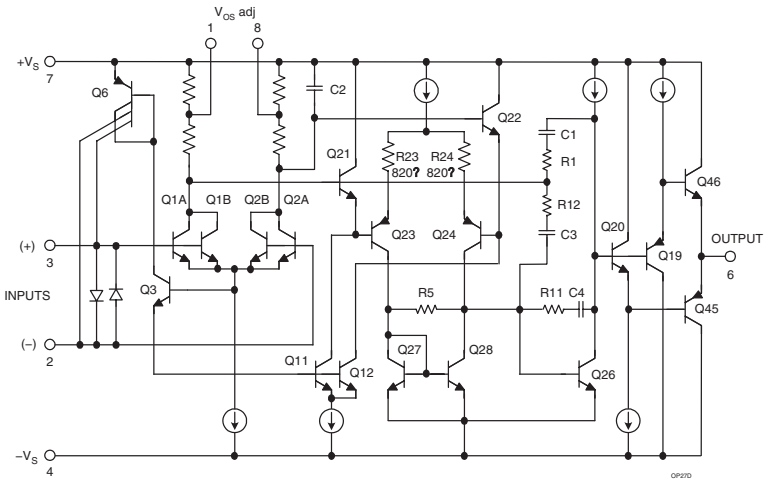


Figure 8-23: The OP27 and OP37 monolithic IC op amps

From the apparent similarity to the OP07 schematic of Figure 8-22, it might be easy to conclude that this amplifier was an adaptation of the OP07. However, the similarity ends in the fact that they are both three-stage amplifiers, and in truth the two different designs have been optimized with different end applications in mind.

In the design process of OP27/37, an examination of various noise sources was done, and the three-stage architecture is biased with the goal of both lower input noise, and higher speed (see Reference 31). Thus the stage operating currents are higher vis-à-vis the OP07, and provision for a decompensated version was also done (the OP37, stable at a gain of five). This was achieved by making the compensation cap C1 smaller on the OP37 version, while the basic OP27 is stable at unity gain. Towards the lower input noise, the current-limit protection resistors in series with the inputs were also removed.

The OP27 did achieve the goals of lower noise and greater speed, with an input noise density of 3.0 $nV/\sqrt{Hz}$ at 1 kHz, a 1/f corner of 2.7 Hz, while the slew rate was 2.8 V/µs and unity gain-bandwidth was 8 MHz. While realizing these new ac performance levels, the OP27/OP37 also retained impressive dc specifications as well. With a zener-zapped trim to the first stage, the offset was 25 µV (max), drift was 0.6 µV/°C (max), and voltage gain was typically 126 dB. The OP27 and OP37 went on to become widely second-sourced, and became standard devices for use as low noise, high dc precision amplifiers.

Single-Supply and Micropackaged OP07 Compatibles

It would be understandable for many to conclude that the high dc precision represented by the better performing versions of the OP07 and OP27 class devices would be sufficient for most applications. More recently however, the ground rules have changed.

While the high precision is still often sought, amplifier versions with single-supply capability are now in demand, as are tiny and even tinier packages. The traditional chip designs of the OP07/OP27 generation often can't work in new applications, because the circuit demands single-supply operation, and/or the package size is incompatible with the large chip size of the older products.

The small relative scale of some of these modern IC packages is shown in Figure 8-24. In the upper row, the decreasing size going from the 14-pin SOIC at the right to the SC-70 package at the left is quite clear. In the bottom portion of the figure, the SC-70 and SOT-23 packages are shown in another perspective, relative to a US one cent piece.

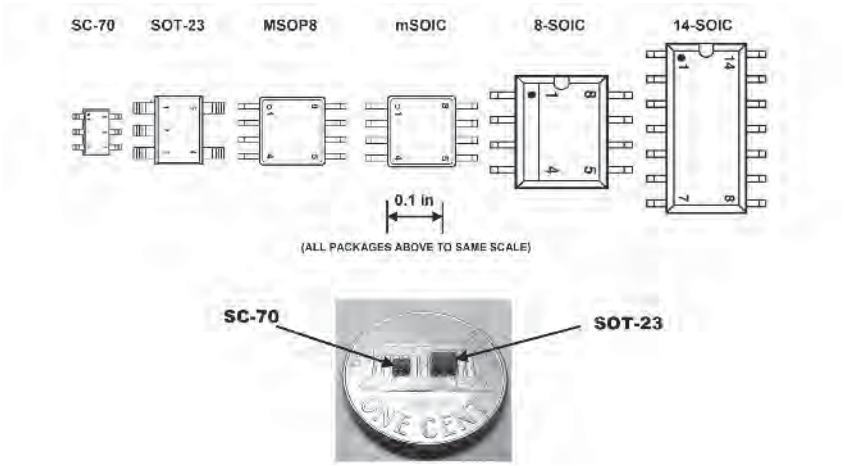


Figure 8-24: The relative scale of some modern IC op amp packages

Two very recent OP07 lineage devices from ADI address these two issues. One is the *OP777* op amp series, which includes the OP777 (single), the OP727 (dual) and OP747 (quad) devices (see Reference 32). Designed by Derek Bowers and released in 2000, these new devices feature rail-to-rail CMOS output stages, a ground sensing bipolar PNP input stage, and a 270 µA operating current. These designs operate over a supply range of 2.7 V–30 V, in MSOP, SOIC and TSSOP packages.

Even more recent is the *OP1177* series, also designed by Derek Bowers and released in 2001. This series includes the OP1177 (single), the OP2177 (dual) and OP4117 (quad) devices (see Reference 33). This design series has a slightly higher operating current than the OP777 series, at 400 µA per amplifier, and it operates from dual supplies of ±2.5 V to ±15 V. While not aimed at single-supply applications, this design does offer a wide range of small packages, with specifications applicable over a –40°C to +125°C range.

Precision JFET IC Op Amps—AD503 to the AD820/AD822/AD824 and AD823 Families

The development of FET input IC op amps was neither as rapid nor as straightforward as the growth of their bipolar IC cousins. There were numerous reasons for this, which will become apparent as this narrative progresses.

First of all, the relative scarcity of high quality FET input op amps early in the history of ICs was certainly not because no one wanted them, but rather because very few could make them. Many FET input op amps had already existed from the days of modular and hybrid types (see preceding section of this Chapter), and FET input amplifiers in general were highly sought after for fast signal processing and low current instrumentation uses. Unfortunately, the development of high performance monolithic FET IC op amps was to become a somewhat long and torturous process.

An early FET input op amp was by Douglas Sullivan and Mitch Maidique. This ADI amplifier was known as the *AD503* and *AD506*, and it was released in 1970. A schematic and photo of the chips used for this design is shown in Figure 8-25.

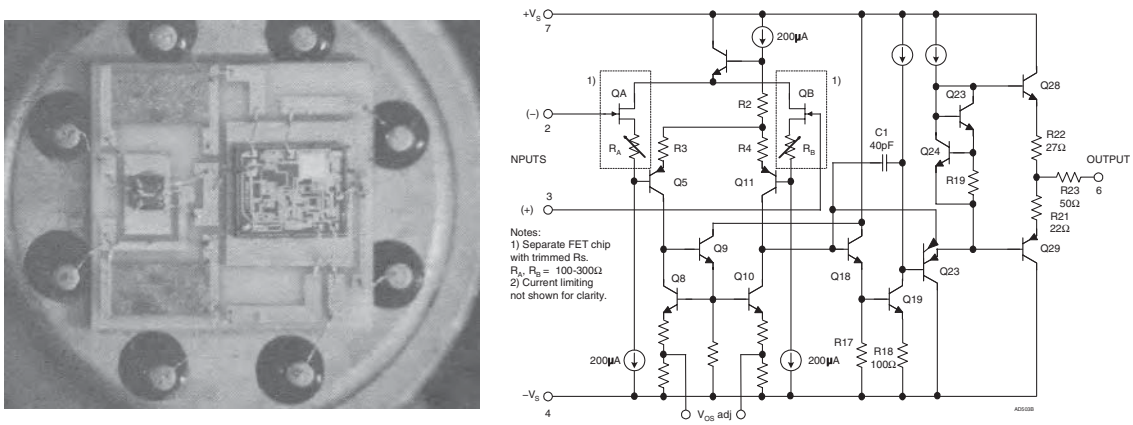


Figure 8-25: The AD503 and AD506 two-chip hybrid IC op amps

As should be evident from the schematic, this amplifier used two chips. One was a main amplifier chip, somewhat similar to a 741 after the input stage. The input stage consisted of a selected N-channel JFET pair, Q_A and Q_B. In the photo to the left, the two active chips can be noted at center right and left,

respectively. Also used was a pair of trimmed resistors, R_A and R_B, shown at the left upper and lower corners of the substrate.

In the case of the AD506J and K grades, these resistors were laser trimmed for lowest offset, delivering to the user devices with maximum offset of no more than 3.5 mV and 1.5 mV, respectively. The nontrimmed AD503 was similar in function, except for higher initial offset (which could be trimmed by the user, via the offset adjust pins). Because of the bootstrapping configuration used, the design had excellent CM specifications—CMR typically was 90 dB, with constant bias current over the input range. It is worthy of note that the AD503/AD506 bias current (as well as later ADI FET input devices) was specified *after a five minute warmup period, a conservative method not used by all op amp makers*.

Operation of the AD503/AD506 family was described in a 1971 applications bulletin (see Reference 35). There were also related uncompensated amplifier types, namely the *AD513* and *AD516* (see Reference 36). Later on, an even tighter *AD506L* grade was introduced, with a 1 mV (max) offset and a 10 µV/°C (max) drift (see Reference 37).

Shortly after the time frame of the early bipolar op amps, there were also several completely monolithic FET input IC op amps, for example the Fairchild µ*A740*, and the Intersil *ICL8007* (see Reference 38). The ICL8007 was perhaps the best of these early completely monolithic P-channel FET input op amps, but that isn't saying a lot. Offset voltages could be as high as tens of mV, and drifts several tens of µV/°C. Input current was low, but that was about the best that could be said of them.

The problem with all the monolithic FETs of the early seventies was simply that the FET devices themselves were poorly controlled. To make any material improvement in monolithic FET IC op amps, a fundamentally better process was needed.

In 1974, this was to happen, in the form of a paper by two National Semiconductor engineers, Rod Russell and David Culmer (see Reference 39). In this paper Russell and Culmer described a new fabrication technique for making FET devices, using *ion-implantation*. This allowed more stable P-channel JFETs to be made, along with quality NPN bipolars. The same paper also described a new series of FET input op amps, the *LF155/LF156/LF157* devices. These parts had much lower offsets and drifts than any previous all-monolithic FET op amp, 5 mV (max) for offset and a typical drift of 5 µV/°C.[8]

While the idea of ion-implantation caught on and became an industry standard method of IC fabrication, the same was not entirely true for the LF155/156/157 devices. Although they were second-sourced (and are still available), others sought a cleaner solution to a standard FET IC op amp topology. The LF155 series used an asymmetrical topology, and there was difficulty controlling the quiescent current.

At PMI, George Erdi designed an FET input op amp series to compete with the National LF155/156/157 parts, which were called the *OP15*, *OP16*, and *OP17*, respectively. They used zener-zap trimming and bias current cancellation; and the best A and E grades achieved offsets of 500 µV (max), and drifts of 5 µV/°C (max).

RCA introduced their answer for a general-purpose FET input op amp, the *CA3130*, also in 1974 (see Reference 40). Using a P-channel MOS input stage and a CMOS output stage, this device was suitable for lower voltage, single-supply uses. It was not, however, a high precision part, due mostly to the poor stability of the MOS devices used. Nevertheless, it was high on general utility, as were the *CA3140* and other spin-offs.

Texas Instruments got into the FET op amp market with their own amplifier series in 1978 (see Reference 41). These devices, in the form of singles, duals, and quads of various power ratings (and speed) did use a PFET input pair operating into a current mirror, with a conventional second stage (a la the 101 or 741, but with higher speed). This line, the *TL06x, TL07x,* and *TL08x*, became standard devices, and are still

[8] Specifications are quoted from December 2001 data sheet for LF155 and LF156 devices.

available. While the faster slew rate and symmetrical signal path of these devices helped ac applications, they weren't designed for high precision.

ADI had been working on an improved FET input monolithic IC op amp, and introduced the first of a long series of devices, the *AD542*, in 1978 (see Reference 42). This two-stage circuit design used a P-channel JFET input differential pair, followed by a second stage integrator. Careful design and laser trimming achieved a maximum offset as low as 0.5 mV in the AD542L, and a maximum drift of 10 μV/°C. While this was not as good as the best bipolar input amplifiers, it was better than any other monolithic FET had done.

Continuing along this same path were other amplifiers such as the *AD544*, a higher speed relation to the AD542, introduced in 1980 (see Reference 43). Both of these devices were designed by Lew Counts, and were aimed at fast settling data acquisition use. They were followed in 1981 by dual counterparts, the *AD642* and *AD644* (see Reference 44). All these devices had trimmed, zero TC supply and input stage currents, for overall stability and predictable slew rate. These features were retained in later precision devices.

This series of JFET input op amps reached their highest precision in 1982, with the introduction of the *AD547* (see Reference 45). This device, designed by Scott Wurcer, achieved for the first time in a monolithic FET op amp a maximum drift of 1 μV/°C, combined with a 250 μV (max) offset, for the AD547L grade of the part. The goals of such low offset and drift were met with laser trimming for both offset and drift at the wafer level. This also has become routine for all high precision ADI FET amplifiers.

The AD711/AD712/AD713 and OP249 IC Op Amps

In 1986 the *AD711/AD712* and *AD548/AD648* FET op amp families were introduced by ADI (see Reference 46). The AD711/AD712 were, respectively, single and dual parts with finely tuned specifications, designed to meet general-purpose as well as intermediate precision uses, but at a moderate cost. The AD712KN sold for $1.90 in quantities of 100, while the AD648KN sold in similar lots for $2.60.

The series featured offset voltages of 500 μV (max), a drift of 10 μV/°C (max) for the AD711K, at a quiescent current of 3 mA. The AD548K had similar offset voltage specifications, and half the drift, at a supply current of 200 μA. JoAnn Close designed the AD548/AD648 series of amplifiers, with inputs from Scott Wurcer and Lew Counts.

Scott Wurcer designed the AD711/AD712 series. The AD711 and AD712 were ultimately to be joined by a quad version, the *AD713*. This family of JFET IC op amps have been very popular since their introduction, and are still available.

Prior to the 1990 acquisition by ADI, PMI introduced their own dual JFET input IC op amp, the *OP249*. Designed by Jim Butler, this similarly specified dual op amp competed directly against the AD712.

Electrometer IC Op Amps

One area of great demand on op amp performance has traditionally been the *electrometer amplifier*, where input currents are required to be less than 1 pA. In the days of the modular op amp, such ultralow current devices as the model 310 and 311 varactor bridge amplifiers had addressed this role. (See the previous section of this chapter for a basic discussion on these amplifiers.) It should be understood that the term electrometer amplifier is here meant to imply any amplifier with ultralow bias currents. It might be a varactor bridge based design, or it might be some other type of front end allowing ultralow bias currents, for example several semiconductor types—MOSFETs, JFETs, and so forth.

The AD515 and AD545 Hybrid IC Electrometer Amplifiers

In hybrid IC form, there were a couple of early electrometer op amps from ADI. The first of these was the *AD515*, a two-chip hybrid similar in general architecture to the AD503 (discussed in conjunction with

Figure 8-25). The AD515 operated at a low power, with a quiescent current of 1.5 mA (see Reference 47). It achieved some impressively low input currents; 75 fA for the best grade AD515L, while maintaining a low offset of 1 mV(max). The AD515 was a successful product, with specifications that were not soon to be eclipsed.

Another early two-chip hybrid IC electrometer op amp was the *AD545*, introduced in 1978 (see Reference 48). This design also operated at low power like the AD515, but with a higher maximum input bias current, 1 pA for the AD545L.

Monolithic IC Electrometer Amplifiers

One of the early monolithic IC electrometer op amps, was the *OPA111*. Burr-Brown introduced this device in 1984 (see Reference 49). Designed by Steve Millaway, the OPA111 used a dielectrically-isolated process for fabrication.

The OPA111 circuit employed P-channel JFETs in the input and second stages, and a first stage cascode design for low bias current variation with input CM changes. The design addressed some of the weak points of the previous LF155/156/157 series (Reference 39). Reference 49 cited several LF15x circuit weaknesses; one was the use of current source loading for the input JFET pair, another was the means of offset trimming, and another was potential susceptibility to popcorn noise, due to the noise currents of the second stage bipolar differential pair. These points were addressed by the OPA111 design.

The OPA111 name was said to have been based on the combination of three key specs; 1 mV (max) offset, a drift of 1 μV/°C (max), and an input voltage noise of 1 μV rms in a 10 Hz–10 kHz bandwidth. This particular combination of specifications was tough to beat, and the OPA111 became a successful IC op amp.

Released in 1987, the first completely monolithic IC electrometer op amp from ADI was the *AD549*, designed by JoAnn Close and Lew Counts (see Reference 50). This op amp achieved its low bias current by virtue of the use of a new "topgate" FET, as designed by Jody Lapham and Paul Brokaw (see Reference 51), plus a sophisticated scheme of bootstrapping around the critical input P-channel JFET pair.

A schematic as adapted from the associated patent is shown in Figure 8-26 (see Reference 52). In the AD549 circuit, the input FETs are J6 and J7 with the input signals applied to their top gates at 10 and 12. The back gates BG1 and BG2 of the pair are biased at approximately the same DC level by a bootstrap loop

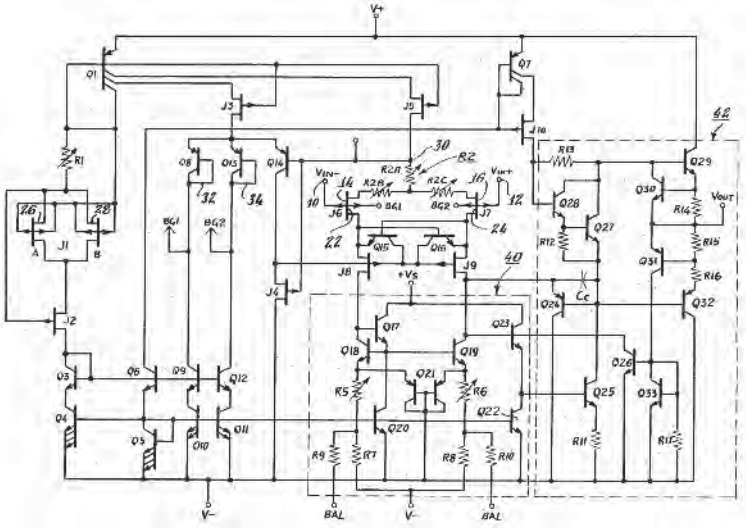


Figure 8-26: The AD549 electrometer IC op amp schematic (adapted from US Patent 4,639,683)

through Q14, and Q13– Q8. A second bootstrap loop through J4 and J8–J9 bootstraps the drains of J6–J7, thus providing for an input bias current level independent of CM voltage, over a ±10 V range.

With this circuit, built on a junction-isolated process, the AD549L was able to achieve a bias current of less than 60 fA, along with a 500 µV (max) offset and a drift of 10 µV/°C (max). It was provided in a hermetically sealed TO-99 package, with Pin 8 connected to the case for guarding within the final application circuit. The AD549L sold for $15.45 in 100 piece lots.

In 1988 ADI introduced another electrometer amplifier based on the design of the AD549, the *AD546* (see Reference 53). JoAnn Close also designed this op amp, and it was offered in a plastic package with somewhat relaxed specifications (vis-à-vis the AD549). The AD546KN had a maximum bias current of 500 fA, a maximum offset of 1 mV, and a drift of 20 µV/°C (typ). It sold for $4.50 in 100 piece lots.

The very latest electrometer amplifier in this series is the still-supplied *AD795*. It is available in an SOIC package and has bias currents of 1 pA or less (see Reference 54).

The AD743/745 Low Noise JFET IC Op Amps

Prior to about 1990, input voltage noise performance in JFET IC op amps had never been competitive with the best bipolar devices, many of which achieved noise densities of 3 $nV/\sqrt{Hz}$ (see earlier OP27 discussions).

In 1990, ADI introduced an answer to applications such as hydrophone amplifiers, which require simultaneously low voltage and current noise from an amplifier. The new amplifier was the *AD743* and *AD745*, designed by Scott Wurcer (see Reference 55). The design of these amplifiers attacked the voltage noise issue by the use of a quad array of very large input transistors, as described in Reference 56.[9]

The result was an input-referred noise of 2.9 $nV/\sqrt{Hz}$ (at 10 kHz) for the two devices, and precision dc amplifier performance specifications. The basic AD743 is a unity-gain stable part, while the faster AD745 is stable at noise gains of five or more.

The AD820/AD822/AD824 and AD823 Series JFET IC Op Amps

In the early 1990s, the first of a series of JFET op amps on the ADI CB process began to appear. This process featured comparable speed and gain NPN and PNP bipolars, designed by Jody Lapham and Brad Scharf (see References 57 and 58). It also had an N-channel FET structure, and a neat feature of this FET was that the pinch-off voltage allowed it to be used as a differential pair at the op amp front end, and the two gates could operate linearly to the negative rail. Thus with a common-emitter complementary bipolar output, a rail-to-rail output stage could be built. The combination of these two key features created a single (or dual) supply op amp with a low-current JFET input stage.

The first op amp of this type to appear was the *AD820*, a single low-power op amp, released in 1993 (see Reference 59). The AD820 was designed by JoAnn Close and Francisco dos Santos. The device architecture was very flexible, and it could be operated from single supplies as low as 3 V, or from dual supplies of up to ±18 V. The input bias current was 10 pA (max) for the AD820B, and the quiescent current was 800 µA (typical).

With the success of the AD820, a dual version was the obvious next step, and the *AD822* appeared in 1994, with specs similar to the AD820 (see Reference 60). Rounding out this family next was the *AD824*, which appeared in 1995 (see Reference 61).

[9] Of course, "very large" is a relative description. Nevertheless, Figure 6 of Reference 56 shows the four input stage transistors consuming about one-half of the chip area.

The AD820/AD822/AD824 were relatively low power parts, with moderate speed. In 1995 a higher speed dual using the same general topology appeared, the *AD823* (see Reference 62). Designed by Jeff Townsend, this amplifier had a 16 MHz bandwidth, and a 22 V/μs slew rate. It also operated from a wide supply range, ±1.5 V to ±18 V dual supplies, or single supplies of +3 V to 36 V.

High Speed IC Op Amps

In the earliest years of IC op amps, everyone was using essentially the same NPN bipolar process, and speed was severely limited because of the slow PNP transistors available. An early scheme to partially get around the PNP bottleneck was the *LM118/218/318*, designed by Bob Dobkin at National Semiconductor in 1971 (see Reference 63). ADI produced their own version of this op amp, the *AD518*, designed by Dave Kress. Although these amplifiers did achieve much higher slew rate and bandwidth, they did not settle fast, nor were they well-suited to driving low impedance loads.

In the early seventies, just about the only truly fast IC process was owned by Harris Semiconductor. This dielectrically isolated process produced equal speed NPN and PNPs, and the Harris HA2500 series became popular for fast settling characteristics. In 1973 ADI released the fast *AD509* op amp, a screened Harris part (see Reference 64).

Until junction isolated CB processes came on board, the dielectrically isolated parts were to dominate high speed applications. There were however, notable exceptions to this general rule. The *AD744*, designed by Scott Wurcer, was introduced in 1988 (see Reference 65). Although this op amp still used a basic NPN process, it took advantage of ion-implanted P-channel FETs for the input differential stage, and could settle quickly and cleanly, reaching a 900 ns settling time to 0.01%.

ADI introduced a high speed 36 V CB process in 1988 (see References 57 and 58, again), and with it, a host of fast IC op amps. Among these were a high speed voltage feedback group, the *AD840* series, and the *AD846* current feedback op amp, all designed by Wyn Palmer. Many other very successful op amps were to soon follow in this series, using the CB process. Notable among them were the unity-gain stable *AD847* and externally compensated *AD829*, also designed by Wyn Palmer. Later on, the *AD811* designed by Dave Whitney, was among the first high performance current feedback op amps available on the CB process, achieving very low video distortion specifications while driving 75 Ω cables (see Reference 66).

Frank Goodenough's Op Amp Reporting for Electronic Design

A notable documentation source on these high speed op amp developments was an **Electronic Design** series, by analog editor Frank Goodenough (see References 67–71). The CB process was just the beginning of ADI high speed IC op amps, and within less than a decade a further jump in performance was produced. This was the 12 V XFCB process, introduced in 1993 (see References 72 and 73). This produced such key parts as the *AD8001*, designed by Scott Wurcer (see Reference 74). The AD8001 set new performance standards, hitting a bandwidth of 800MHz on ±5 V supplies, and achieving very low video distortion.

Frank Goodenough's op amp articles continued to provide a valuable source of IC performance, as well as historical references, through the late 1990s, including other op amp categories as well (see References 75–78). He passed away in February of 1998, and was fittingly memorialized by Roger Allan of **Electronic Design** (see Reference 79).

References: IC Op Amps

(Note: Appended annotations indicate relevance to op amp history.)

Birth of the Monolithic IC Op Amp, General-Purpose IC Op Amps

1. Bob Widlar, "Design Techniques for Monolithic Operational Amplifiers," **IEEE Journal of Solid-State Circuits**, Vol. SC-4, August 1969. *(Design methods used in μA709, LM101A and LM108.)*
2. "The μA702 Wideband Amplifier," Chapter 5 within James N. Giles, Editor, **Fairchild Semiconductor Linear Integrated Circuits Handbook**, Fairchild Semiconductor, 1967, pp. 33–55. *(A detailed design and application discussion of the μA702 IC op amp.)*
3. R. J. Widlar, "A Unique Circuit Design for a High Performance Operational Amplifier Especially Suited to Monolithic Construction," **Proceedings of the NEC**, Vol. XXI, October 1965, pp.85–89. (*The μA709, the first widely used IC op amp.)*
4. Robert J. Widlar, "Monolithic Op Amp with Simplified Frequency Compensation," **EEE**, July 1967. (*The LM101 IC op amp.)*
5. James Solomon, "The Monolithic Operational Amplifier: A Tutorial Study," **IEEE Journal of Solid-State Circuits**, Vol. SC-9, No. 6, December 1974. See also National Semiconductor AN-A. *(The classic paper on IC op amp design techniques.)*
6. Dave Fullagar, "A New High Performance Monolithic Operational Amplifier," **Fairchild Semiconductor Application Brief**, May 1968. *(The μA741 IC op amp.)*
7. Robert J. Widlar, "IC Op Amp with Improved Input-Current Characteristics," **EEE**, December 1968. *(The LM101A IC op amp.)*
8. Ronald Russell, Thomas Frederiksen, "Automotive and Industrial Electronic Building Blocks," **IEEE Journal of Solid-State Circuits**, Vol. SC-7, December 1972, pp. 446–454. *(The LM324 and other single-supply Ics.)*
9. Data sheet for **AD741J, K, L, S Lowest Cost High Accuracy IC Op Amps**, Analog Devices, Inc., January 1973.

SuperBeta IC Op Amps

10. Robert J. Widlar, "The LM110 An Improved IC Voltage Follower," **National Semiconductor LB-11**, March 1970. *(The use of superbeta transistors in follower-connected IC op amps LM102 and LM110.)*
11. R. J. Widlar, "Super Gain Transistors for ICs," **IEEE Journal of Solid-State Circuits**, Vol. SC-4, August 1969 pp. 249–251. *(General principles of super-beta transistors in IC op amps.)*
12. Jim Solomon, William Davis, P. Lee, "A Self-Compensated Monolithic Operational Amplifier with Low Input Current and High Slew Rate," **ISSCC Digest of Technical Papers**, February 1969, pp.14–15. *(The use of superbeta transistors in the MC1556 IC op amp.)*
13. Bob Widlar, "IC Op Amp Beats FETs on Input Current," **EEE**, December 1969. *(The superbeta input LM108 IC op amp.)*
14. George Erdi, Jim Williams, "Precision Op Amp Serves Host of Needs," **Electronic Design**, September 1, 1983. *(The LT1008 and LT1012 superbeta input IC op amps.)*
15. Modesto Maidique, "A High Precision Super Beta Operational Amplifier," **IEEE Journal of Solid-State Circuits**, Vol. SC-7, December 1972. See also: "AD508: Monolithic Chopperless Op Amp Super β Inputs, <1 μV/°C Drift," **Analog Dialogue**, Vol. 6, No. 1, 1972. *(The superbeta input AD508 IC op amp.)*

16. Modesto Maidique, "Monolithic Operational Amplifier With 1 μV/°C Drift," **Analog Dialogue**, Vol. 5, No. 3. *(The AD504 IC op amp.)*
17. Preliminary Data sheet for **AD508J, K, L IC Chopperless Low Drift Operational Amplifier**, Analog Devices, Inc., June, 1972.
18. Doug Grant, "Low Drift Super Beta Op Amp," **Analog Dialogue**, Vol. 12, No. 1. *(The AD517 IC op amp.)*
19. Richard Wagner, "Laser-Trimming on the Wafer," **Analog Dialogue**, Vol. 9, No. 3. *(Laser wafer trimming of thin-film resistors for IC offset and gain.)*
20. "Precision Op Amp," **Analog Dialogue**, Vol. 24, No. 1. *(The AD705 super-beta precision IC op amp.)*
21. "Two Precision Dual Op Amp Families," **Analog Dialogue**, Vol. 24, No. 3. *(The AD706 and OP297 superbeta precision dual IC op amps.)*
22. "Quad Op Amp," **Analog Dialogue**, Vol. 25, No. 1. *(The AD704 super-beta precision quad IC op amp.)*

Precision Bipolar IC Op Amps

23. George Erdi, "A Low Drift, Low Noise Monolithic Operational Amplifier For Low Level Signal Processing," **Fairchild Semiconductor Application Brief APP-136**, July 1969. *(The μA725 IC op amp.)*
24. George Erdi, "Minimizing Offset Voltage Drift With Temperature In Monolithic Operational Amplifiers," **Proceedings of NEC**, 1969 pp. 121–123. *(Method of offset trim for minimum drift in precision dc amplifiers.)*
25. George Erdi, "Instrumentation Operational Amplifier With Low Noise, Drift, Bias Current," **Precision Monolithics APP Note**, 1972. *(The OP05 IC op amp.)*
26. George Erdi, "A Precision Trim Technique for Monolithic Analog Circuits," **IEEE Journal of Solid-State Circuits**, Vol. SC-10, December, 1975 pp. 412–416. *(The "zener-zap" offset trim method.)*
27. Donn Soderquist, George Erdi, "The OP-07 Ultra-Low Offset Voltage Op Amp," **Precision Monolithics AN-13**, December, 1975. *(The OP07 IC op amp.)*
28. "Precision Bipolar Op Amp Has Lowest Offset, Drift," **Analog Dialogue**, Vol. 22, No. 1. *(The AD707 precision IC op amp.)*
29. Bill Schweber, "Dual Bipolar Op Amp Provides Superior Matching of Specs," **Analog Dialogue**, Vol. 23 No. 1. *(The AD708 precision IC op amp, dual of the AD707.)*
30. George Erdi, Tom Schwartz, Scott Bernardi, and Walt Jung, "Op Amps Tackle Noise-and for Once, Noise Loses," **Electronic Design**, December 12, 1980. *(The OP27 and OP37 IC op amps.)*
31. George Erdi, "Amplifier Techniques for Combining Low Noise, Precision, and High-Speed Performance," **IEEE Journal of Solid-State Circuits**, Vol. SC-16, December, 1981 pp. 653–661. *(Design techniques of the OP27 and OP37 IC op amps.)*
32. "Precision Micropower Single-Supply Op Amps Have 100 μV max Offset," **Analog Dialogue**, Vol. 34, No. 4. *(The OP777, OP727, and OP747 precision single and dual supply, rail-rail output single/dual/quad IC op amps.)*
33. Data sheet for "**Precision Low Noise Low Input Bias Current Operational Amplifiers OP1177/OP2177**," www.analog.com.

Precision JFET IC Op Amps

34. Doug Sullivan, Modesto Maidique, "High Performance IC FET-Input Op Amp," **Analog Dialogue**, Vol. 4, No. 2, 1970. *(The AD503 and AD506 two-chip hybrid IC op amp.)*
35. Richard S. Burwen, Doug Sullivan, "AD503, AD506 IC FET Input Operational Amplifiers Technical Bulletin," **Analog Devices Application Bulletin**, August 1971. *(Design and application of the AD503 and AD506 two-chip hybrid IC op amp.)*
36. "FET-Input ICs Can Slew at 50 V/µs," **Analog Dialogue**, Vol. 5, No. 3, 1971. *(The AD513 two-chip hybrid IC op amp.)*
37. "AD506L: Economical Low-Drift FET-Input," **Analog Dialogue**, Vol. 7, No. 1, 1973. *(The AD506L two-chip hybrid IC op amp.)*
38. Dave Fullagar, "Better Understanding of FET Operation Yields Viable Monolithic JFET Op Amp," **Electronics**, November 6, 1972. *(The ICL8007 IC op amp.)*
39. Ronald W. Russell, Daniel D. Culmer, "Ion-Implanted JFET-Bipolar Monolithic Analog Circuits," **ISSCC Digest of Technical Papers**, February 1974, pp. 140–141, 243. *(Ion-implanted JFETs, and the LF155/156/157 series of FET IC op amps.)*
40. Otto Schade, Jr. "CMOS/Bipolar Linear Integrated Circuits," **ISSCC Digest of Technical Papers**, February 1974, pp. 136–137. See also: R. L. Sanquini, "Building C-MOS, Bipolar Circuits on Monolithic Chip Enhances Specs," **Electronics**, October 3, 1974. *(The CA3130 CMOS IC op amp.)*
41. Dale Pippenger, Dale May, "Put BIFETs Into Your Linear Circuits," **Electronic Design,** January 4, 1978, pp. 104–107, 109–111.
42. Lew Counts , Rich Frantz, "High-Performance, Low-Cost Bipolar-FET Op Amp," **Analog Dialogue**, Vol. 12, No. 3, 1978. *(The AD542 monolithic FET IC op amp.)*
43. "Fast FET Op Amp," **Analog Dialogue**, Vol. 14, No. 1, 1980. *(The AD544 IC op amp.)*
44. "High Performance Dual FET Op Amps," **Analog Dialogue**, Vol. 15, No. 2, 1981. *(The AD642/AD644 IC op amps.)*
45. "First Monolithic FET Op Amp with 1 µV/°C Drift," **Analog Dialogue**, Vol. 16, No. 1 1982. *(The AD547 drift and offset trimmed IC op amp.)*
46. "Highest-Performing Low-Cost BiFET Op Amps," **Analog Dialogue**, Vol. 20, No. 2, 1986, p. 22.
47. Dave Kress, "FET-Input Electrometers," **Analog Dialogue**, Vol. 10, No. 1, 1976, p.11.
48. "FET-Input AD545," **Analog Dialogue**, Vol. 12, No. 3, 1978, p.18.
49. Steve Millaway, "Monolithic Op Amp Hits Trio of Lows," **Electronic Design,** February 9, 1984. *(The OPA111 low bias current IC op amp.)*
50. JoAnn Close, Lew Counts, "Junction-Isolation Process Yields 50 fA Op Amp," **Electronic Design**, July 10, 1986, pp.99–102, 104. See also: JoAnn Close, "Monolithic Electrometer Has 60 fA Max Bias Current," **Analog Dialogue**, Vol. 21, No. 2, 1987, p. 22. *(The AD549 electrometer IC op amp.)*
51. Jerome F. Lapham, Adrian P. Brokaw, "Low-Leakage JFET," **US Patent 4,985,739**, filed April 27, 1987, issued January 15, 1991. *(Design of the 'top-gate' low-leakage JFET IC process.)*
52. Lewis Counts, JoAnn Close, "Very Low Input Current JFET Amplifier," **US Patent 4,639,683**, filed February 7, 1986, issued January 27, 1987. *(The 'top-gate' low-leakage JFET IC process and AD549 IC op amp.)*

53. "High Performance Electrometer Op Amp in Plastic 8-Pin DIP," **Analog Dialogue**, Vol. 23, No. 4, 1988, p. 12. *(The AD546 electrometer IC op amp.)*

54. "Low-Noise, Low-Drift Precision Op Amps for Instrumentation," **Analog Dialogue**, Vol. 27, No. 1, 1993. *(The AD795 low noise, low I_B and OP213 dual single-supply, precision IC op amps.)*

55. "FET-Input Op Amp Has Lowest Combined V and I Noise," **Analog Dialogue**, Vol. 25, No. 1, 1991, p. 12. *(The AD743 and AD745 low noise IC op amps.)*

56. Scott Wurcer, "A 3 nV/√Hz, DC-Precise, JFET Operational Amplifier," **Proceedings of BCTM**, 1989, pp. 116–119. *(Design principles of the AD743 and AD745 low noise IC op amps.)*

57. "Op Amps Combine Superb DC Precision and Fast Settling," **Analog Dialogue**, Vol. 22, No. 2, 1988. *(The AD846 IC op amp, the AD840 series, and the high speed CB process used.)*

58. Jerome F. Lapham, Brad W. Scharf, "Integrated Circuit with Complementary Junction-Isolated Transistors and Method of Making Same," **US Patent 4.969,823**, filed May 5, 1988, issued Nov. 13, 1990. *(Design of the ADI CB IC process.)*

59. "Single-Supply FET," **Analog Dialogue**, Vol. 27, No. 2, 1993, p. 26. *(The AD820 single-supply rail-rail output IC op amp.)*

60. "Dual FET, 3 V to ±18 V," **Analog Dialogue**, Vol. 28, No. 1, 1994, p. 24. *(The AD822 single-supply rail-rail output dual IC op amp.)*

61. "Quad JFET, Single-Supply Op Amp," **Analog Dialogue**, Vol. 29, No. 1. *(The AD824 single-supply, rail-rail output quad IC op amp.)*

62. "Dual 16MHz Rail-Rail FET," **Analog Dialogue**, Vol. 29, No. 2. *(The AD823 single-supply, rail-rail output dual IC op amp.)*

High Speed IC Op Amps

63. Bob Dobkin, "LM118 Op Amp Slews 70 V/µs," **National Semiconductor LB-17**, September 1971. *(The high slew rate LM118 IC op amp.)*

64. "AD509: Fast Op Amp 2 µs to 0.01%," **Analog Dialogue**, Vol. 7, No. 1, p. 10. *(The AD509 fast IC op amp.)*

65. Kristen Dinsmore, "Fast, Accurate BIFET Op Amp Settles to 0.01% in 900 ns Max," **Analog Dialogue**, Vol. 21, No. 2, 1988, pp. 14–15.

66. Dave Whitney and Walt Jung, "Applying a High-Performance Video Operational Amplifier," **Analog Dialogue**, Vol. 26, No. 1 1992, pp. 10–13. *(The AD811 high-speed, high output video IC op amp and applications.)*

67. Frank Goodenough, "Focus Monolithic IC Op Amps: Faster and More Precise," **Electronic Design**, February 4, 1988, pp. 127–132. *(A survey of high-speed IC op amps.)*

68. Frank Goodenough, "A Slew of New High Performance Op Amps Shatters Speed Limits," **Electronic Design**, March 3, 1988, pp. 29–32. *(High speed IC op amps and processes, including the ADI CB process.)*

69. Frank Goodenough, "New Processes, Designs Boost IC Op Amp Speeds," **Electronic Design**, April 12, 1990, pp. 45–48, 52–56. *(Survey of high speed IC op amps with emphasis on CB processes and current feedback architectures.)*

70. Frank Goodenough, "Linear ICs Attain 8 GHz NPNs, 4 GHz PNPs," **Electronic Design**, December 19, 1991, pp. 35–37, 40, 43–45. *(The high-speed 'UHF-1' DI process as used by Harris.)*

71. Frank Goodenough, "New Processes to Spawn Next-Generation Analog, Mixed-Signal, Power ICs," **Electronic Design**, January 2, 1992, pp. 59–62, 64–66, 68, 70. *(Survey of high-speed process developments.)*

72. Frank Goodenough, "Wideband IC Op Amps Reach New Bandwidth Highs," **Electronic Design**, September 2, 1993, pp. 48, 50, 52, 56, 58, 63, 64–66. *(The ADI XFCB process, and a survey of other high speed processes.)*

73. Frank Goodenough, "IC Op Amps Combine Low Cost and Performance," **Electronic Design**, September 2, 1993, pp. 39–40, 42, 46. *(Survey of high speed processes, ADI AD8001 XFCB process IC op amp and AD96XX series IC op amps.)*

74. "Fast Op Amp: High Performance, Low Power, Low Cost," **Analog Dialogue**, Vol. 28, No. 2, 1994, p. 11. *(The AD8001 high-speed IC op amp, first on the XFCB process.)*

75. Frank Goodenough, "Silicon, Analog Processes Becoming More Sophisticated," **Electronic Design**, May 2, 1994, pp. 97,98, 100–103. *(Survey of complementary and mixed signal compatible processes).*

76. Frank Goodenough, "Rail-Rail In-and-Out IC Op Amps Run Off 2.7 V," **Electronic Design**, May 16, 1994, pp. 51, 52, 54, 56, 60, 64–65. *(Survey of rail-rail, low voltage single-supply design techniques and IC op amp devices.)*

77. Frank Goodenough, "Single-Supply Op Amps Come of Age," **Electronic Design Analog Applications Issue**, November 7, 1994, pp. 52–61. *(Survey of rail-rail design techniques and IC op amp devices.)*

78. Frank Goodenough, "Op Amp, ADC Topple Old Price/Performance Marks," **Electronic Design**, December 5, 1994, pp. 75, 76, 78, 80, 81, 84, 87. *(New product highlight of high speed, low power AD8011 IC op amp and AD878 ADC.)*

79. Roger Allan, "Frank Goodenough: 1925–1998," **Electronic Design**, March 9, 1998, p. 6.

Classic Cameo
Bob Widlar—Linear IC Pioneer, Personality

Bob Widlar reviewing his LM10 op amp, circa 1977

(Photo courtesy of Bob Pease and National Semiconductor)

This history of IC op amp developments began with the work of Bob Widlar, back in the early 1960s. Starting with the first successful IC op amp, the μA709, Widlar was to author a virtually unbroken string of IC op amp successes. Only his better-known *op amp* achievements are covered here, so readers should not feel he designed only op amps. As noted earlier, many linear IC design techniques he pioneered early on became standard methods. It should also be understood that he made major contributions to other IC circuits, for example IC bandgap voltage references, and IC three-terminal voltage regulators.

Throughout his career, Widlar was known not only as an innovator, but also as a colorful personality of the first order. Some Widlar stories can be found in a remembrance offered by Bob Pease.[10] Another tribute was also offered by Jim Solomon, which includes personal views of this most fascinating designer by a number of Widlar's co-workers.[11]

Bob Widlar passed away in February of 1991, at a relatively young age of 53 years. He was running near his home in Mexico, a favorite pastime of his. It is safe to say that his work efforts (and also his play antics) will not be forgotten.

---

[10] Bob Pease. "What's All This Widlar Stuff, Anyhow?" **Electronic Design**, July 25, 1991, pp. 146, 148, 150.

[11] James E. Solomon, "A Tribute to Bob Widlar," **IEEE Journal of Solid-State Circuits**, Vol. SC-26, No. 8, August 1991, pp. 1087–1089.

This page intentionally left blank

INDEX

This page intentionally left blank

SUBJECT INDEX

B

D

G

M

P

This page intentionally left blank

ANALOG DEVICES' PARTS INDEX

STANDARD DEVICE PARTS INDEX